Capacitor Mismatch Calibration Technique to Improve the SFDR of 14-bit SAR ADC

Hua Fan[1], Franco Maloberti[2], Dagang Li[3], Daqian Hu[3], Yuanjun Cen[3] and Hadi Heidari[4]

[1] State Key Laboratory of Electronic Thin Films and Integrated Devices, School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu, China (e-mail:fanhua7531@163.com)

[2]Department of Electrical, Computer, and Biomedical Engineering, University of Pavia 27100, Italy.

[3] Chengdu Sino Microelectronics Technology Co.,Ltd, Chengdu, China

[4] Electronics and Nanoscale Engineering Division, School of Engineering, University of Glasgow, G12 8QQ, Glasgow, UK

Abstract—This paper presents mismatch calibration technique to improve the SFDR in a 14-bit successive approximation register (SAR) analog-to-digital converter (ADC) for wearable electronics application. Behavioral Monte-Carlo simulations are applied to demonstrate the effect of the proposed method where no complex digital calibration algorithm or auxiliary calibration DAC needed. Simulation results show that with a mismatch error typical of modern technology, the SFDR is enhanced by more than 20 dB with the proposed technique for a 14-bit SAR ADC.

Index Terms—Analog-to-Digital Converter, Successive Approximation Register(SAR) ADC, Capacitive digital-to-analog converter(DAC), Capacitor Mismatch Calibration.

I. INTRODUCTION

The increasing availability of sensors and communication technologies have both facilitated and catalysed the development of wearable electronics, which are devices that can be deployed, worn or mated with human skin to pay close attention to activities of individual continuously without disturbing or affecting the activities of people [1]–[5]. At present, considerable interest has been devoted to real-time continuous monitoring physiological biomarkers of an individual using wearable biosensors [6], [7], which are essential to the realization of personalized medicine through continuously monitoring state of health. For example, a mechanically flexible and fully integrated sensor array is presented in [8] for multiplexed in situ perspiration analysis, which simultaneously and selectively measures sweat metabolites (such as glucose and lactate) and electrolytes, as well as the skin temperature (to calibrate the response of the sensors); Also, a wearable biochemical sensor for monitoring alcohol consumption lifestyle through Ethyl glucuronide (EtG) detection in human sweat is developed in [9]. Smart and high performance wearable sensor node combines sensing, processing, computing and communication technologies, where resolution scalable analog-to-digital converters (ADC) is a crucial block as shown in Fig. 1. While implementing sensor nodes in simple or complex networks, the size and cost of individual sensor node is very critical consideration [10]–[12], accordingly, a very important consideration for ADCs used in wireless sensor networks (WSNs) and body area network (BAN), is the power dissipation, even so, the power of ADCs is still
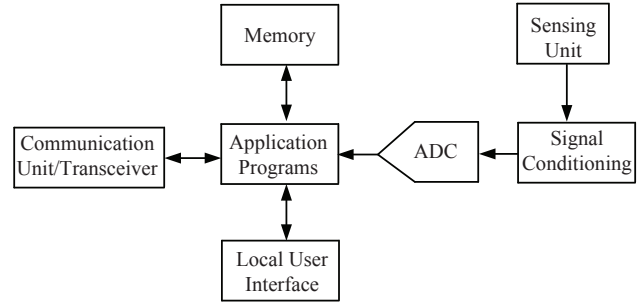

Fig. 1. Basic Architectural Components of smart Sensor Node [24].

much smaller than that of analog front-end [13] in wearable systems. Furthermore, when sensor nodes are used in the body area networks for data collection, linearity and resolution are usually of much more vital importance compared with power consumption, because the amplitude of these signals is quite small. If the ADC resolution is too low, we will not be able to tell the difference between these signals. This might affect the diagnosis of doctors [14]. For instance, electromyography (EMG) requires that the A-D conversion precision should be at least 13-bit [15]. The SAR ADC has been chosen in this work not only because of its excellent power efficiency but also because it offers a flexible binary search algorithm to support scalability or reconfigurability to realize multi-functional and multi-sensing wearable sensor nodes. Beyond that, SAR ADCs are also widely used in RFID, air pollution monitoring, image sensor and smart sensor network [16]–[23].

In low-power high-resolution SAR ADCs, unit capacitor of DAC is chosen according to the matching limitations rather than the thermal noise restrictions. For high resolution SAR ADC, for example, 14 bits, capacitor mismatch needs to be compensated to enhance the SFDR of SAR ADC to be greater than 90 dB, or else, the capacitor mismatch will deteriorate the spurious free dynamic range (SFDR) of a SAR ADC to less than 70 dB [25].

Capacitor mismatch calibration techniques can be always classified into two methods: foreground [26], [27] and background schemes [28]. To satisfy the demands of resolution and

power consumption simultaneously for wearable applications, an inherently linear architecture without calibration maybe preferable.

This work presents dynamic averaging technique: By dynamically selecting different DAC unit elements to represent a given digital input code in different bit cycling operations, the capacitor mismatch errors of the ADC can be dynamically counteracted without the need for extra complicated digital circuits. Simulation results show that more than 20 dB SFDR of improvement is achieved for a 14-bit SAR ADC. The remainder of this paper is organized as follows. section II describes conventional dynamic element matching (DEM) technique, section III describes circuit architecture. Section IV gives detailed description about the dynamic averaging technique proposed, then section V compares the performance between conventional, DEM and dynamic averaging technique proposed. The conclusions are finally drawn in section VI.

II. CONVENTIONAL DEM TECHNIQUE

As well known, if the variance of the mismatch error of the unit capacitor is σ_u, with binary capacitive architecture, the mismatch mainly affects the DNL with maximum at the middle point [29]:

$$\sigma_{DNL,binary} \approx 2^{m/2}\sigma_0 \tag{1}$$

here, m is the resolution of the capacitive array. While for unary capacitive architecture, the error will not be accumulated at the middle point, then [29]

$$\sigma_{DNL,unary} = \sigma_0 \tag{2}$$

as a result, unary architecture may be an appropriate choice for the SAR ADC in consideration of linearity.

On the other hand, the one-sigma SFDR of the ADC output is improved by $10log(2^m - 1)$ dB with conventional DEM calibration technique [30], [31]. As a result, the theoretical improvement of SFDR for 6-bit ADC with unary elements by using the conventional DEM technique is 18 dB.

III. SAR ARCHITECTURE

Because the power of SAR ADC is always much smaller than the analog front end [13], then linearity is given much more consideration than the power.

Fig. 2 shows the block diagram of the 14-bit combined capacitor-resistor SAR ADC, which consists of 6-bit capacitive main DAC and 8-bit resistor-string sub DAC, in total, 64 unit capacitors are applied.

IV. DYNAMIC AVERAGING TECHNIQUE

In this section, the dynamic averaging technique will be discussed based on the main capacitive DAC of capacitor-resistor combined SAR ADC in Fig. 2.

Fig. 4 shows the dynamic averaging technique based on conventional DEM technique [32], [33] in Fig. 3. As well known, the conventional capacitive DAC is based on binary architecture, as shown in Fig. 4(a), at first, redundant capacitor 16C is added to correct the wrong decision, shown in Fig. 4(b),
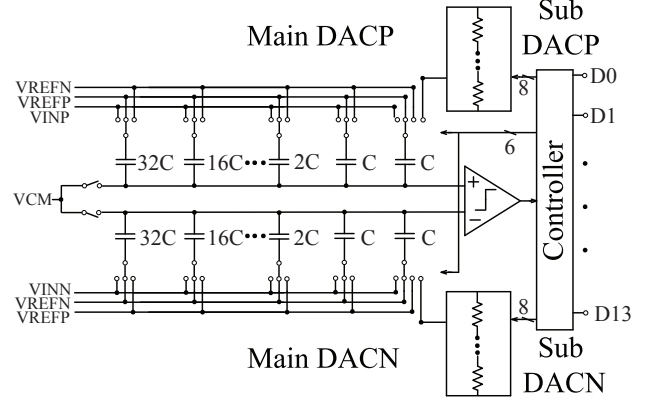

Fig. 2.   A capacitor-resistor combined 14-bit SAR ADC architecture.
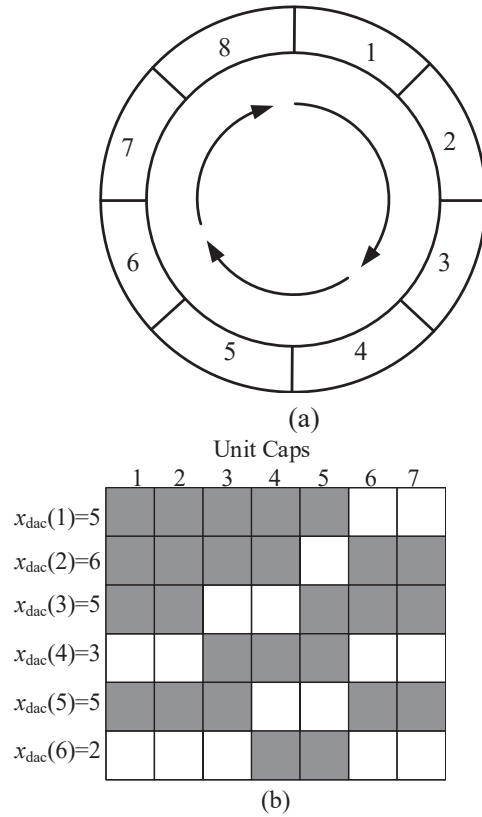

Fig. 3.   (a) Element Selection in Conventional Dynamic Element Matching (DEM) technique; (b) DEM for unit capacitor selection [32], [33]

as a result, a certain range of error does not have influence on the conversion result, then to achieve optimum static linearity, unary architecture is applied in this work, finally, capacitor-resistor combined DAC in Fig. 2 using 80 unary capacitors as 6-bit capacitive main DAC rather than conventional binary architecture. Meanwhile, it is convenient to implement the dynamic averaging scheme with unary capacitive architecture. After sampling the input voltage, the conversion begins with the dynamic averaging. For example, for the i-th conversion,

when input voltage Vin(i)=0.0391, through the binary search, 32C, 8C and C are connected to VREFP in the positive capacitive array, which means the total number of capacitors connected to VREFP is 41, in the following step, the i-th conversion repeats once with the left shift vector of 41 capacitors; for the (i+1)-th conversion, if input voltage Vin(i+1)=0.0031, accordingly, 32C and 8C are connected to VREFP, corresponding to a shift of 40. Generally speaking, for every sampled input voltage Vin(i), the whole conversion repeats once with cycling shift of capacitors, generating two digital output code Dout1(i) and Dout2(i) corresponding to the same input voltage Vin(i), accordingly, the average of these two codes Dout1(i) and Dout2(i) is the final output Dout(i).

(a)

(b)

80 Caps

(c)

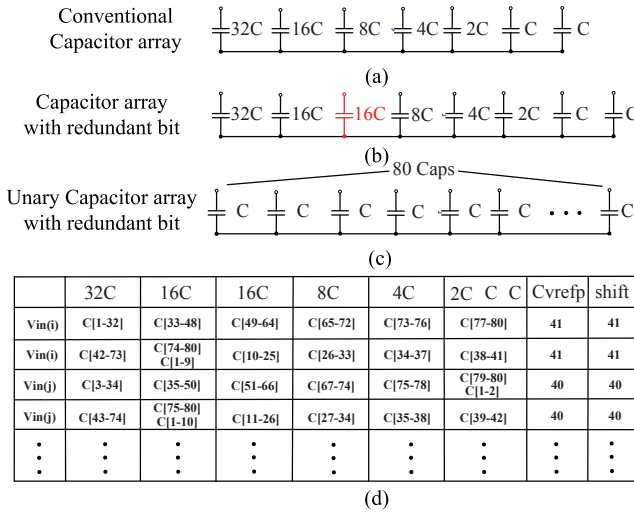|	32C	16C	16C	8C	4C	2C C C	Cvrefp	shift
Vin(i)	C[1-32]	C[33-48]	C[49-64]	C[65-72]	C[73-76]	C[77-80]	41	41
Vin(i)	C[42-73]	C[74-80] C[1-9]	C[10-25]	C[26-33]	C[34-37]	C[38-41]	41	41
Vin(j)	C[3-34]	C[35-50]	C[51-66]	C[67-74]	C[75-78]	C[79-80] C[1-2]	40	40
Vin(j)	C[43-74]	C[75-80] C[1-10]	C[11-26]	C[27-34]	C[35-38]	C[39-42]	40	40
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

(d)

Fig. 4. (a) The conventional 6-bit main capacitive array in Fig. 2; The proposed dynamic averaging method applied to the 6-bit main capacitive DAC features: (b)Redundant capacitor 16C inserted; (c) the Unary Capacitive Architecture; (d) Dynamic Averaging Technique.

V. SIMULATION RESULTS

To demonstrate the proposed dynamic averaging technique, behavioral simulation employing dynamic averaging technique was carried out to evaluate the performance improvement of 14-bit capacitor-resistor combined ADC. In the simulation, only the capacitor mismatch is considered. The capacitor mismatch for every capacitor is randomly generated and the values of the unit capacitors are taken to be Gaussian random variables with standard deviations of 0.1%, 0.2%, 0.3% and 0.4% respectively to cover as much different technologies as possible [34].

Fig. 5 and Fig. 6 show the FFT results based on three switching techniques with respectively Conventional, DEM and dynamic averaging proposed with σ_u=0.1%, σ_u=0.2%, σ_u=0.3% and σ_u=0.4% respectively. In Fig. 5 and Fig. 6, the 14-bit SAR ADC before calibration uses the 6-bit main capacitive array in Fig. 4(a) and the 14-bit SAR ADC after calibration adopts the 6-bit unary capacitive array with dynamic averaging shown in Fig. 4(d). In any case, the improvement of SFDR is over 20 dB.
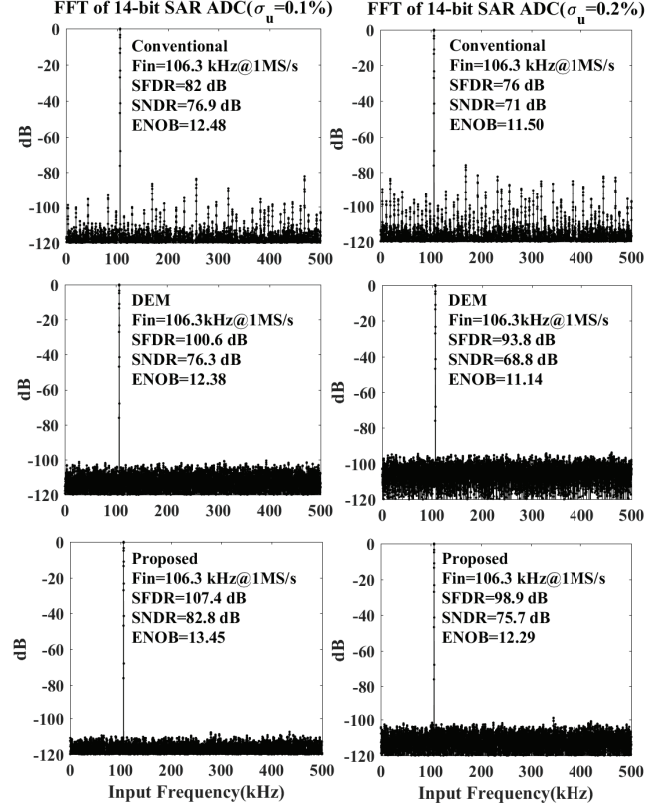

Fig. 5. FFT simulation results for 14-bit SAR ADC with respectively Conventional, DEM and Proposed with σ_u=0.1% (left) and σ_u=0.2% (right)

Fig. 7 and Fig. 8 show the SFDR results based on three switching techniques for 500 Monte Carlo runs with respectively conventional, DEM and dynamic averaging proposed with σ_u=0.1%, σ_u=0.2%, σ_u=0.3% and σ_u=0.4% respectively. Without dynamic averaging technique, the worst-case and the averaged SFDR are 69.7 dB and 79.2 dB respectively with $\sigma_u = 0.2\%$. The variation of SFDR reaches 25 dB. After using the dynamic averaging technique, the worst-case, the averaged and the variation of SFDR are improved from 69.7, 79.2 and 25 dB to 94.8, 101.4 and 11.2 dB, respectively.

Fig. 9 and Fig. 10 show the SNDR results based on three switching techniques for 500 Monte Carlo runs with respectively conventional, DEM and dynamic averaging proposed with σ_u=0.1%, σ_u=0.2%, σ_u=0.3% and σ_u=0.4% respectively. By using the dynamic averaging technique, the worst-case, the averaged of SNDR are improved from 66 and 73.6 dB to 71.1 and 76.4 dB respectively with $\sigma_u = 0.2\%$.

Table I concludes 500 Monte Carlo SNDR and SFDR simulation results with DEM technique, which shows improvements of SFDR by using DEM is about 18 dB in every case, which agrees well with theoretical analysis in section II, for 6-bit ADC with unary elements, improvement of SFDR is about 18 dB by using the conventional DEM technique. However,
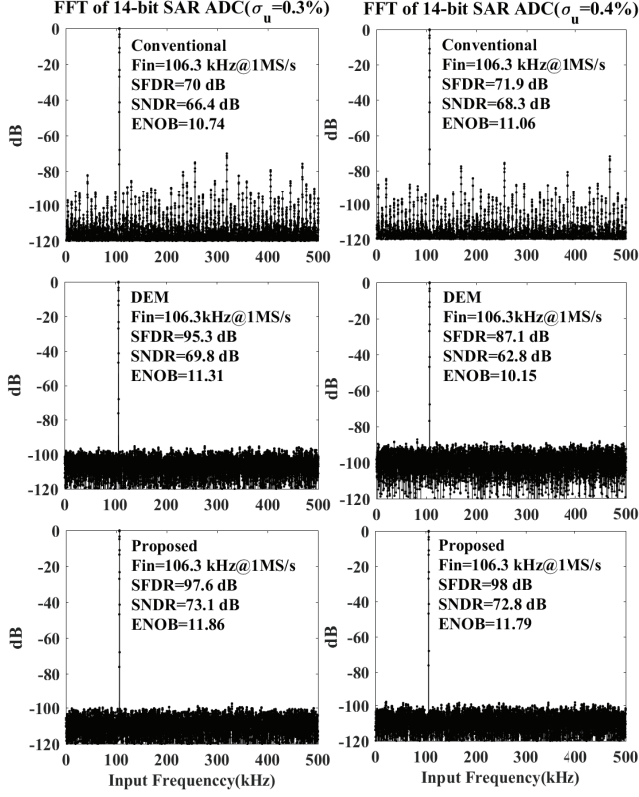
Fig. 6. FFT simulation results for 14-bit SAR ADC with respectively Conventional, DEM and Proposed with σ_u=0.3% (left) and σ_u=0.4% (right)

Fig. 7. 500 Monte Carlo SFDR simulation results for 14-bit SAR ADC with respectively Conventional, DEM and Proposed with σ_u=0.1% (left) and σ_u=0.2% (right)

DEM can not benefit SNDR, SNDR even becomes worse with conventional DEM.

Table II concludes 500 Monte Carlo SFDR simulation results, which shows the approach proposed in this work has no limitation on σ_u, almost 20 dB improvement of SFDR can be obtained in every case. Moreover, about 3 dB SNDR improvement can be achieved by the proposed dynamic averaging technique.

TABLE I
500 MONTE CARLO SIMULATION SUMMARY BY USING DEM

	Conventional (dB)	DEM (dB)	Improvement (dB)
mean(SFDR)(σ_u=0.1%)	85.2	102.3	17.1
mean(SFDR)(σ_u=0.2%)	79.2	97.3	18.1
mean(SFDR)(σ_u=0.3%)	75.8	93.9	18.1
mean(SFDR)(σ_u=0.4%)	73.2	91.4	18.2
mean(SNDR)(σ_u=0.1%)	78.8	77.8	-1
mean(SNDR)(σ_u=0.2%)	73.6	72.4	-1.2
mean(SNDR)(σ_u=0.3%)	70.4	69.1	-1.3
mean(SNDR)(σ_u=0.4%)	67.9	66.5	-1.4

VI. CONCLUSION

Capacitor mismatch calibration based on dynamic averaging for SAR ADCs was proposed. Simulation results demonstrate

TABLE II
500 MONTE CARLO SIMULATION SUMMARY BY USING DYNAMIC AVERAGING

	Conventional (dB)	Proposed (dB)	Improvement (dB)
mean(SFDR)(σ_u=0.1%)	85.2	106.9	21.7
mean(SFDR)(σ_u=0.2%)	79.2	101.4	22.2
mean(SFDR)(σ_u=0.3%)	75.8	97.8	22
mean(SFDR)(σ_u=0.4%)	73.2	95.3	22.1
mean(SNDR)(σ_u=0.1%)	78.8	81.9	3.1
mean(SNDR)(σ_u=0.2%)	73.6	76.4	2.8
mean(SNDR)(σ_u=0.3%)	70.4	72.9	2.5
mean(SNDR)(σ_u=0.4%)	67.9	70.5	2.6

over 20dB SFDR improvement is achieved by using the dynamic averaging with redundancy technique. Meanwhile, no complicated digital calibration algorithm or auxiliary calibration DAC is needed, therefore, the technique proposed is easy to realize on-chip calibration.
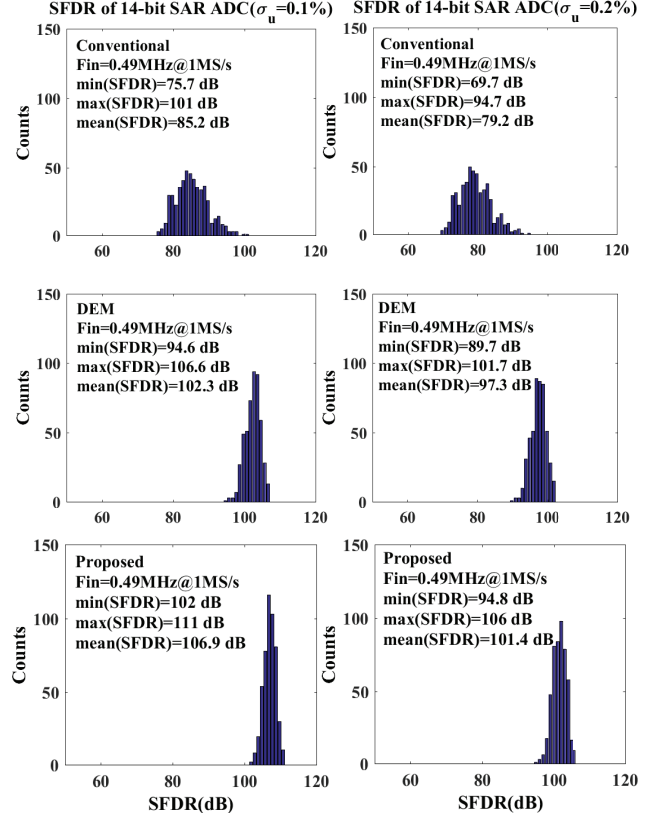
VII. ACKNOWLEDGMENTS

Fig. 8. 500 Monte Carlo SFDR simulation results for 14-bit SAR ADC with respectively Conventional, DEM and Proposed with σ_u=0.3% (left) and σ_u=0.4% (right)
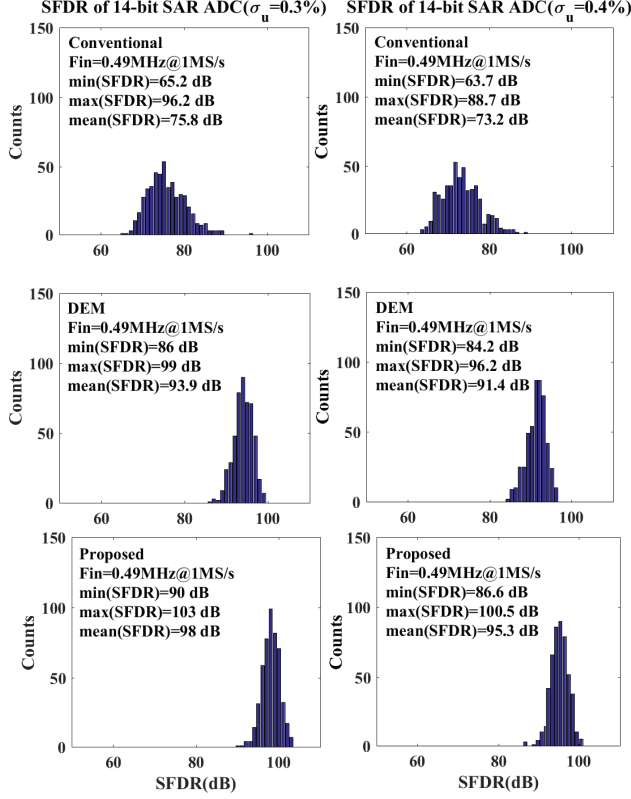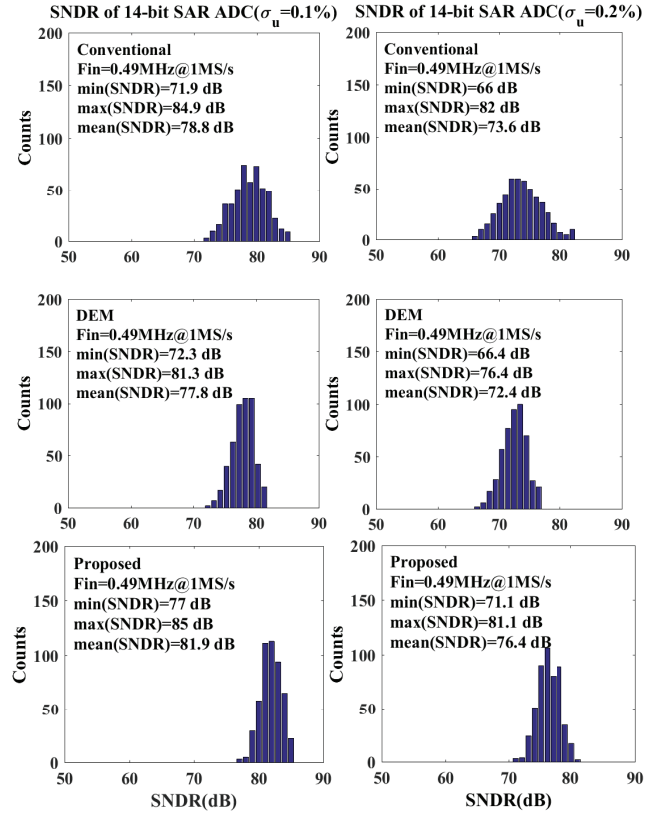

Fig. 9. 500 Monte Carlo SNDR simulation results for 14-bit SAR ADC with respectively Conventional, DEM and Proposed with σ_u=0.1% (left) and σ_u=0.2% (right)

REFERENCES

[1] M. Melzer, J. I. Mönch, D. Makarov, Y. Zabila, G. S. Cañón Bermúdez, D. Karnaushenko, S. Baunack, F. Bahr, C. Yan, M. Kaltenbrunner et al., "Wearable magnetic field sensors for flexible electronics," Advanced Materials, vol. 27, no. 7, pp. 1274–1280, 2015.

[2] D. L. Bellin, H. Sakhtah, J. K. Rosenstein, P. M. Levine, J. Thimot, K. Emmett, L. E. Dietrich, and K. L. Shepard, "Integrated circuit-based electrochemical sensor for spatially resolved detection of redox-active metabolites in biofilms," Nature communications, vol. 5, 2014.

[3] Q. Liang, X. Yan, X. Liao, S. Cao, S. Lu, X. Zheng, and Y. Zhang, "Integrated active sensor system for real time vibration monitoring," Scientific reports, vol. 5, 2015.

[4] S. Xu, Y. Zhang, L. Jia, K. E. Mathewson, K.-I. Jang, J. Kim, H. Fu, X. Huang, P. Chava, R. Wang et al., "Soft microfluidic assemblies of sensors, circuits, and radios for the skin," Science, vol. 344, no. 6179, pp. 70–74, 2014.

[5] W. Wu, L. Wang, Y. Li, F. Zhang, L. Lin, S. Niu, D. Chenet, X. Zhang, Y. Hao, T. F. Heinz et al., "Piezoelectricity of single-atomic-layer MoS2 for energy conversion and piezotronics," Nature, vol. 514, no. 7523, pp. 470–474, 2014.

[6] S.-K. Kang, R. K. Murphy, S.-W. Hwang, S. M. Lee, D. V. Harburg, N. A. Krueger, J. Shin, P. Gamble, H. Cheng, S. Yu et al., "Bioresorbable silicon electronic sensors for the brain," Nature, vol. 530, no. 7588, pp. 71–76, 2016.

[7] A. J. Bandodkar and J. Wang, "Non-invasive wearable electrochemical sensors: a review," Trends in biotechnology, vol. 32, no. 7, pp. 363–371, 2014.

[8] W. Gao, S. Emaminejad, H. Y. Y. Nyein, S. Challa, K. Chen, A. Peck, H. M. Fahad, H. Ota, H. Shiraki, D. Kiriya et al., "Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis," Nature, vol. 529, no. 7587, pp. 509–514, 2016.

[9] A. P. Selvam, S. Muthukumar, V. Kamakoti, and S. Prasad, "A wearable biochemical sensor for monitoring alcohol consumption lifestyle through Ethyl glucuronide (EtG) detection in human sweat," Scientific reports, vol. 6, 2016.

[10] B. Kaliannan and V. S. R. Pasupureddi, "A low power charge mode compressive acquisition of multichannel eeg signals," in Circuits and Systems (ISCAS), 2016 IEEE International Symposium on. IEEE, 2016, pp. 518–521.

[11] F. Maloberti and P. Malcovati, "Microsystems and smart sensor interfaces: a review," Analog Integrated Circuits and Signal Processing, vol. 15, no. 1, pp. 9–26, 1998.

[12] P. Ciccarella, M. Carminati, G. Ferrari, D. Bianchi, S. Grillanda, F. Morichetti, A. Melloni, and M. Sampietro, "Impedance-sensing cmos chip for noninvasive light detection in integrated photonics," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 63, no. 10, pp. 929–933, 2016.

[13] ADI, "Low power, five electrode electrocardiogram (ECG) analog front end," ANALOG DEVICES ADAS1000 DATASHEET, 2012.

[14] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultralow-power electronics for biomedical applications," Biomedical Engineering, vol. 10, pp. 247–274, 2008.

[15] Z. Chen, Y. Jiang, C. Cai, H.-G. Wei, S.-W. Sin, U. Seng-Pan, Z. Wang, and R. P. Martins, "A 22.4 μW 80dB SNDR $\Sigma\Delta$ modulator with passive analog adder and SAR quantizer for EMG application," in IEEE Asian Solid State Circuits Conference (A-SSCC), 2012, pp. 257–260.

[16] H. Liu, Q. Zhou, J. Yang, T. Jiang, Z. Liu, and J. Li, "Intelligent lumi-

SNDR of 14-bit SAR ADC(σ_u=0.3%) **SNDR of 14-bit SAR ADC(σ_u=0.4%)**

Conventional
Fin=0.49MHz@1MS/s
min(SNDR)=61.8 dB
max(SNDR)=82.8 dB
mean(SNDR)=70.4 dB

Conventional
Fin=0.49MHz@1MS/s
min(SNDR)=60 dB
max(SNDR)=78 dB
mean(SNDR)=67.9 dB

DEM
Fin=0.49MHz@1MS/s
min(SNDR)=62.3 dB
max(SNDR)=73.3 dB
mean(SNDR)=69.1 dB

DEM
Fin=0.49MHz@1MS/s
min(SNDR)=60.3 dB
max(SNDR)=71.3 dB
mean(SNDR)=66.5 dB

Proposed
Fin=0.49MHz@1MS/s
min(SNDR)=67.1 dB
max(SNDR)=78.1 dB
mean(SNDR)=73.1 dB

Proposed
Fin=0.49MHz@1MS/s
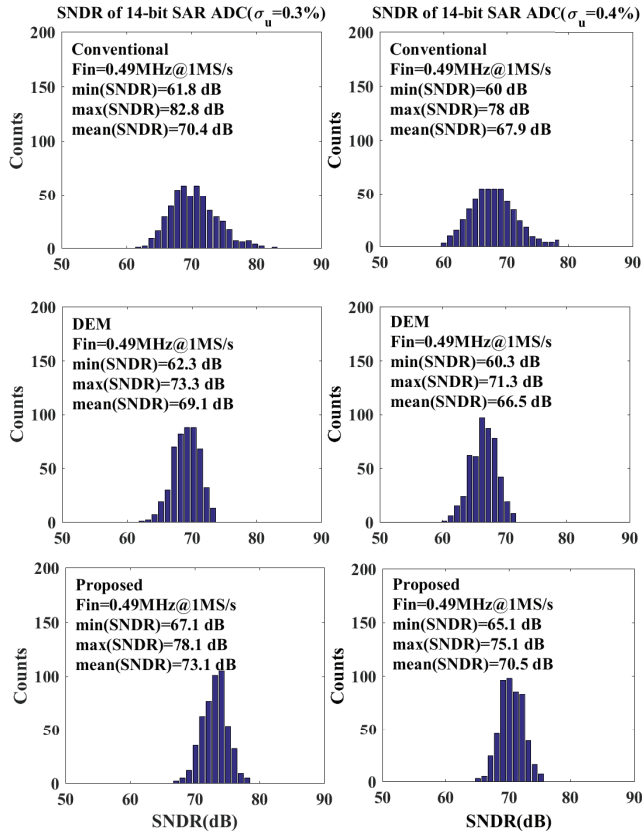min(SNDR)=65.1 dB
max(SNDR)=75.1 dB
mean(SNDR)=70.5 dB

Fig. 10. 500 Monte Carlo SNDR simulation results for 14-bit SAR ADC with respectively Conventional, DEM and Proposed with σ_u=0.3% (left) and σ_u=0.4% (right)

nance control of lighting systems based on imaging sensor feedback," *Sensors*, vol. 17, no. 2, p. 321, 2017.

[17] B. Zhao, N.-C. Kuo, and A. M. Niknejad, "An inductive-coupling blocker rejection technique for miniature rfid tag," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 8, pp. 1305–1315, 2016.

[18] M. Liu, A. van Roermund, and P. Harpe, "A 7.1 fJ/conv.-step 88dB-SFDR 12b SAR ADC with energy-efficient swap-to-reset," in *European Solid-State Circuits Conference, ESSCIRC Conference 2016: 42nd*. IEEE, 2016, pp. 409–412.

[19] M. Kim, U. Ha, Y. Lee, K. Lee, and H.-J. Yoo, "A 82nW chaotic-map true random number generator based on sub-ranging SAR ADC," in *European Solid-State Circuits Conference, ESSCIRC Conference 2016: 42nd*. IEEE, 2016, pp. 157–160.

[20] M. Carminati, G. Ferrari, and M. Sampietro, "Emerging miniaturized technologies for airborne particulate matter pervasive monitoring," *Measurement*, 2015.

[21] Y. Kobiyama, Q. Zhao, and K. Omomo, "Privacy preserving infrared sensor array based indoor location awareness," in *Systems, Man, and Cybernetics (SMC), 2016 IEEE International Conference on*. IEEE, 2016, pp. 001 353–001 358.

[22] M. Ortner, "Improving magnetic linear position measurement by field shaping," in *Sensing Technology (ICST), 2015 9th International Conference on*. IEEE, 2015, pp. 359–364.

[23] B. P. Reddy and A. Murali, "SoC FPGA-based field oriented control of BLDC motor using low resolution Hall sensor," in *Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE*. IEEE, 2016, pp. 2941–2945.

[24] M. Chaudhari and S. Dharavath, "Study of smart sensors and their

applications," *International Journal of Advanced Research in Computer and Communication Engineering*, vol. 3, no. 1, pp. 5031–5034, 2014.

[25] S. Fateh, P. Schönle, L. Bettini, G. Rovere, L. Benini, and Q. Huang, "A reconfigurable 5-to-14 bit sar adc for battery-powered medical instrumentation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 11, pp. 2685–2694, 2015.

[26] Wang, Z. and Lin, R. and Gordon, E. and Lakdawala, H. and Carley,L.R. and Jensen, J.C., "An in-situ temperature-sensing interface based on a SAR ADC in 45nm LP digital CMOS for the frequency-temperature compensation of crystal oscillators," in *Digest of Technical Papers of IEEE International Solid-State Circuits Conference(ISSCC)*, 2010, pp. 316–318.

[27] Z. Wang, "A 45nm cmos temperature sensing interface for crystal frequency temperature compensation," Ph.D. dissertation, Carnegie Mellon University, 2009.

[28] Kuramochi, Y. and Matsuzawa, A. and Kawabata, M., "A 0.027-mm^2 Self-Calibrating Successive Approximation ADC Core in 0.18-μm CMOS," *IEICE Transactions on Fundamentals of Electronics Communications and Computer Sciences*, vol. 92, pp. 360–366, 2009.

[29] H. Khorramabadi, "EE 247 Analysis and Design of VLSI Analog Digital Interface Integrated Circuits lecture notes," *http://inst.eecs.berkeley.edu/ ee247/fa07/lectures.html*, 2009.

[30] M. Taherzadeh-Sani and A. A. Hamoui, "Analysis of dynamic element matching (DEM) in pipelined ADCs," in *IEEE International Symposium on Circuits and Systems*, 2006, pp. 5263–5266.

[31] H. S. Mendonca, J. M. da Silva, and J. S. Matos, "Computing ADC harmonic content from a reduced number of values," in *Proceedings of the 20th IEEE Instrumentation and Measurement Technology Conference*, vol. 2, 2003, pp. 1217–1220.

[32] J.-G. Jo, J. Noh, and C. Yoo, "A 20-MHz bandwidth continuous-time sigma-delta modulator with jitter immunity improved full clock period SCR (FSCR) DAC and high-speed DWA," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2469–2477, 2011.

[33] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 753–762, 1995.

[34] H. Fan *et al.*, "High Resolution and Linearity Enhanced SAR ADC for Wearable Sensing Systems ," in *IEEE Int. Symp. Circuits and Systems (ISCAS)*, vol. XX, 2017.