Phys. Status Solidi A **214,** No. 8, 1600835 (2017) / **DOI** 10.1002/pssa.201600835

physica status solidi a
www.pss-a.com
applications and materials science

Dual barrier InAlN/AlGaN/GaN-on-silicon high-electron-mobility transistors with Pt- and Ni-based gate stacks

Konstantinos Floros*[,1], Xu Li[1], Ivor Guiney[2], Sung-Jin Cho[1], Dilini Hemakumara[1], David J. Wallis[2], Edward Wasige[1], David A. J. Moran[1], Colin J. Humphreys[2], and Iain G. Thayne[1]

[1] School of Engineering, University of Glasgow, Glasgow G12 8LT, United Kingdom
[2] Department of Materials Science & Metallurgy, University of Cambridge, Cambridge CB3 0FS, United Kingdom

Received 31 October 2016, revised 30 June 2017, accepted 1 July 2017
Published online 20 July 2017

Keywords AlGaN, GaN, high electron mobility transistors, InAlN, silicon, transition metals

* Corresponding author: e-mail k.floros.1@research.gla.ac.uk, Phone: +44 141 330 2000

In this work, we report the performance of 3 μm gate length "dual barrier" InAlN/AlGaN/GaN HEMTs on Si substrates with gate–drain contact separations in the range 4–26 μm. Devices with Pt- and Ni-based gates were studied and their leakage characteristics are compared. Maximum drain current I_{DS} of ~1 A mm^{-1}, maximum extrinsic transconductance g_m ~203 mS mm^{-1} and on-resistance R_{on} ~4.07 Ω mm for gate to drain distance L_{GD} = 4 μm were achieved. Nearly ideal sub-threshold swing of ~65.6 mV dec^{-1} was obtained for L_{GD} = 14 μm. The use of Pt-based gate metal stacks led to a two to three orders of magnitude gate leakage current decrease compared to Ni-based gates. The influence of InAlN layer thickness on the transistor transfer characteristics is also discussed.

1 Introduction Wide bandgap GaN-based semiconductors continue to attract interest for high power and frequency electronics applications due to the fundamental properties of these materials including large breakdown field, high electron mobility, and saturation electron velocity in the device channel formed in the widely investigated AlGaN/GaN heterostructure [1–5]. Moving to an InAlN/GaN heterojunction, higher quantum well polarization charges can be induced, which can reduce channel resistance and result in higher HEMT drive currents [6]. In addition, InAlN possesses the widest range of bandgaps in the nitride system which can be beneficial for carrier confinement to the device channel. Furthermore, $In_{0.18}Al_{0.82}N$ can be grown lattice matched to GaN, resulting in reduced wafer strain, improved surface morphology and potentially decreased defect density [7–8]. If AlGaN is inserted as an interlayer, surface morphology can be improved and electron mobility can be increased in InAlN/AlGaN/AlN/GaN structures [9].

Lower gate leakage current and sub-threshold swing can be achieved for these InAlN/AlGaN/AlN/GaN structures compared to devices that use an InAlN/AlN/GaN based structure with similar barrier heights [10]. Barrier layers incorporating InAlN and AlGaN have been utilized in both Ga- and N-polar GaN-based heterojunctions [11–14].

Outstanding performance RF devices have been previously reported using InAlN/AlGaN/AlN/GaN epi-stacks grown on sapphire substrates [15]. The novelty of the work reported here is that for the first time, these dual barrier structures have been incorporated into transistors on a silicon substrate, ultimately targeting power switching applications. The importance of this development is that power switching transistors have many tens of millimeters of gate periphery and so a large diameter, low cost substrate platform is vital to satisfy the needs of next generation high efficiency power electronics applications [16]. It is this requirement that motivates the study of dual barrier devices with layout capable of supporting high voltage operation on a silicon substrate.

2 Experimental

2.1 Device structure and fabrication The layer structure of the InAlN/AlGaN/GaN-on-Si HEMT wafers in this study is depicted in Fig. 1. There is no AlN interlayer

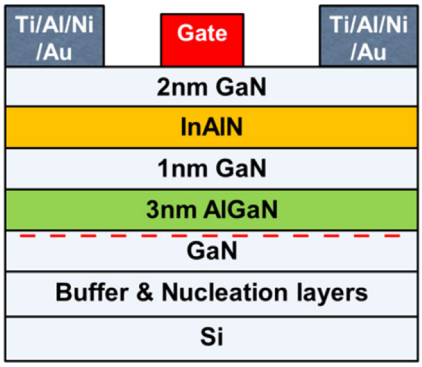

Figure 1 HEMT layer structure. Gate metals used Pt/Au or Ni/Au. InAlN barrier layer thicknesses of 5 and 8 nm were utilized.

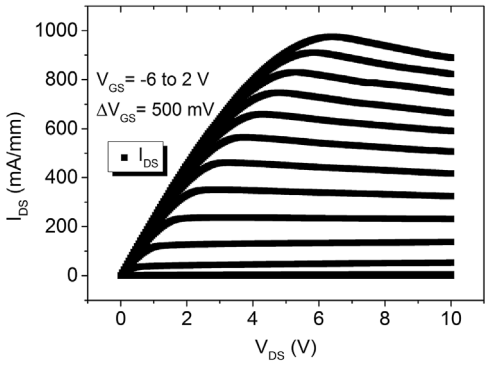

Figure 2 DC output characteristics of 8 nm InAlN/AlGaN/GaN-on-Si HEMT ($W_G = 100\mu m, L_{GS} = 3\ \mu m, L_G = 3\ \mu m, L_{GD} = 4\ \mu m$).

between the AlGaN and GaN layer, so that the surface morphology is not compromised due to the greater lattice mismatch between AlN and GaN. The devices were fabricated on 6″ diameter Si wafer grown by metal organic chemical vapor deposition (MOCVD). From the surface, the layer structure consisted of a 2 nm GaN capping layer, an $In_{0.18}Al_{0.82}N$ barrier layer (both 5 and 8 nm InAlN barrier layers were studied in this work), a 1 nm GaN layer, a 3 nm $Al_{0.25}Ga_{0.75}N$ layer, a 200 nm unintentionally doped (UID) GaN channel, a total of 3.6 μm thick carbon-doped GaN buffer and compositionally graded $Al_xGa_{1-x}N$ transition layer and a 250 nm AlN nucleation layer. The carbon-doped buffer was used to improve the breakdown voltage.

Growth temperature was 1130 °C for AlN, 980 °C for the graded $Al_xGa_{1-x}N$ transition layer, 970 °C for the carbon-doped GaN buffer layer, 1045 °C for GaN channel and capping layers, as well as the $Al_{0.25}Ga_{0.75}N$ layer and 795 °C for the $In_{0.18}Al_{0.82}N$ barrier layer. Average surface roughness R_a of 0.47 nm was measured using atomic force microscopy over a $5 \times 5\ \mu m^2$ scan area.

The device fabrication process started with a ~600 nm mesa etch, patterned using photolithography and defined by reactive ion etching (RIE) in a $SiCl_4$ chemistry. Following this, e-beam evaporated Ti/Al/Ni/Au ohmic contacts of 30/180/40/100 nm thicknesses were lifted-off and then annealed at 770 °C for 30 s in N_2. Then, Schottky gate Pt/Au and Ni/Au contacts of 20/200 nm thicknesses were deposited. The devices have a gate width of 100 μm, a 3 μm gate length, a 3 μm gate to source distance and the gate-to-drain distances range from 4 to 26 μm (large gate–drain separations are required for supporting breakdown voltage of up to 600 V).

2.2 Electrical measurements The electrical transport characteristics of the two wafers were determined at room temperature by Van der Pauw measurements. Channel 2DEG carrier density for the 8 nm InAlN sample was $\sim 1.6 \times 10^{13}\ cm^{-2}$ and Hall mobility μ_H was $\sim 1290\ cm^2\ V^{-1}\ s^{-1}$, resulting in a sheet resistance of $\sim 301\ \Omega\ sq^{-1}$. For the 5 nm InAlN sample, channel 2DEG carrier density was $\sim 1.47 \times 10^{13}\ cm^{-2}$ and Hall mobility μ_H was $\sim 1540\ cm^2\ V^{-1}\ s^{-1}$, resulting in a sheet resistance of $\sim 277\ \Omega\ sq^{-1}$.

The I_{DS}–V_{DS} characteristics of typical fabricated HEMTs with $L_{GD} = 4\ \mu m$ utilizing the 8 nm InAlN barrier layer and Pt/Au based gates are shown in Fig. 2.

Table 1 summarizes key metrics obtained from this device. Contact resistance $R_c = 0.44\ \Omega$ mm was obtained using transfer length method (TLM) measurements. The devices with the shortest source to drain distance $L_{GD} = 4$ μm demonstrate maximum I_{DS} current density of 1 A mm^{-1} and extrinsic transconductance of 203 mS mm^{-1}. Sub-threshold slope of 65.6 mV dec^{-1} was obtained for $L_{GD} = 14\ \mu m$. On-resistance of 4.07 Ω mm was obtained for $L_{GD} = 4\ \mu m$. Threshold voltage was ~−3.4 V (estimated at 1 μA mm^{-1}).

Figure 3 illustrates the role of gate–drain distance on the device transfer characteristics. A 50% reduction in maximum extrinsic transconductance was observed for an increase of drain-to-source spacing from 4 to 26 μm. Drain-to-source off state leakage currents were mostly maintained below 1 μA mm^{-1} (Fig. 4). Gate leakage was the dominant contributor in off-state leakage in both cases.

High work function metals, such as Pt can be used as gate electrodes in order to provide a larger Schottky barrier to reduce gate leakage current. However, Ni is very commonly used due to its stronger adhesion to GaN [17]. The gate leakage characteristics of two typical devices that

Table 1 Device performance metrics for 8 nm InAlN/AlGaN/GaN-on-Si HEMT.

metric	InAlN/AlGaN/GaN-on-Si HEMT
maximum drain current	~1 A mm^{-1}
Hall carrier density	$\sim 1.6 \times 10^{13}\ cm^{-2}$
Hall electron mobility	$\sim 1290\ cm^2\ V^{-1}\ s^{-1}$
sheet resistance	~301 Ω sq^{-1}
contact resistance	~0.44 Ω mm
extrinsic transconductance	~203 mS mm^{-1} ($L_{GD} = 4\ \mu m$)
sub-threshold swing	~65.6 mV dec^{-1} ($L_{GD} = 14\ \mu m$)
on-resistance	~4.07 Ω mm ($L_{GD} = 4\ \mu m$)
threshold voltage	~−3.4 V (L_{GD} = 4–26 μm)

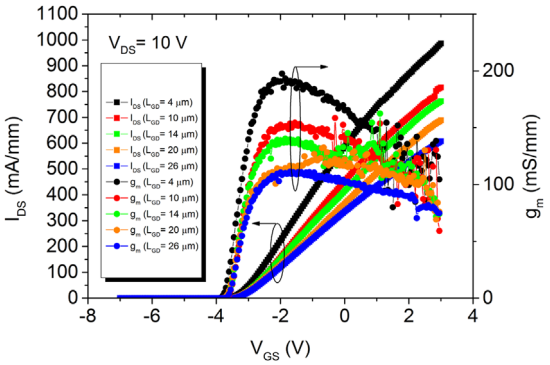

Figure 3 Transfer characteristics for different source-to-drain separations ($W_G = 100\,\mu m$, $L_{GS} = 3\,\mu m$, $L_G = 3\,\mu m$) from 8 nm InAlN/AlGaN/GaN-on-Si HEMT.

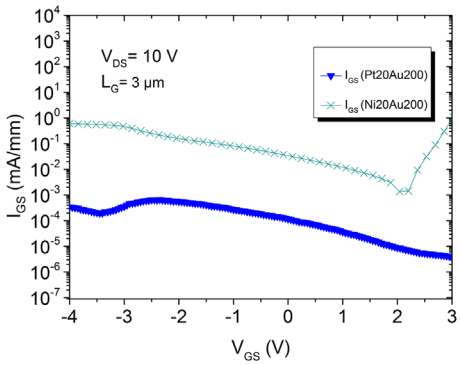

Figure 5 Gate leakage comparison for Pt/Au and Ni/Au gate stacks of 20/200 nm thicknesses ($W_G = 100\,\mu m$, $L_{GS} = 3\,\mu m$, $L_G = 3\,\mu m$, $L_{GD} = 4\,\mu m$).

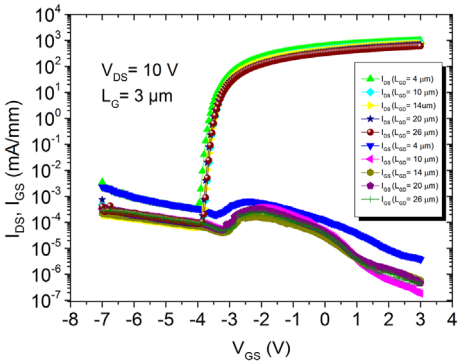

Figure 4 Transfer curves for different source to drain separations in semi-logarithic scale ($W_G = 100\,\mu m$, $L_{GS} = 3\,\mu m$, $L_G = 3\,\mu m$).

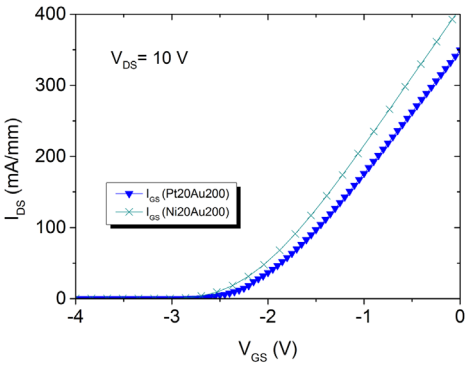

Figure 6 Comparison of transfer curves for Pt/Au and Ni/Au gate metal stacks ($W_G = 100\mu m$, $L_{GS} = 3\,\mu m$, $L_G = 3\,\mu m$, $L_{GD} = 4\,\mu m$).

employed Pt/Au and Ni/Au gates are illustrated in Fig. 5. The Pt-based gates have consistently shown an overall improvement in gate leakage of 2–3 orders of magnitude. It should be noted that no adhesion problems were observed for either the Pt- or Ni-based gates.

The transfer characteristics of devices employing Pt/Au and Ni/Au gates are shown in Fig. 6. The difference of ~0.5 eV in work function between Pt and Ni leads to a larger surface Schottky barrier height and a resulting lower channel 2DEG density under the gate if Pt is used. The device threshold voltage is then positively shifted.

In order to observe the influence of the InAlN layer thickness on the device metrics, the transfer characteristics for HEMTs fabricated on both the 5 and 8 nm InAlN barrier thickness were compared (Fig. 7). These devices employed Ni/Au gates.

Threshold voltage was ~ -3 V for the 8 nm InAlN sample and ~ -1.6 V for 5 nm InAlN. The threshold voltage shift is attributed to the difference in spontaneous polarization and the resulting difference in 2DEG density between the two heterostructures. Similar extrinsic transconductance g_m 203 and 194 mS mm^{-1} for 8 nm InAlN and 5 nm InAlN samples were observed. Given the lower sheet resistance $R_{sh} = 277\,\Omega\,sq^{-1}$ of the 5 nm InAlN wafer compared to $301\,\Omega\,sq^{-1}$ of the 8 nm InAlN wafer, the similar extrinsic transconductance g_m is due to higher

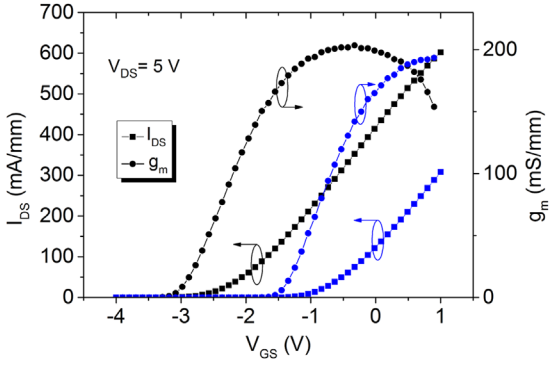

Figure 7 Comparison of transfer characteristics for 8 nm InAlN (black) and 5 nm InAlN (blue). The increased polarization-induced charge for thicker (8 nm) InAlN, results in a more negative threshold voltage ($W_G = 100\,\mu m$, $L_{DS} = 12\,\mu m$, $L_G = 3\,\mu m$).

contact resistance $R_c = 0.95\,\Omega\,\text{mm}$ for 5 nm InAlN compared to $R_c = 0.44\,\Omega\,\text{mm}$ for the 8 nm InAlN wafer.

3 Conclusions In summary, we fabricated InAlN/AlGaN/GaN on Si-based HEMTs and presented their electrical transport and DC performance characteristics. Two different InAlN thicknesses and a range of drain to gate spacing were used. The results obtained suggest that InAlN/AlGaN/GaN on Si-based transistors have the potential to exploit the large band gap and polarization of InAlN for power electronic applications. Gate stacks based on Pt led to a two to three orders of magnitude decrease in gate leakage compared to Ni-based gates.

Acknowledgements This work is supported by the UK EPSRC grant "Silicon Compatible GaN Power Electronics" EP/K014471/1. Fabrication of the devices was carried out at the James Watt Nanofabrication Centre (JWNC).

References

[1] Y.-F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. Denbaars, and U. K. Mishra, IEEE Electron Device Lett. **17**, 455 (1996).
[2] W. Lu, J. Yang, M. A. Khan, and I. Adesida, IEEE Trans. Electron Devices **48**, 581 (2001).
[3] S. Chowdhury and U. K. Mishra, IEEE Trans. Electron Devices **60**, 3060 (2013).
[4] A. Eblabla, X. Li, I. Thayne, D. J. Wallis, I. Guiney, and K. Elgaid, IEEE Electron Device Lett. **36**, 899 (2015).
[5] R. Brown, D. Macfarlane, A. Al-Khalidi, X. Li, G. Ternent, H. Zhou, I. Thayne, and E. Wasige, IEEE Electron Device Lett. **35**, 906 (2014).
[6] J. Kuzmík, IEEE Electron Device Lett. **22**, 510 (2001).
[7] O. Ambacher, R. Dimitrov, M. Stutzmann, B. E. Foutz, M. J. Murphy, J. A. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Chumbes, B. Green, A. J. Sierakowski, W. J. Schaff, and L. F. Eastman, Phys. Status Solidi B **216**, 381 (1999).
[8] K. S. Kim, A. Saxler, P. Kung, M. Razeghi, and K. Y. Lim, Appl. Phys. Lett. **71**, 800 (1997).
[9] M. Hiroki, N. Maeda, and T. Kobayashi, Appl. Phys. Express **1**, 111102 (2008).
[10] M. Hiroki, N. Maeda, and T. Kobayashi, Phys. Status Solidi C **6**, 1 (2009).
[11] J. Lu, Y. L. Hu, D. F. Brown, F. Wu, S. Keller, J. S. Speck, S. P. DenBaars, and U. K. Mishra, Jpn. J. Appl. Phys. **51**, 115502 (2012).
[12] J. Lu, D. Denninghoff, R. Yeluri, S. Lal, G. Gupta, M. Laurent, S. Keller, S. P. Denbaars, and U. K. Mishra, Appl. Phys. Lett. **102**, 232104 (2013).
[13] S. W. Kaun, E. Ahmadi, B. Mazumder, F. Wu, E. C. H. Kyle, P. G. Burke, U. K. Mishra, and J. S. Speck, Semicond. Sci. Technol. **29**, 045011 (2014).
[14] E. Ahmadi, F. Wu, H. Li, S. W. Kaun, M. Tahhan, K. Hestroffer, S. Keller, J. S. Speck, and U. K. Mishra, Semicond. Sci. Technol. **30**, 055012 (2015).
[15] D. Denninghoff, J. Lu, E. Ahmadi, S. Keller, and U. K. Mishra, in: Proc. 71st Device Research Conference (DRC), Notre Dame, IN, USA, 2013 (IEEE, Notre Dame, 2013), pp. 197–198.
[16] B. J. Baliga, Semicond. Sci. Technol. **28**, 074011 (2013).
[17] B. Ofuonye, J. Lee, M. Yan, C. Sun, J.-M. Zuo, and I. Adesida, Semicond. Sci. Technol. **29**, 095005 (2014).

