On-detector Electronics for the LHCb VELO Upgrade

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ABSTRACT: The LHCb Experiment is designed for precision measurements of CP violation and rare decays of beauty and charm hadrons. The experiment will be upgraded to a trigger-less system reading out the full detector at a 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator will be a hybrid pixel detector read out by the VeloPix ASIC with on-chip zero-suppression. The overview of the system and the design of the VELO on-detector electronics that include the front-end hybrid, the opto-conversion and power distribution boards will be summarised. The results from the evaluation of these prototypes and further enhancement techniques will be discussed.

KEYWORDS: Front-end electronics for detector readout; Particle tracking detectors; On-board data handling.

Contents

1. Introduction **1**

2. Front-end hybrid and VeloPix ASICs **3**

3. Data Link Tapes **4**

4. Vacuum Feedthrough **5**

5. Opto Power Board(OPB) **5**

6. Results and Measurements with the Prototype boards **6**

1. Introduction

The Large Hadron Collider beauty (LHCb) Experiment [1][2] is a single arm spectrometer aimed at measuring CP violation and rare decays of beauty and charm hadrons. The Vertex Locator (VELO) [3][4] surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. The upgraded LHCb VELO [5][6] will be installed together with the rest of the upgraded LHCb experiment during the LHC long shutdown (LS2) currently scheduled to start in 2019-2020. The upgraded LHCb VELO will comprise a lightweight hybrid pixel detector with a trigger-less system [7] reading out the full detector at 40 MHz. The luminosity will increase to 2×10^{33} cm^{-2} s^{-1}, which is a factor of five larger than at present. The reconstruction speed and precision of the detector is enhanced by the L-shaped pixel geometry of the modules. The distance from the beam to the first sensitive pixel is decreased to 5.1mm. An illustration of the upgraded VELO highlighting the main components of the on-detector electronics can be seen in Figure 1. The VELO will operate in vacuum and is designed to absorb the VELO motion. Each VELO half is retracted in the horizontal plane and is only closed once stable beam conditions are declared. This is done in order to ensure detector safety during beam injection and adjustments. VELO is operated in secondary vacuum, separated from the beam by a thin foil. This is done to minimise the material traversed by the particles before their first measured point. The system will use evaporative CO_2 cooling, which will circulate in microchannel substrates [8]. The VELO will have 41 million pixels that will be read out by the custom developed VeloPix front-end ASIC [9].

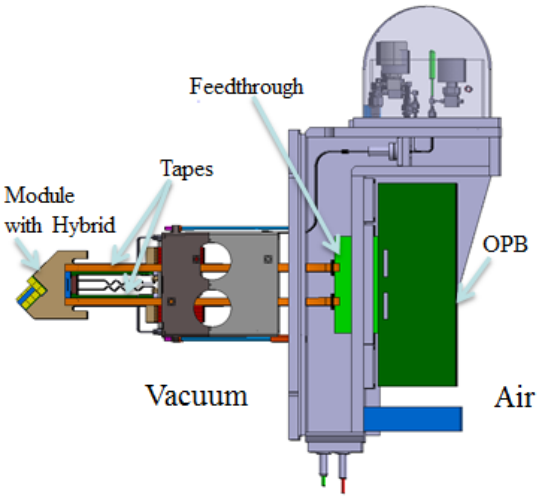


Figure 1: An illustration of the upgraded VELO highlighting the module comprising VeloPix ASIC-sensor assembly and front-end hybrid mounted on the micro-channel cooling substrate, data tapes, vacuum feedthrough and Opto and Power Board (OPB).

The on-detector electronics comprises of the following components-

- Front-end hybrid and VeloPix ASICs
- Data link tape
- Vacuum Feedthrough
- Opto and power board (OPB)

These blocks are shown in the overview of the VELO upgrade electronics in Figure 2.

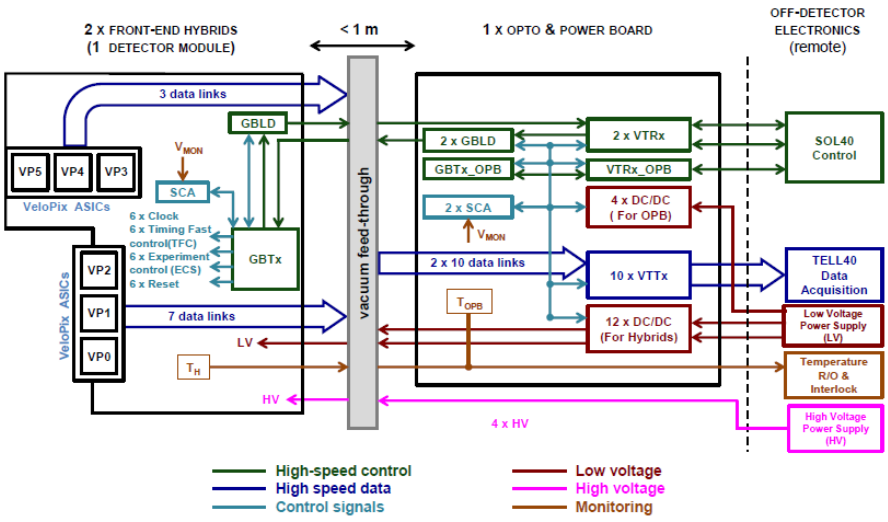


Figure 2: Overview of the VELO Upgrade electronics showing the role and functionality of each block in the system. The colours indicate the type of signals involved.

The optical components in the system such as lasers, diodes, fibres and optical connectors cannot be placed inside the secondary vacuum. This is mainly because of the-

- Difficulty of cooling the high-power dissipating optical components in vacuum.
- Sensitivity to radiation.
- Accessibility of interconnects for maintenance.
- Additional mass in the detector acceptance.

The electronics should also be easily accessible to allow maintenance and repair during operation. For similar reasons stated above, the DC/DC converters powering the front-end ASICs have to be moved into an accessible area outside the vacuum tank.
This motivates the design of the OPB [10] that comprises all parts that need to be outside the vacuum to operate. All the ICs have to be radiation tolerant in addition to its functionality. The local clock for the front-end hybrid as well as the timing, clock and command for the ASICs is handled by the GBTx on the hybrid itself. The serial data and control links are carried over flexible data tapes that extend upto the vacuum wall where they interface to the vacuum feedthrough board.
The design of the on-detector electronics is based on the GBT chip-set [11][12] and the versatile link developed for the LHC upgrades [11] [13].

The paper will describe and focus on the design of these building blocks of the on detector electronics, key features and design constraints. It will also show results of the prototypes tested and further investigations into methods of improving signal transmission.

2. Front-end hybrid and VeloPix ASICs

The front-end hybrid is mounted on the VELO detector module. There are in all 52 modules, 26 on each side of the beam. Each silicon sensor is bump-bonded to a row of three VeloPix ASICs, the assembly of which forms a tile. Each module is made up of 4 such tiles, 2 on each side of the microchannel cooling substrate. The VeloPix ASIC is based on the Timepix3 ASIC and is designed in the TSMC 130 nm CMOS process .The ASIC has data driven read-out with on chip zero suppression. It has four serial outputs, each transmitting data at 5.12 Gb/s. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the full VELO [9].
The hybrid will provide power, high voltage, control signal distribution and read-out signal routing to the tiles.
The prototype hybrid is designed as a split design with control electronics separated from the read-out ASICs as shown in Figure 3. This allows evaluation of multiple instances of the part that contains the VeloPix ASIC and sensors while reusing the same control components. The GBTx is used to implement multipurpose high speed bidirectional optical links and the Slow Control Adaptor (SCA) for voltage monitoring. The SCA chip will not be present on the production hybrid since the monitored supply voltages (from the VeloPix ASIC) will be routed out to the OPB. The GBLD (radiation tolerant laser driver ASIC with pre-emphasis) is used as a line driver to route the control signals from the hybrid to the VTRx (versatile link transceiver) on the OPB.

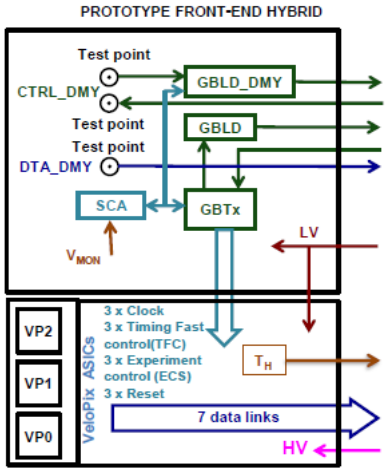


Figure 3: The block diagram of the prototype split hybrid with control electronics separated from the read-out ASICs. The GBTx supplies the Timing and fast control (TFC), Clock(CLK), Experiment control system (ECS) and Reset (RST) to the VeloPix ASICs. A dummy control link (CTRL_DMY) to and from the off-detector electronics is established to check the full link between the components of the VELO electronics. Data dummy (DTA_DMY) is a provision to apply a signal on the hybrid and read it at the OPB.

The layout is a 6 layer flexi-rigid board with Isola Itera and Dupont Pyralux AP plus material, both rated for high speed signal transmission. It is a single sided component assembly with dense BGA (ball grid array) packages. Design rules and guidelines for controlled impedance and high speed transmission have been implemented and followed in the PCB layout.

3. Data Link Tapes

The data link are implemented as low mass, 56 cm long electrical tape carrying data at 5.12 Gb/s per link. The tapes route control and data signals between the modules to the vacuum feedthrough. The VELO has 208 tapes for 52 modules with 20 data links per module. The tapes have to be flexible to absorb the motion of the VELO and vacuum compatible. This has been verified by subjecting the tape prototype to 3000 bends and testing the quality of the tape by measuring scattering (S) parameters thereafter.

Prototypes are built with a special laminate, Dupont Pyralux AP PLUS, that is suitable for high speed signal transmission applications. Unlike typical printed circuit boards that are constructed from various woven fiberglass, AP-PLUS is a “weave-free” all-polyimide profile that provides a smoother surface and homogeneous medium for improved signal integrity. The homogeneous dielectric core provides a consistent dielectric constant (Dielectric constant (1MHz -10 GHz) - 3.4) for controlled impedance circuit requirements. The material also provides excellent thickness stability with tolerances of +/- 10%, which minimizes impedance variations of signal lines. The copper foil is rolled-annealed, that provides a smooth surface finish and minimizes the skin effect loss. The layout has 3 layers with signals in an edge coupled stripline environment. A Molex Slimstack connector with a 400 µm pitch is used, which is mounted on the inner layer (of the 3 layer stackup) by removing the top layer dielectric in this region. This avoids vias on the high speed signal traces.

4. Vacuum Feedthrough

The vacuum feedthrough is an interface between the high speed data link tape and the OPB and brings the signals through the vacuum wall. This board will be integrated with the vacuum wall but the first prototype is made as a purely electrical object which is described here. The prototype vacuum feedthrough board is interfaced to the OPB with PCIe connectors that carry the data and the low voltages. The low voltages are provided on a separate connector from that of the data (that run over data tapes) on the front-end hybrid side. These low voltages are distributed on the hybrid by separate cables.

The prototype vacuum feedthrough is a multilayer board with FR4 and Isola Itera. All the high speed data signals, running at 5.12 Gb/s, are routed in an edge coupled stripline environment and shielded with ground planes on either sides. Controlled impedance, matched trace lengths and blind via technology are used to achieve optimal design.

5. Opto Power Board (OPB)

The OPB [10] connects between the vacuum feedthrough and the off-detector electronics and its main functions are-

- Optical to electrical conversion for the data and control signals.
- Control and monitoring of the components on the OPB.
- DC/DC conversion of the supply voltages for the hybrids and OPB itself.

Each OPB will service two front-end hybrids that are attached on opposite sides of the detector module.

The prototype OPB is designed in line with the prototype hybrid capable of reading 3 VeloPix ASICs on one tile. The prototype OPB has full functionality of the production board but with reduced number of channels. This is implemented in order to save prototype components and reduce complexity. The overview of the prototype system and the role of the prototype OPB is shown Figure 4.

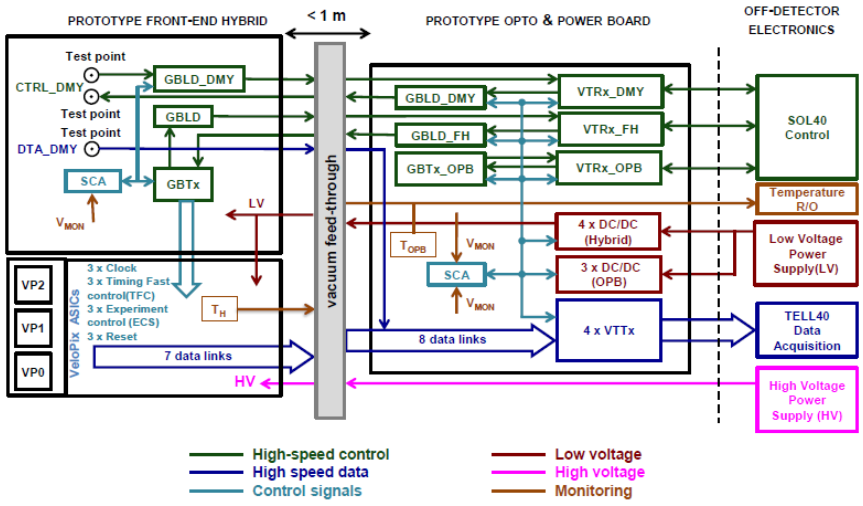


Figure 4: Overview of the prototype system showing the role of the prototype OPB. The main components of the prototype hybrid and OPB are shown. The colours indicate the type of signals involved.

The prototype OPB is designed to test the electrical functionality of the link from the hybrid to the off-detector electronics. The OPB uses the GBTx, the serialiser/deserialiser IC that also provides a clock and control interface. The GBTx communicates with the Slow Control Adaptor (SCA) that provides I2C to configure the GBLD laser driver ASICs and logical I/O signals for the DC-DC converters. The ADC inputs of the SCA ASIC are used for voltage monitoring and monitoring the received optical power. The DC-DC converters supply power to the front-end hybrid and the OPB itself. The VTRx (Versatile Transceiver) and the VTTx (twin transmitters) are optical modules, which provide an optical interface to the system. The VTRx is used for the bidirectional control signals between the hybrid and off detector electronics. The VTTx is used for transmitting data read out by the VeloPix ASIC to the off-detector electronics. The DC-DC converters are radiation and magnetic field tolerant modules that supply the voltages required for the front-end hybrids and the OPB itself. Temperature readout system is used to read the temperature of the hybrid and the OPB.

The prototype is a multilayer board with hybrid construction of FR4 and Isola Itera laminate similar to that of the vacuum feedthrough. High speed data signals are routed as edge coupled stripline with continuous GND planes on either side. Controlled impedance and matched trace length design rules are followed for high speed differential signals.

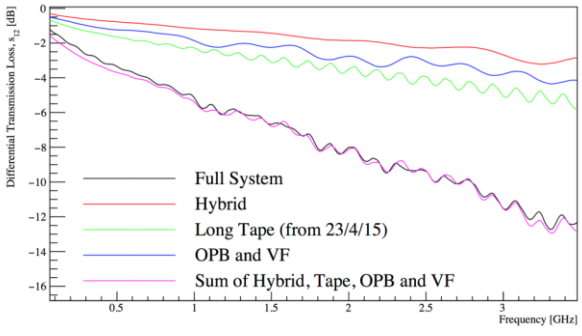
6. Results and Measurements with the prototype boards

A full link setup for testing comprised the front-end hybrid, data tape, vacuum feedthrough and the OPB connected to a 4 port 13GHz network analyser.

The test setup has the front-end hybrid connected to the network analyser using Bulls eye high-density, high-performance test points rated to 20 GHz / 40 Gbps. The hybrid is connected to the 56cm long data tape followed by the vacuum feedthrough and the OPB. The OPB further connects to the network analyser using of the shelf host compliance SFP+ to SMA interface card.

S-parameters describe the response of an N-port network to signal(s) incident to any or all of the ports. The first number in the subscript refers to the responding port, while the second number refers to the incident port. The S-parameters of individual components and full link were measured. A plot of transmission loss S_{12} (dB) verses frequency (GHz) of each component on the link and the complete link is shown in Figure 5.

The full system measures a loss of around 9.4 dB at base harmonic of 2.5 GHz. The figure also shows the eye diagram that was measured using a 5.12 Gb/s pseudo-random 7 bit pattern (PRBS7) for the full link showing an open eye.



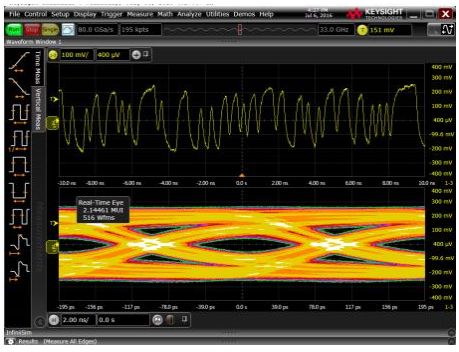


Figure 5: (left) Signal loss as a function of frequency losses for the hybrid (red), data tape (green), and combined vacuum feedthrough and OPB (blue) and the sum of all the component (magenta). This closely overlaps to the full system test (black) (right) The eye diagram of the full system tested using PRBS7 at 5.12 Gb/s.

To improve the eye diagram for the final system, passive CTLE (continuous time linear equalization) circuit is being investigated. The schematic diagram with the optimum values is show in Figure 6. The plot in Figure 6 also shows the improved eye at the receiver when emulating the effects of the CTLE circuit in a real-time oscilloscope. Presently the CTLE circuit has been emulated in the oscilloscope and prototype circuit on printed circuit board (PCB) is in progress.

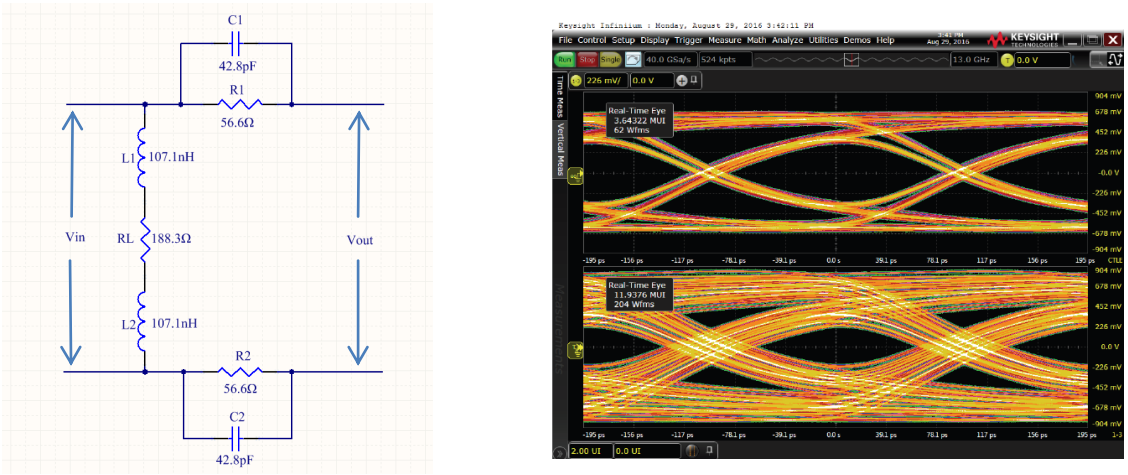


Figure 6: (left) Passive CTLE circuit emulated in the oscilloscope (right) The improvement from the raw eye diagram (bottom) to the one after CTLE emulated by real-time oscilloscope applied at the receiver end (top).

Conclusions

The upgraded VELO electronics will be installed during the LS2 shutdown currently scheduled in 2019-2020. The VELO upgrade will move to a hybrid pixel detector with a trigger-less system capable of reading out the full 40 MHz bunch crossing rate of the LHC. The project is in the final development stages with all the on-detectors electronics prototypes designed and successfully tested. Further studies to improve signal integrity with a passive CTLE are in progress.

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