Compact 1D-silicon photonic crystal electro-optic modulator operating with ultra-low switching voltage and energy

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Abstract: We demonstrate a small foot print (600 nm wide) 1D silicon photonic crystal electro-optic modulator operating with only a 50 mV swing voltage and 0.1 fJ/bit switching energy at GHz speeds, which are the lowest values ever reported for a silicon electro-optic modulator. A 3 dB extinction ratio is demonstrated with an ultra-low 50 mV swing voltage with a total device energy consumption of 42.8 fJ/bit, which is dominated by the state holding energy. The total energy consumption is reduced to 14.65 fJ/bit for a 300 mV swing voltage while still keeping the switching energy at less than 2 fJ/bit. Under optimum voltage conditions, the device operates with a maximum speed of 3 Gbps with 8 dB extinction ratio, which rises to 11 dB for a 1 Gbps modulation speed.

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1. Introduction

Silicon photonics is proving to be a promising future choice of technology for the development of next generation computers designed to meet the continuously growing demand for larger bandwidths and higher data processing speeds, thanks to the significant improvements in the performance of the individual components of a silicon photonic link [1-11]. Low energy consumption is an important requirement for practical optical interconnects [11, 12], and this led to work by different groups aimed at reducing both the losses of passive components and the operating energy of the active components of an optical data link. A promising approach for reducing the energy consumption of an electro-optic (EO) modulator involves using a high Q-factor and ultra-small resonators, e.g. ring resonators [5, 6, 8] and photonic crystal (PhC) cavities [4, 7]. Although the use of high Q-factor resonators limits the bandwidth, this problem can be overcome by employing wavelength division multiplexing (WDM) [7, 10]. Furthermore, new approaches designed to mitigate the thermal sensitivity of cavity-based modulators are emerging [8]. Electro-optic modulators, including cavity modulators, are based on the carrier plasma dispersion effect [13], where carriers are either injected into or removed from the active area. Each approach has its own

advantages and drawbacks. Modulation with the carrier depletion approach has proved to be successful in terms of achieving fast modulation speeds (≈50 Gbps) [8, 9] compared with the carrier injection approach (< 5 Gbps without pre-emphasis) [4–7]. However, one major drawback associated with depletion modulators is that they require a large voltage swing [8, 14–16] to realize a sufficient change in the width of the depletion region for the modulation operation. Conversely, carrier injection modulators can operate with much smaller switching voltages since modulation operation is not dependent on the change of the depletion region width and is instead performed by the external carrier injection and removal process. The need for a larger voltage swing increases the switching energy consumption by the modulator. In addition, after photonic-electronic integration the external energy requirement also increases greatly due to the complex electronic circuitry, the need for amplifiers and a large transient energy [11, 17–19]. With this in mind, efforts have been made to reduce the switching voltage of silicon EO modulators and the most notable demonstration in this regard has been a carrier injection ring resonator modulator operating with a 150 mV swing voltage but still with a high switching energy of 7.9 fJ/bit [6]. In addition to the switching energy, the total energy consumption of these devices is also large, namely of the order of 100 fJ/bit, and there is a need to reduce both the switching and the total energy consumption of the EO modulator. The total energy consumption of a carrier injection electro-optic modulator is made up of two components; switching energy (AC) and holding energy (DC energy). The switching energy depends on the resistance and the capacitance of the device and the required voltage swing, while holding energy is predominantly determined by the resistance of the device. Reducing the footprint of the device lowers the resistance and capacitance values and this can help to reduce the total energy consumption, increase the modulation speed and achieve higher integration density.

In this paper, by using a suitably designed high Q-factor 1D PhC cavity with a small width, we have removed the size and resistance limitation imposed by the 2D nature of the PhC. The combination of a low resistance and capacitance and a high Q-factor enables us to demonstrate a silicon EO modulator operating with a sub-100-mV swing voltage that leads to an ultra-small switching energy at GHz speeds. Furthermore, thanks to the low resistance of the device, the DC energy consumption is also significantly reduced. The device operates with a high extinction ratio (ER) that scales with the applied swing voltage and can achieve ER > 10 dB for 1 Gbps.

2. Design and fabrication

To achieve a low swing voltage operation with a high ER in a silicon EO modulator, it is important to use a cavity design that simultaneously offers good electrical characteristics (low resistance and capacitance) and a high Q-factor. In earlier reports, cavity-based carrier injection silicon EO modulators either had a low Q-factor [6, 20] or very high resistance [4, 7]. A properly designed 1D PhC cavity has the potential to exhibit a high Q-factor along with reduced resistance and capacitance values simultaneously. There are multiple advantages of using a 1D rather than a 2D PhC cavity for modulation operation. First, the device footprint is smaller, which not only helps to achieve a higher integration density but also reduces the capacitance and resistance of the device. Second, we can form the doped regions in silicon simply by creating side slabs, and this allows us to keep the resistance of the device low in contrast to 2D PhC devices where doping is performed in the PhC area. In a 2D PhC theresistance scales with the fill factor of the PhC holes [21].

With these advantages in mind, we based our device on a 1D PhC cavity with the modulated mode gap design [22, 23]. The novelty of the design employed in the present work is the introduction of thin silicon side slabs, which are useful for forming *pin* junctions for injecting current into the cavity. In the present design, the PhC is only 600 nm wide (w) and has a periodicity (a) of 350 nm. The cavity is created by enlarging the radius of the holes, starting from the center, according to a parabolic function $r(i) = r_0\,(1-i^2/m^2)$, where $r_o = 0.3a,$

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and $m = 17$, until it is larger than a nominal value of $0.22a$. Figure 1(a) shows a schematic of the PhC cavity with 50 nm thick side slabs and its mode profile calculated by the 3D FDTD method. This small footprint 1D PhC cavity with 50 nm thick side slabs can achieve a very high theoretical Q-factor of 3.2 x10^6 along with a small mode volume of 0.078 μm^3 making it a suitable candidate to demonstrate a low energy and efficient EO modulator by incorporating a *pin* junction across it. There is a trade-off between the resistance and the Q-factor of the cavity with respect to side slab thickness as the thicker side slabs lower the resistance but also degrade the Q-factor. We estimated that a side slab thickness (z) of 50 nm is a good compromise because it keeps the measured resistance low while maintaining a high Q-factor. To achieve a low EO modal volume we designed a *pin* junction with small physical dimensions, as shown in Fig. 1(b). Thanks to the tightly bound mode, as shown in Fig. 1(a), it is possible to bring the doped fingers very close to the cavity. The *p* and *n* doped areas shown in the red and green respectively are only 1.4 μm apart. We used *pin* junctions instead of *p-n* junction because for later case the doped areas will overlap with the optical mode which increases the optical absorption and reduces the Q-factor.

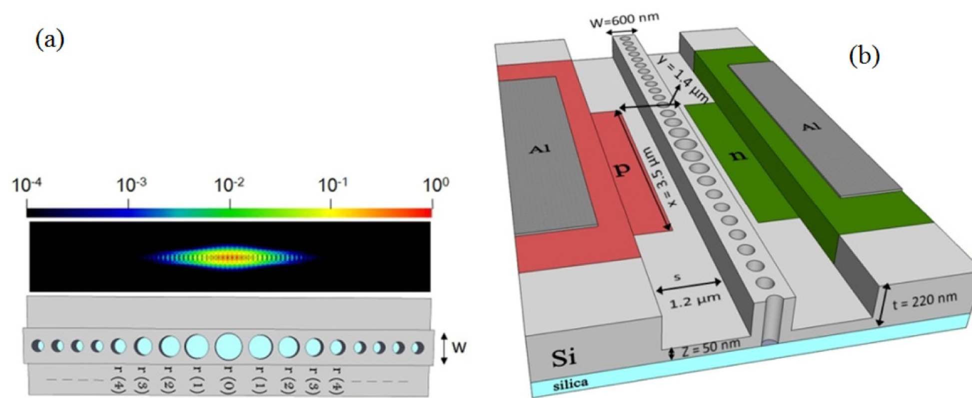

Fig. 1. (a) Schematic of a PhC cavity with 50 nm thick side slabs and 0th order mode profile calculated by 3D FDTD. (b) Schematic of a 1D silicon PhC cavity EO modulator showing the physical dimensions the device.

The device was fabricated by employing multiple photo and e-beam lithography steps and dry etching. The *p* and *n* doped regions were created by boron and phosphorous ion implantation, respectively, each with a final doping density of 5x10^{18}/cm^3. The metal pads were created by an evaporation and lift-off process. Complete details of the fabrication process can be found in our previous reports [4, 22].

3. Spectrum and electrical characteristics

A transverse electric (T.E.) polarized CW laser was used to measure the transmission spectrum of the PhC cavity. The light was butt-coupled to the PhC via a tapered waveguide through fiber objectives. The light collected from the device was fed to a spectrometer to measure the transmission spectrum. The transmission spectrum of one of the devices is shown in Fig. 2(a). With the set of parameters discussed in the design section above, the measured resonance wavelength of the cavity is 1598 nm with a loaded Q-factor of 20 K. The PhC cavity device has only 1.0 dB additional loss compared with the reference silicon waveguide. The coupling and intrinsic Q-factors of the device are estimated to be 22.3 K and 1.9 x10^5, respectively.

The key features of the device are its low resistance and capacitance values. The differential resistance of the device measured from the IV curve is only 900 Ω as shown in Fig. 2(b), thanks to the small width of the 1D PhC cavity with side slabs and the tightly bound mode, which allows the spacing between the doped fingers to be small. This resistance value

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is significantly lower than that of 2D PhC cavities with lateral *pin* junctions [4, 7] where the resistances of 1 M Ω and 100 KΩ were reported. This clearly demonstrates the advantage of using a small width 1D PhC cavity rather than a 2D PhC cavity for EO modulation.

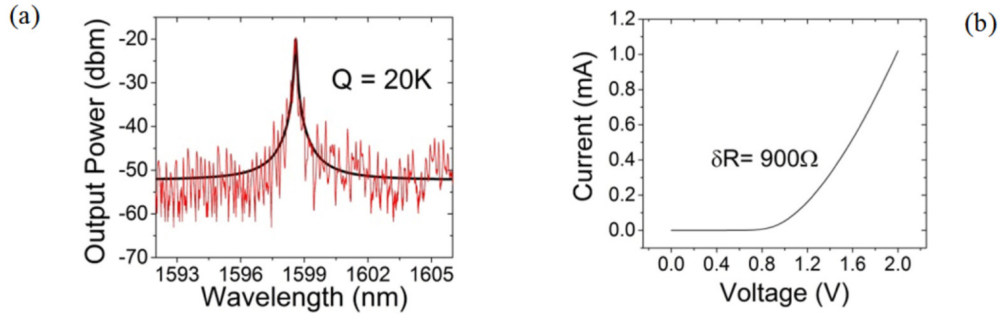

Fig. 2. (a) Transmission spectrum of the PhC cavity showing a 20K Q-factor. (b) IV curve of the device showing 900 Ω differential resistance.

Similarly, due to the small physical dimensions of the cavity and the doped fingers, the capacitance of the device calculated numerically by Comsol Multiphysics is low, as shown in Figs. 3(a) and 3(b) . For very small physical dimensions, the parallel plate model for calculating the capacitance is not accurate because the fringe capacitance contribution becomes dominant and hence it is important to include the effects of the fringing fields.

We estimated the capacitance numerically by considering a 3D model of the real device structure that includes the contribution from the fringing field, as shown in Fig. 3(b).

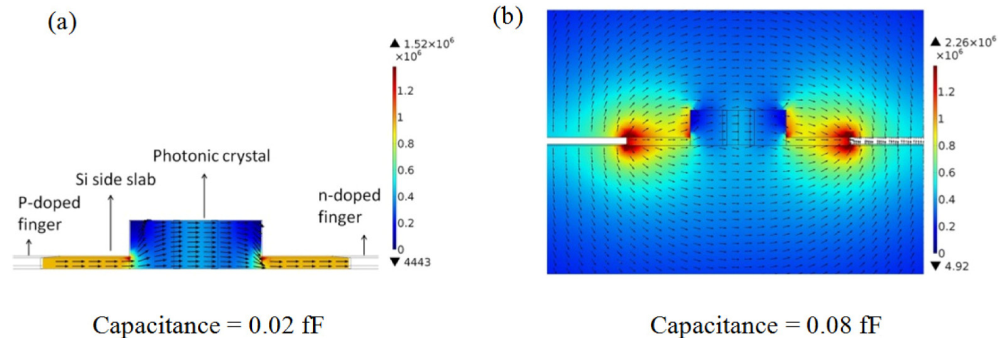

Fig. 3. Numerical estimation of device capacitance. Color plot gives the electric field strength and black arrows show the electric field lines. Without fringing fields the capacitance is 0.02 fF (a) and it increases to 0.08 fF when the fringing fields are included (b).

Considering only the top 220-nm-thick silicon slab and only doped fingers as the electrodes (no metal pads), the capacitance of the device is estimated to be only 0.08 fF, of which 0.06 fF is fringe capacitance. On the other hand, when the full device is considered (220-nm-thick top slab with a 2 µm buried oxide and a thick silicon substrate) with 125 x 125 μm^2 metal pads and doped fingers as electrodes, the total capacitance of the device is estimated to be 15.5 fF, which is dominated by the pad capacitance, thereby highly dependent on the pad size. The pad capacitance increases substantially when a buried oxide layer and a silicon substrate are included in the model. The capacitance increases as the thickness of the silicon substrate increases up to 150 µm. Further increases in the silicon substrate thickness do not increase the pad capacitance due to the weak electric field in the region beyond 150 µm thickness.

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4. Electro-optic response

First, we measured the EO response for carrier injection using only a DC source. The carriers were injected via aluminum (Al) metal pads by using an electrical probe. No significant change was observed in the resonance wavelength until 0.9 V while a small blue shift (around 30 pm) was observed for 1.0 V. Further voltage increases did not result in any further blue shift of the resonance owing to the counteracting thermal response. The observed change in the resonance peak is the net shift resulting from the counteracting plasma dispersion and thermal response.

For the AC EO response, a rectangular 2^7-1 NRZ PRBS signal from a pulse pattern generator (PPG) was applied to the metal pads with a DC bias via a bias tee. A probe terminating with a 50 Ω resistance was used to supply the electrical signal. A probe with a 50 Ω termination was used for two reasons, namely to realize impedance matching with the signal generator and thus eliminate the signal back reflections and to correctly estimate the voltage drop across the pads (by matching with the resistance of oscilloscope used for observing the input signal). Different performance parameters related to the EO modulation of the device are discussed below.

4.1 Swing voltage dependence

A schematic of the input electrical signal showing the definitions of different voltage terms is shown in Fig. 4(c). For a modulation speed of 1 Gbps, a V_{top} value of at least 1.0 V was needed to observe clean open eye diagrams. Keeping V_{top} fixed at 1.0 V by adjusting the DC bias level, we tuned the V_{pp} voltage from 30 to 400 mV.

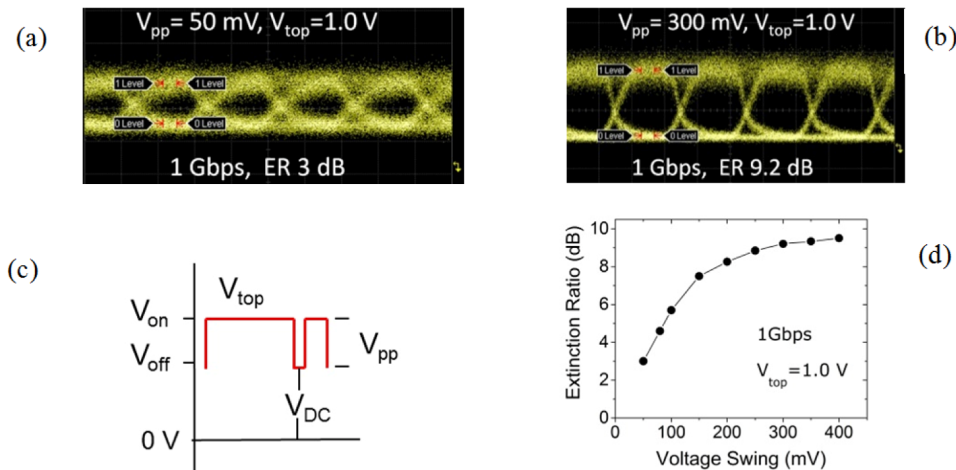

Fig. 4. Eye diagrams for 1 Gbps obtained with swing voltages of (a) 50 mV and (b) 300 mV showing ERs of 3 dB and 9.2 dB, respectively. (c) Schematic of the input electrical signal. (d) ER vs swing voltage for 1 Gbps modulation speed.

The device exhibited modulation at 1 Gbps for a swing voltage of as low as 50 mV with a 3 dB ER as shown in Fig. 4(a). This is the first ever demonstration of a silicon EO optic modulator operating with a sub-100-mV swing voltage. It was not possible to obtain eye diagrams for input swing voltages of less than 50 mV due to the poor signal-to-noise ratio. The ER increases significantly by increasing swing voltage until 200 mV, where an ER of 8.3 dB is achieved. Further increases in the swing voltage do not increase the ER significantly and the value saturates at 9.2 dB for V_{pp} = 300 mV as shown in Figs. 4(b) and 4(d).

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4.2 Operation bandwidth

The operation bandwidth of the device was obtained by measuring the small signal frequency response. The response was measured in the 10 MHz to 10 GHz frequency range with a 6 dBm input RF power and a 0.9 V DC bias. The input laser wavelength was matched to the resonance wavelength of the cavity. A modulated optical signal collected from the device and amplified by EDFA was fed to a network analyzer that converted the optical signal to an electrical with an inbuilt detector. The measured frequency response is shown in Fig. 5 and exhibits a 3 dB bandwidth of 1.3 GHz.

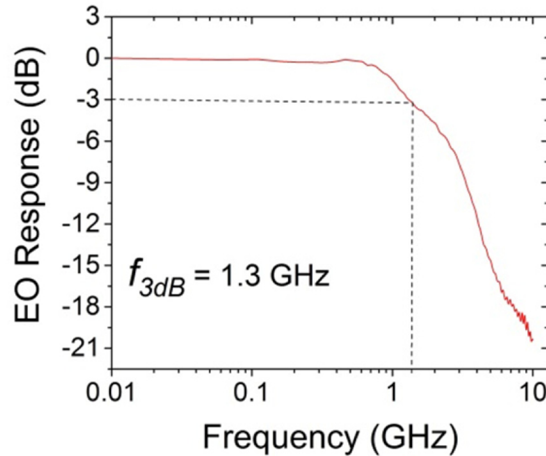

Fig. 5. Small signal frequency response of the device showing a 3 dB bandwidth of 1.3 GHz.

The 3 dB bandwidth and data rates of cavity based carrier injection EO modulators is significantly lower compared to that of MZI modulators [9]. This drawback can be overcome by using WDM. New intelligent techniques to achieve efficient WDM systems for enhancing data rates are coming forward [7].

4.3 Maximum modulation speed and extinction ratio

As mentioned in section 4.1, the ER for V_{top} = 1.0 V saturates at 9.2 dB for a swing voltage of 300 mV at 1 Gbps but these voltage conditions are not the optimum conditions for achieving the highest modulation speed and ER with the device under test.

By tuning different voltage conditions we found out that a combination of V_{top} = 1.1 V with V_{pp} = 500 mV exhibits a speed of 3 Gbps with an ER of 8 dB, as shown in Fig. 6(a), which is the maximum speed achieved by our device with a high ER. The eye diagram closes at 3.5 Gbps, as shown in Fig. 6(b). The ER for same voltage conditions increases to 11 dB for 1 Gbps, as shown in Figs. 6 (c) and 6(d).

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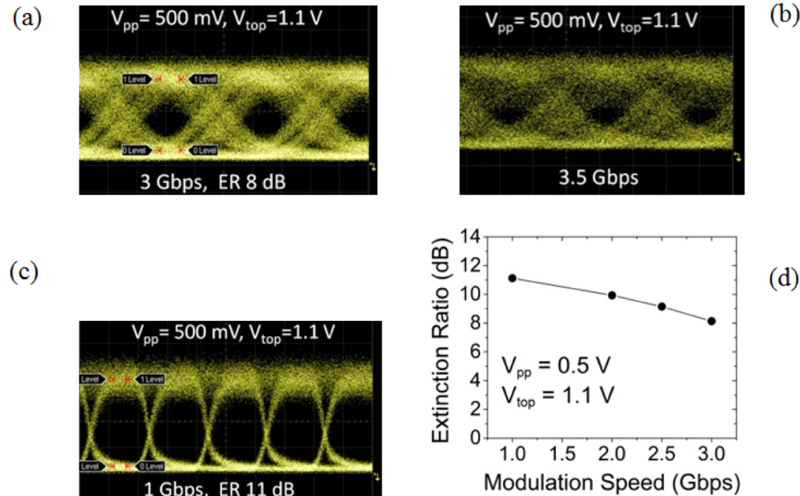

Fig. 6. (a-c) Eye diagrams for optimum input voltage conditions to achieve maximum modulation speed and ER. A maximum modulation speed of 3 Gbps with 8 dB ER (a) while 11 dB ER is demonstrated for 1 Gbps (c). (d) Modulation speed vs ER.

5. Analysis

5.1 Speed limitation

Factors that can limit the 3 dB bandwidth and modulation speed of an EO modulator are the photon lifetime in the cavity ($\tau = \lambda Q/2\pi c$), the RC time constant ($2\pi RC$) and the carrier lifetime. The loaded Q-factor of the cavity used for the modulation operation is 20 K, which corresponds to a photon lifetime of 17 ps and hence a 59 GHz bandwidth should be allowed. Similarly, the RC time constant limited bandwidth is 11.4 GHz (calculated for R = 900 Ω, C = 15.5 fF). When we take account of both these limitations, the 3 dB bandwidth should be 11.2 GHz, which is higher than the experimentally measured value of 1.3 GHz. Thus, by virtue of the improved electrical characteristics, the speed of the device is not limited by the RC time constant.

To investigate the speed limitation factor, we carried out measurements to determine the fall time (90-10% of optical power) and the rise time (10-90%) of a modulated optical signal. An optical signal modulated by a 1 ns wide rectangular electrical pulse with V_{pp} = 500 mV and V_{top} = 1.1 V is shown in Fig. 7. A CW laser light with a wavelength equal to the resonance peak of the cavity was coupled to the device. When the pulse is on (V_{on}), the injection of carriers blue shifts the resonance peak of the cavity as a result of the plasma dispersion effect, which reduces the transmission level. The removal of carriers rematches the cavity resonance to the input wavelength. Hence, the injection of carriers corresponds to the fall time while the removal of carriers corresponds to the rise time of the modulated optical signal.

The measured fall and rise times of the modulated optical signal are around 400 and 300 ps, respectively. From these values, it is evident that for given voltage conditions, the carrier injection process is slower than the carrier removal. The input signal does not have a reverse bias portion for sweeping out the carriers, and hence the carriers are removed by diffusion followed by non-radiative surface recombination process at the hole sidewalls [24, 25]. Although the carrier removal time varies from sample to sample as non-radiative surface recombination also depends on the physical damage caused by the etching process, it is usually reported to be in the region of a few hundred picoseconds [24, 25], which is consistent with the rise time measured for the current device.

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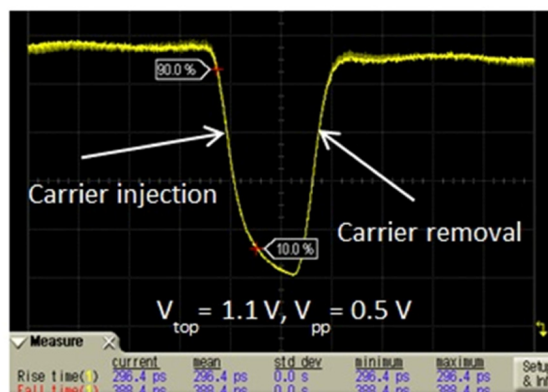

Fig. 7. Modulated optical signal showing fall and rise times of 388 and 296 ps, respectively.

The fall time can be reduced by increasing V_{top} but a larger voltage also induces the detrimental thermal effect, which red shifts the resonance wavelength. The red shift of the resonance wavelength spoils the modulation response because on carrier removal the initial on-state optical power level is not reached. For our device, we experimentally observed this effect for V_{top} values of greater than 1.1 V. Thus, for the present device, the maximum on-state voltage can only be 1.1 V. In addition to this dynamic thermal effect a static thermal effect due to device or ambient temperature changes also exists. For practical applications it would be necessary to tune the resonance wavelength by integrating tuning heaters as is done in ring-resonator-based modulators [26]. Integrating tuning heaters with PhC can be complicated but is possible by a proper design. We believe that tuning power would be eventually lower than that of ring resonator because of small size of PhC cavity.

Keeping V_{top} fixed at 1.1 V, we next measured the modulation response for different off-state voltages (V_{off}) and hence different voltage swings. The optical signals modulated by a 10 ns wide rectangular electrical pulse with different swing voltages are shown in Figs. 8(a) and 8(b). Different responses are observed for the V_{pp} ranges 0.05 V- 0.3 V and 0.3 V-1.9 V. In the 0.05 V-0.3 V range, both the fall and rise times decrease with an increase in voltage swing (smaller V_{off}) as shown in Figs. 8 (a)-8(c). On the other hand, in the V_{pp} range of 0.3 V-1.9 V the fall time increases considerably for larger swing voltages, as shown in Fig. 8(a) and 8(c) (square) while rise time is less dependent on the swing voltage, as shown in Fig. 8(b) and 8(c) (circles). Even with a negative off-state voltage (V_{pp}> 1.1 V), which is usually used for faster carrier extraction, the rise time is reduced only slightly. The modulation depth stays almost constant as the swing voltage is reduced to 0.3 V. Further reduction of the swing voltage reduces the modulation depth substantially, which is consistent with the ER values measured from the eye diagrams and shown in Fig. 4(d).

From Fig. 8, it can be concluded that it is indeed the carrier injection process that limits the modulation speed of the device under test for the voltage conditions used, except for a 300 mV swing voltage, where the rise and fall times are almost the same. Higher speeds can be achieved by using larger swing voltages where the rise time is minimum, provided the fall time (carrier injection) can also be made faster.

The carrier injection process can be made faster by reducing the intrinsic region width. Thanks to the small width and tightly bound mode of our cavity, there is a possibility of further reducing the intrinsic region width by reducing the gap between the *p* and *n* regions. A smaller intrinsic region will increase the electric field strength in the region, which will in turn increase carrier acceleration and also reduce the carrier transit distance. Both effects contribute to making the carrier injection process faster. An improvement in modulation speed by reducing the intrinsic region width through the use of a comb-shaped doping profile

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is reported in [27]. Furthermore, reducing the gap between *p* and *n* regions will further improve the performance of the device by reducing the resistance.

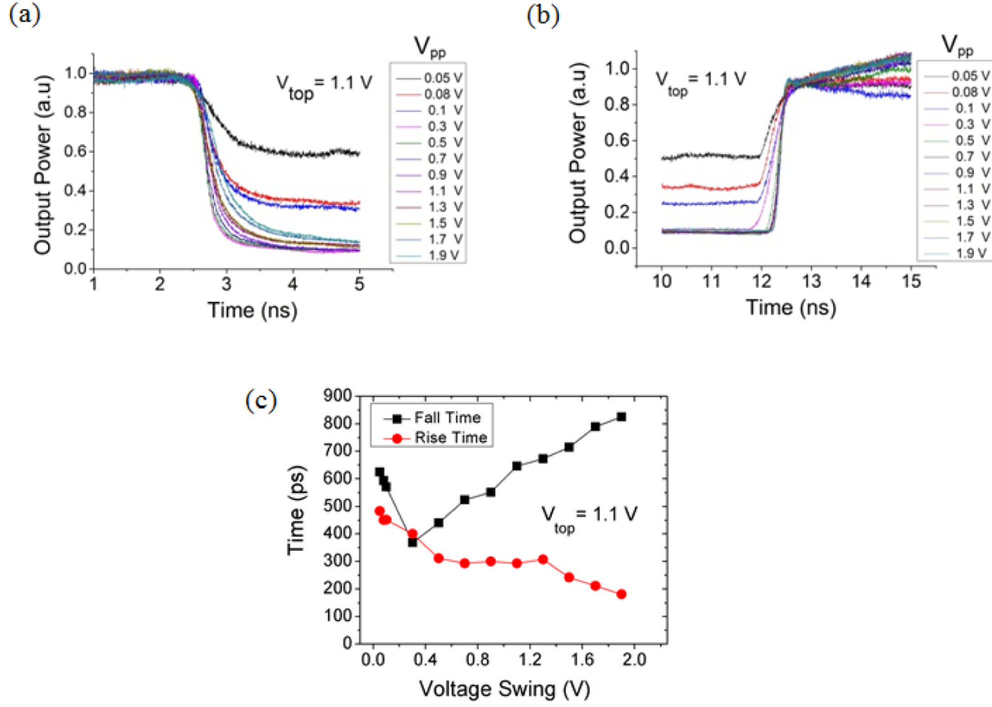

Fig. 8. Fall times (a) and rise times (b) of modulated optical signal for different swing voltages while keeping V_{top} fixed at 1.1 V. (c) Comparison of fall times and rise times for different swing voltages at fixed V_{top}.

5.2 Energy consumption

The energy consumption by carrier injection EO modulators has two components; switching energy (AC) and holding energy (DC). Reducing the switching energy consumption by an EO modulator is important especially to simplify the drive circuitry and reduce the external energy consumption. For this reason, the switching energy requirement of an EO modulator is often discussed and estimated separately and lots of efforts have been done to reduce it [5-7].The switching energy can be estimated from the product of charge required to achieve switching and the applied swing voltage [6], as given by Eq. (1).

$$E_S = \frac{1}{4} Q_c V_{pp} \tag{1}$$

The amount of charge (Q_c) required for switching can be estimated by two methods; (a) By taking the product of current required for switching and the switching time as given by Eq. (2), which gives the upper limit of the charge. (b) From the silicon plasma dispersion equation [13], which is the method followed in [5–7].

$$Q_c = \left(I_{on} - I_{off}\right)\tau \tag{2}$$

In method (a), using experimental values of injected current and fall times given in Fig. 2(b) and 8(c) respectively in Eq. (2), the charge is estimated to be 10.4 fC for a 50 mV swing voltage. This gives a switching energy consumption of only 0.13 fJ/bit. The switching energy increases with the applied voltage swing and is plotted in Fig. 9(a).

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In method (b) the estimation of amount of charge required to achieve switching is highly dependent on the wavelength shift used for the calculation. As counteracting plasma dispersion and thermal effects occur simultaneously, it is difficult to determine the value of the wavelength shift responsible for the measured modulation response accurately. For this reason, a more realistic approach is to estimate the switching energy corresponding to the wavelength shift by using the full width at half maximum (FWHM) of the cavity line. Thus, although experimentally we observed a 30 pm blue shift of the resonance wavelength for V_{top} = 1.0 V, which would lead to a very small switching energy value, in this study we estimate the switching energy by considering the wavelength shift by the FWHM (80 pm). Another important factor for the correct estimation of the switching energy is the carrier - optical mode overlap factor (Γ). Assuming carrier spread into the whole thickness of the PhC (220 nm) and lateral spread only equal to the lateral length of the doped finger (3.5 μm), the estimated value of Γ in our device is 0.64. Using Γ = 0.64, the wavelength shift by 80 pm corresponds to a refractive index change of $2.736e^{-4}$, which corresponds to an injected charge density of $5.9e^{16}/cm^3$. Thanks to a small intrinsic region volume of our device (0.6 μm^3) the total injected charge is only 5.67 fC. For a 50 mV applied swing voltage showing modulation with a 3 dB ER, which is the case shown in Fig. 4(a), our device thus operates with a switching energy of only 0.07 fJ/bit. Note that here we assumed a hypothetical carrier spread profile, and if the realistic carrier spread deviates from the assumed profile, the switching energy will increase. Therefore, 0.07 fJ/bit is the lower limit of the switching energy.

As discussed above, the switching energy estimated by method (a) and (b) gives the upper and lower limits of the switching energy respectively. The switching energy consumption by our device is therefore in the range of 0.07 fJ/bit to 0.13 fJ/bit. This switching energy value is one to two orders of magnitude lower than that in earlier reports on silicon EO modulators, where the switching energy is reported to be 7.9 fJ/bit [6] and 0.4 fJ/bit (but calculated for Γ = and Δλ < FWHM) [7].

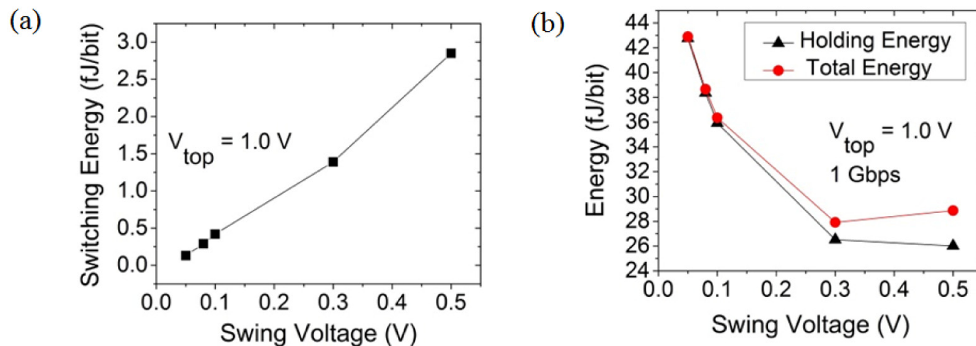

Fig. 9. (a) Switching energy as a function of swing voltage estimated by method (a). (b) Holding and total energy consumption as a function of swing voltage. The switching energy contribution in the total energy is estimated by using method (a).

The holding energy for modulation with a 50 mV swing voltage is 42.7 fJ/bit, which is calculated by taking the average of the DC power consumption (IV) at the on and off states. The holding energy is large for smaller voltage swings as the V_{off} values in those cases are also at a high DC level. The holding energy can be reduced by increasing the voltage swing while keeping V_{top} fixed at 1.0 V, which does not greatly increase the switching energy but substantially lowers the holding energy, as shown in Fig. 9(b). The holding energy for V_{pp} = 0.3 V at 1 Gbps is 26.5 fJ/bit. Under this voltage condition, the device operates with a maximum speed of 2 Gbps. As the holding energy scales inversely with the bit rate, the holding energy at 2 Gbps is thus 13.25 fJ/bit, which leads to a total energy consumption of only 14.65 fJ/bit (1.4 fJ/bit switching energy estimated by method (a)) at 2 Gbps. The total

energy consumed by our device is much lower than earlier reports on the cavity based carrier injection silicon EO modulators [4–7]. Comparing with non-cavity based silicon EO modulators, e.g, MZI modulators [9, 28, 29], the energy consumption is reduced by three orders of magnitude that clearly shows the advantage of using cavity approach to reduce the energy consumption of EO modulators.

Thus, to achieve the lowest switching energy, the optimum voltage condition for our device is V_{pp} = 50 mV, V_{top} = 1.0 V, while to realize the minimum total energy, the best voltage condition is V_{pp} = 300 mV, V_{top} = 1.0 V.

Please note that the charging energy ($\frac{1}{4}CV_{pp}^2$) also contributes to the switching energy consumption and depends on the capacitance of the device. In an integrated optical interconnect the metallic pads can be removed and therefore the charging energy depends on the junction capacitance of the device. Thanks to the small junction capacitance and an ultra-low swing voltage operation, the charging energy in our device is negligible (< 1 aJ/bit).

6. Conclusions

In conclusion, we have experimentally demonstrated a 1D silicon PhC cavity with a small footprint (600 nm wide) and silicon side slabs, which simultaneously achieves a high Q-factor and low resistance and capacitance values, which helps to reduce the swing voltage and energy consumption of EO devices. By using a 1D PhC cavity with side slabs, we demonstrated a carrier injection silicon EO modulator operating with the lowest reported switching voltage (50 mV) and switching energy (0.1 fJ/bit) at a 1 Gbps modulation speed, which is one to two orders of magnitude lower than previously reported results [4–7]. In addition to the switching energy, the DC energy consumption is also significantly reduced and we demonstrated a total energy consumption of 14.65 fJ/bit at 2 Gbps for optimum voltage conditions (V_{pp} = 300 mV, V_{top} = 1.0 V). Furthermore, ER is also improved compared with previously reported cavity based carrier injection silicon EO modulators [4–7]. We achieved a high ER (11 dB at 1 Gbps) and a maximum modulation speed of 3 Gbps (8 dB ER).

An analysis of the fall and rise times of the modulated optical signal shows that for the voltage conditions used the speed of the device is limited by the carrier injection process rather than carrier removal. Thanks to the small width of the 1D PhC cavity with its tightly bound mode, the modulation speed can be further improved by reducing the intrinsic region width. The combination of low energy consumption, high ER, GHz speeds and an ultra-compact size constitutes a significant step towards the development of energy efficient and compact silicon optical interconnects for future exa-scale computers.

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