optica

Photonic-crystal nano-photodetector with ultrasmall capacitance for on-chip light-to-voltage conversion without an amplifier

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Received 24 February 2016; accepted 31 March 2016 (Doc. ID 259981); published 5 May 2016

The power consumption of a conventional photoreceiver is dominated by that of the electric amplifier connected to the photodetector (PD). An ultralow-capacitance PD can overcome this limitation, because it can generate sufficiently large voltage without an amplifier when combined with a high-impedance load. In this work, we demonstrate an ultracompact InGaAs PD based on a photonic crystal waveguide with a length of only 1.7 μm and a capacitance of less than 1 fF. Despite the small size of the device, a high responsivity of 1 A/W and a clear 40 Gbit/s eye diagram are observed, overcoming the conventional trade-off between size and responsivity. A resistor-loaded PD was actually fabricated for light-to-voltage conversion, and a kilo-volt/watt efficiency with a gigahertz bandwidth even without amplifiers was measured with an electro-optic probe. Combined experimental and theoretical results reveal that a bandwidth in excess of 10 GHz can be expected, leading to an ultralow energy consumption of less than 1 fJ/bit for the photoreceiver. Amplifier-less PDs with attractive performance levels are therefore feasible and a step toward a densely integrated photonic network/processor on a chip. © 2016 Optical Society of America

OCIS codes: (230.5298) Photonic crystals; (230.5160) Photodetectors; (130.3120) Integrated optics devices.

http://dx.doi.org/10.1364/OPTICA.3.000483

1. INTRODUCTION

Future microprocessors will need an unprecedented many-core complementary metal oxide semiconductor (CMOS) architecture, and therefore will require dense network management on a chip with a high bit rate and low power consumption that cannot be matched by an electrical interconnect. To this end, on-chip/off-chip optical communication has been extensively studied [1–4]. For more sophisticated data processing in an on-chip application beyond simple optical communication, a photonic-network-on-chip (PhNoC) architecture, which includes many integrated nanophotonic devices that can manage high-speed optical signals, has also been discussed [1,5]. III–V materials and their photonic devices have been the main players as regards high-speed transceivers in telecom/datacom photonic networks, and are still promising candidates for the construction of these chip-com networks that can be integrated with laser sources, photoreceivers, and other functional nanophotonic devices with ultra-low-power consumption well beyond that of group-IV materials. Therefore, III–V nanophotonic devices should enhance the possible functions and density in computing networks beyond those achievable with silicon photonics technology.

The demand is increasing in particular for a compact photoreceiver for these applications, because its sensitivity will determine the optical power budget of the laser source and the loss budgets for intermediary components such as photonic switches, couplers, filters, and other routing devices. Photoreceivers generally consist of a photodetector (PD) and a trans-impedance amplifier (TIA) to generate sufficient voltage to drive the subsequent electronic circuits, and they are often fully integrated at the CMOS level for short-range optical interconnection [6,7]. However, even with a recent CMOS-integrated PD-TIA, the power consumption of several milliwatts dominates the total power of the system [2,3]. This amounts to a subpicojoule/bit level energy cost if we assume a signal bit rate of 10 Gbit/s, and concern is growing that this situation will constitute a significant bottleneck when establishing chip-com photonic networks [4]. One of the challenges with PDs is to realize an ultrasmall capacitance and thus allow the resistance–capacitance (RC) bandwidth to be kept at a high level even during connection to a high impedance receiver circuit. This would lead to a reduction of electrical amplification or even its elimination (referred as a receiver-less PD [4,8]). There would then be a strong demand for

nano-structure PDs with a small size (that is, a small junction capacitance) while maintaining high responsivity.

Photonic crystal (PhC) waveguides are promising as nano-PDs because of their strong light confinement in an ultrasmall dimension. We have already reported PhC-PDs embedded in an InGaAs absorption layer in an InP-based PhC waveguide, which we obtained using an ultracompact buried-heterostructure (BH) formation [9], and with which we demonstrated a detection bandwidth of around 6 GHz [10]. Such a BH technique should provide good applicability for nano-PDs, because this structure can confine both photons and carriers in an ultrasmall space that cannot be achieved by any other PDs. In addition, a lateral p-i-n junction and an air-bridge structure are also effective for the reduction of junction capacitance. On the other hand, Ge-waveguide PDs have been extensively studied for optical interconnection in a Si CMOS chip, and some of them are only 4 μm long [3,11]. However, InGaAs exhibits stronger absorption than Ge, and this is very important in terms of reducing PD size and subsequently junction capacitance. The applicable detection wavelength for InGaAs is longer than that for Ge, namely, the L-band range, resulting in its good applicability to a wide-range wavelength-division multiplexing (WDM) system. In addition, the potential for integration with InP-based active nano-photonic devices such as all-optical switches, memories, and lasers [12–14] with record-low power consumption is very attractive. With these features, the combination of PhC waveguides and InGaAs material offer the possibility of realizing a nano-PD with the smallest size and capacitance yet reported, which has great potential for use as a photoreceiver on a chip.

In this paper, we describe an InGaAs-embedded PhC-PD that has a detector length of only 1.7 μm, which still exhibits a high responsivity of 1 A/W and a clear eye diagram for a 40 Gbit/s signal. The theoretical capacitance is less than 1 fF, including the fringe electric field of a p-i-n junction. This offers the potential for high voltage generation simply by high-impedance loading without amplifiers. To demonstrate this, we fabricated a PhC-PD integrated with a several-kΩ load resistor. There has been no report evaluating the on-chip light-to-voltage conversion dynamics of nano-PDs, because any external 50 Ω electrical measurement system will affect the device load and make it difficult to directly measure the voltage across it. In our measurement, we employed an electro-optic (EO) probing technique to solve this problem, and this is its first demonstration for testing nano-PDs, to the best of our knowledge. This method clearly revealed a conversion efficiency as high as 4 kV/W and a multigigahertz bandwidth. Although the bandwidth of the present device is still limited by the parasitic capacitance of the additional metal wiring used for an EO probing measurement, the expected bandwidth would be more than 10 GHz when removing the parasitic elements. This suggests that the optical energy required as a photoreceiver is less than 1 fJ/bit even without electrical amplification. These results reveal a successful way of realizing an ultrasmall/ultralow-energy photoreceiver that can be densely integrated on a chip.

2. REQUIREMENTS FOR RESISTOR-LOADED P-I-N PD

To discuss the optical power required for a resistor-loaded p-i-n PD if we are to eliminate the need for an electrical amplifier when generating a signal voltage, we assumed the simple PD–resistor circuit shown in Fig. 1(a). The optical power needed for a p-i-n PD is determined by two requirements: (i) the optical power needed to obtain a sufficiently high signal-to-noise (S/N) ratio for error-free operation and (ii) the optical power needed to generate a sufficiently high voltage to drive an electrical circuit. With the aim of realizing a amplifier-less PD with only a connection to a load resistor, the S/N ratio is given by $(\mathrm{S/N})_{\mathrm{rms}} = \overline{i_s^2}/\overline{i_n^2}$, where $\overline{i_s^2}$ and $\overline{i_n^2}$ are the mean square of signal photocurrent and noise current, respectively, and are given by

$$\overline{i_s^2} = (\eta_{\mathrm{pd}} P_{\mathrm{in}})^2, \tag{1}$$

$$\overline{i_n^2} = \left\{ 2e(i_s + i_d) + \frac{4kT}{R_{\mathrm{eq}}} \right\} f_{\mathrm{BW}}. \tag{2}$$

P_{in} is the power of the input optical signal, η_{pd} is the responsivity of the p-i-n PD, e is the electron charge, i_d is dark current, k is the Boltzmann constant, T is temperature, R_{eq} is the equivalent resistance for a PD–resistor circuit including the PD resistance R_{pd} and load resistance R_{load}, and f_{BW} is the signal bandwidth. The first and second terms for $\overline{i_n^2}$ indicate shot noise and thermal noise

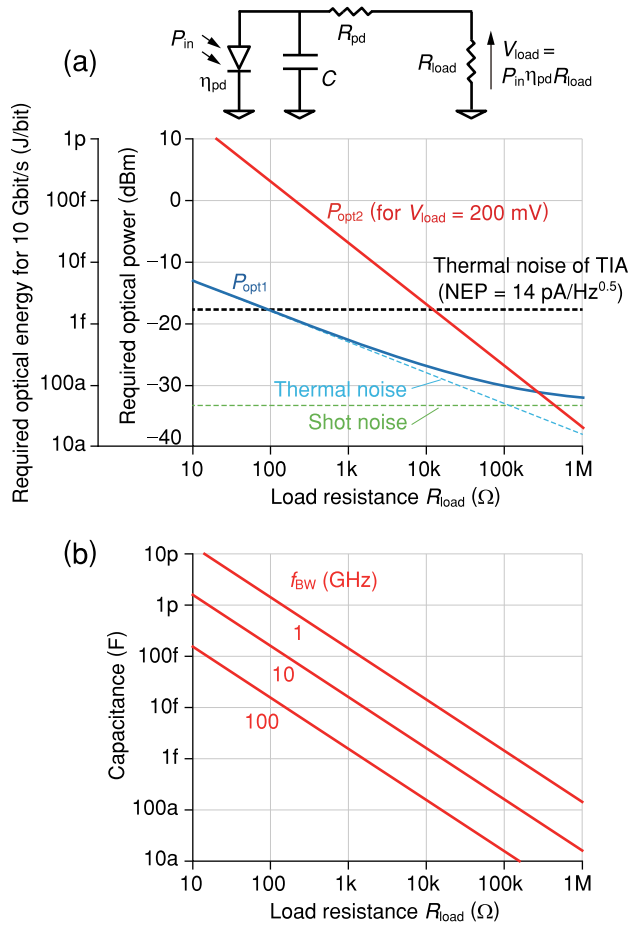

Fig. 1. Theoretical required optical power and capacitance for a resistor-loaded PD. (a) Calculated required optical power and energy for a bit rate of 10 Gbit/s. The circuit model is shown at the top. P_{opt1} and P_{opt2} are denoted by red and blue curves, respectively, while the required optical power for the PD-TIA circuit is shown by a black dashed curve. (b) Required capacitance. The three curves are for different RC bandwidths (1, 10, and 100 GHz). R_{pd} is assumed to be much smaller than R_{load}.

(Johnson noise), respectively. By arranging these equations, the optical power P_{opt1} needed to meet requirement (i) is given by

$$P_{\mathrm{opt1}} = \frac{1}{\eta_{\mathrm{pd}}}\sqrt{\left\{2e(i_{\mathrm{s}} + i_{\mathrm{d}}) + \frac{4kT}{R_{\mathrm{eq}}}\right\} f_{\mathrm{BW}} \cdot (\mathrm{S/N})_{\mathrm{rms}}}. \quad (3)$$

On the other hand, when we consider the photocurrent-to-voltage conversion at a load resistor needed to meet requirement (ii), the required optical power P_{opt2} is given by

$$P_{\mathrm{opt2}} = \frac{i_{\mathrm{s}}}{\eta_{\mathrm{pd}}} = \frac{V_{\mathrm{load}}}{\eta_{\mathrm{pd}} R_{\mathrm{load}}}. \quad (4)$$

This indicates that a high light-to-voltage conversion would be obtained with a high R_{load}, resulting in a reduction in the required optical power. When P_{opt1} and P_{opt2} are compared, the larger value determines the required optical power. Figure 1(a) shows the theoretical optical power as a function of R_{load}. Here, we assumed $\eta_{\mathrm{pd}} = 1$ A/W, $i_d = 100$ pA, and $T = 300$ K, which are our experimental results as described in Section 3. $f_{\mathrm{BW}} = 10$ GHz is assumed, and the required $(\mathrm{S/N})_{\mathrm{rms}}$ is 144 (corresponding to a Q factor of 6), which is assumed to achieve a bit-error rate of 10^{-9} [15]. P_{opt1} is calculated from Eq. (3) and is shown by the blue curve, and the shot noise and thermal noise are shown separately by dashed curves. The P_{opt2} curve for $V_{\mathrm{load}} = 200$ mV (red), which is needed to drive a CMOS inverter [3], is calculated from Eq. (4). A high R_{load} can reduce both P_{opt1} and P_{opt2}, although P_{opt2} dominates P_{opt1} up to the shot noise limit. As a reference, the black dashed line denotes the thermal noise limit for a CMOS-integrated PD-TIA circuit with a noise equivalent power (NEP) of 14 pA/Hz$^{0.5}$ [16], which determines the required optical power of around −18 dBm. With $R_{\mathrm{load}} = 20$ kΩ for a resistor-loaded PD, an optical power of −20 dBm or an optical energy of 1 fJ/bit for 10 Gbit/s is available, which are below those of a PD-TIA circuit. Note that a TIA also consumes a huge amount of electric power (several milliwatts) [2,3], and this dominates the overall power consumption. Therefore, a resistor-loaded PD with a sufficiently high R_{load} is attractive as an ultralow power photoreceiver.

On the other hand, we have to take the RC bandwidth into account, which is given by $f_{\mathrm{RC}} = (2\pi R_{\mathrm{load}} C)^{-1}$, where C is the equivalent capacitance of the circuit and should be as small as possible to maintain a large operation bandwidth. Figure 1(b) shows the capacitance needed to keep the RC bandwidth at 1–100 GHz. This indicates that $C < 1$ fF is required when considering $R_{\mathrm{load}} > 10$ kΩ and $f_{\mathrm{BW}} = 10$ GHz. Recent Ge-waveguide PDs have exhibited a junction capacitance of 4–5 fF [17,18], which does not meet this requirement. As a consequence, we need to reduce the capacitance of the PD to less than 1 fF to achieve both a high light-to-voltage conversion and a high bandwidth with a resistor-loaded configuration without any signal amplifiers.

3. DESIGN AND FABRICATION OF PhC InGaAs PD

We have employed the combination of a PhC waveguide and cavity and an ultrasmall BH to demonstrate optical nanodevices such as nanolasers and all-optical memories [9,12], which exhibited a record-low power consumption thanks to the strong confinement of both photon and carrier. This structure can be employed for PDs by embedding a compact InGaAs absorber, thereby reducing the junction capacitance by miniaturization. Figure 2(a) shows a schematic of our PhC-PD. The device consists of an InP PhC waveguide, a BH for embedding the InGaAs, and a lateral p-i-n junction. The fabrication process is the same procedure that we reported in [14,19]. Butt-joint regrowth was performed, and the InGaAs absorber was embedded in a 250-nm-thick InP slab. The absorber was designed with a thickness of 150 nm, a width of 400 nm, and lengths of 0.8, 1.7, and 3.4 μm corresponding to $2a$, $4a$, and $8a$, respectively, where a is the lattice period of the PhC. A lateral p-i-n junction was formed by employing Zn diffusion and Si ion implantation for the p- and n-type doping, respectively. The PhC air holes were formed by EB lithography and Cl_2-based dry etching. After metallization, the InAlAs sacrificial layer beneath the PhC slab was etched to form an air-bridge structure. The separation between the p- and n-doped layers was designed to be 0.9 μm, but it decreased slightly during the doping process. Figure 2(b) shows a scanning electron micrograph (SEM) image of the sample, indicating a flat surface thanks to the successful butt-joint regrowth. The air hole diameter and the lattice constant of the PhC were 200 and 420 nm, respectively. Because of the index difference between the input InP waveguide and the InGaAs-embedded waveguide, their widths

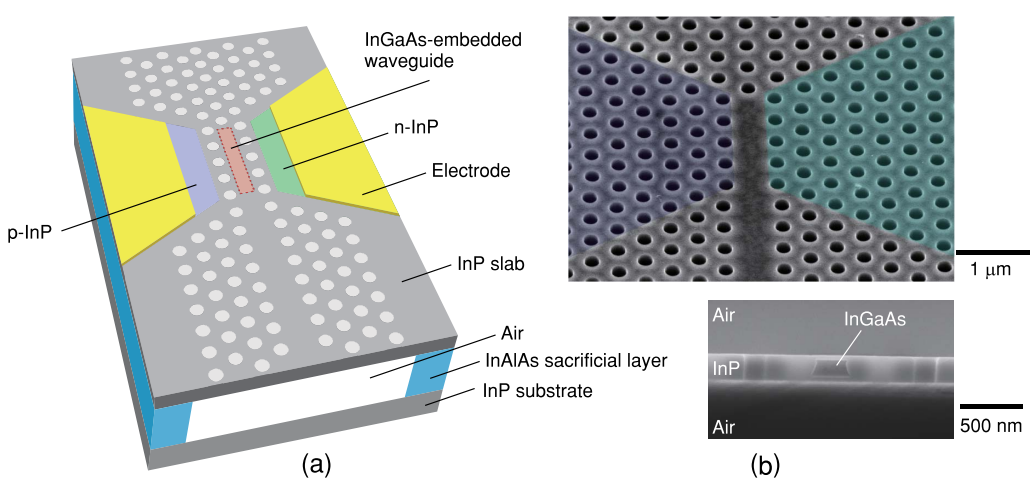

Fig. 2. PhC-PD structure. (a) Structural schematic of PhC-PD. (b) Top view and cross sectional view SEM images of fabricated device, where there are 8 rows of air holes beside the InGaAs absorber.

should be adjusted so that their guiding bands match. To this end, the widths of the InP and InGaAs-embedded region were changed to $1.1W_0$ and $0.95W_0$, respectively, where $W_0 = \sqrt{3}a$ is the basic line defect width defined as the removal of one row of air holes.

Thanks to the small physical dimensions of the p-i-n junction, the capacitance should be down to the fF level. To confirm this, we estimated the capacitance as shown in Fig. 3. Parallel-plate capacitance, which is identified as depletion capacitance, was approximated as $C = \epsilon_0 \epsilon_{\mathrm{InGaAs}} L_{\mathrm{abs}} T_j / d_j$, where ϵ_0 is the permittivity of a vacuum, $\epsilon_{\mathrm{InGaAs}} = 13.9$ is the relative permittivity of InGaAs, and $T_j = 0.25$ μm is the junction thickness. d_j is the roughly estimated width of the depletion layer when applying the bias voltage and is set to 0.5 μm, which might be reasonable for the full depletion of the absorption layer and the suppression of free-carrier absorption. L_{abs} is the InGaAs absorber length, which equals the junction length. The parallel-plate capacitance is less than 0.2 fF for $L_{\mathrm{abs}} < 3.4$ μm thanks to the ultrasmall dimensions, and is much smaller than those of the Ge-waveguide PDs with 4–5 fF [17,18]. However, for an ultrasmall junction, the fringing field contribution of the junction also becomes significant, and hence it is important to include the fringe capacitance [20]. This contribution was fully simulated by the finite-element method (FEM) with a full 3-D model, and is shown by red plots. The simulated capacitance for a doped region with a width of 5 μm and different L_{abs} indicates that the capacitance would be higher than that of the parallel plate model. The total capacitance of our PhC-PD is still < 1 fF, and this is still smaller than those of Ge-waveguide PDs. One of the reasons for such a low capacitance is the air-bridge structure, which results in a low fringe capacitance, and which has not been used for Ge-based PDs and previous InP-based PDs.

Another concern is the electrical pad, which has an area of 70 μm × 80 μm in our experiment and has a theoretical capacitance of about 11 fF. However, it should be removed when the device is actually integrated on a chip. Consequently, our PhC-PD structure has a sufficiently small capacitance for connection with a high load resistance at the 10 kΩ level.

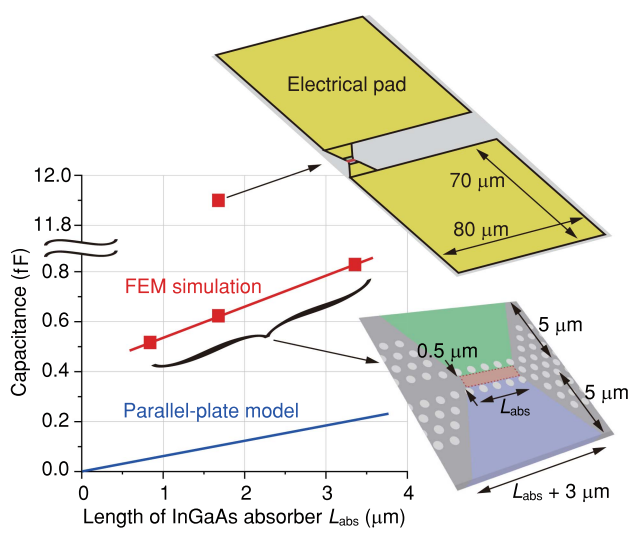

Fig. 3. Theoretical capacitance of PhC-PD. The blue curve is calculated from the parallel-plate model. The red plots are the results simulated by FEM with a 3-D model. The lower three plots are for only the p-i-n junction area of PD and the upper plot is for the PD with electrical pads.

4. DC OPTICAL RESPONSES OF PhC-PD

First the photocurrent characteristics for a continuous-wave (CW) light input were measured to evaluate the DC responses. In the measurement, a fiber polarization controller was used to tune the input light to TE polarization. The optical power in the waveguide should be estimated and used for evaluating the responsivity, because our PD would be applied for integrated on-chip/off-chip communication rather than for external fiber communication. The photocurrent for a different reverse bias voltage and CW optical power is shown in Fig. 4(a), for which a coupling loss of approximately −11 dB between the input fiber and the waveguide facet was used for the power estimation. The dark currents were approximately <100 pA and 15 nA for bias voltages of −2 and −10 V, respectively. Figure 4(b) shows photocurrent as a function of optical input power at a bias voltage of −2 V. Importantly, we successfully estimated a large optical responsivity of 0.98 A/W even for a surprisingly short absorber length of 1.7 μm. Figure 4(c) shows the photocurrent spectrum for a different absorber length. A photocurrent was observed for the wavelength range corresponding to the propagation band of the InGaAs-embedded PhC waveguide, which is located below a wavelength of 1.58 μm. The disappearance of the photocurrent below 1.49 μm is also due to the cut-off of the input PhC waveguide. The periodic peaks (2 nm interval) appear due to the Fabry–Perot interference between the waveguide facet end and the input boundary of the PD [10]. The photocurrent was reduced when the absorber length became short, as summarized in Fig. 4(d). The theoretical responsivity η_{PD} for a single round trip of light in the absorber is given by

$$\eta_{\mathrm{PD}} = \eta_{\mathrm{eff}} \cdot \frac{e}{h\nu} \cdot \left\{ 1 - \exp\left(-2\frac{n_g}{n} \alpha_{\mathrm{abs}} \Gamma L_{\mathrm{abs}} \right) \right\}, \tag{5}$$

where e is the electron charge, h is the Planck constant, ν is the frequency of light, n is the material index, n_g is the group index, α_{abs} is the absorption constant of InGaAs, Γ is the optical confinement factor, and L_{abs} is the absorber length. η_{eff} is a loss factor that includes the losses for both light and the photogenerated carrier. The former includes the optical propagation loss and the coupling loss into the absorber, while the latter includes carrier trapping at the hetero interface, which induces the radiative or nonradiative recombination of generated carriers. Specifically, our BH formation does not increase the nonradiative carrier recombination loss thanks to the successful butt-joint epitaxial growth. In fact, a carrier lifetime of 7 ns has been confirmed for our BH structure [12], and this would be long enough to prevent carrier loss during a fast carrier extraction in a PD. Figure 4(d) includes the theoretical curves given by Eq. (5), in which we adopted the simulated values of $\Gamma = 0.5$ and $n_g = 5$, and assumed parameters of $\alpha_{\mathrm{abs}} = 1.0 \times 10^4\ \mathrm{cm}^{-1}$, $n = 3.4$, and $\eta_{\mathrm{eff}} = 0.8$. The theoretical curves are a good fit with the experimental plots. The shortest length with which to maintain a high responsivity was $L_{\mathrm{abs}} = 1.7$ μm in this experiment. However, for further size reduction, a slow-light effect along with a higher n_g will work if we employ a careful design to suppress the backreflection of light [21].

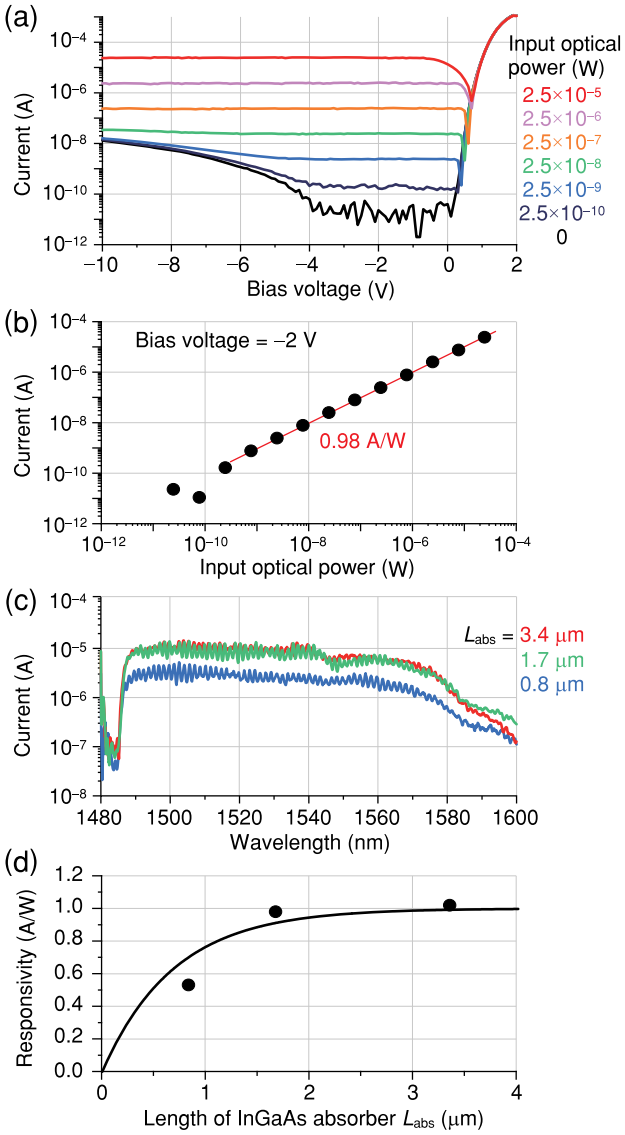

Fig. 4. Static response of the PhC-PD for CW light input. (a) Photocurrent versus applied bias voltage characteristics for a device with an absorber length $L_{abs} = 1.7$ μm. The light wavelength was set at the peak of the photocurrent spectrum (1536.7 nm). Different colors denote the different optical powers launched into the PD. (b) Photocurrent versus optical power characteristics plotted for a bias voltage of −2 V. (c) Photocurrent spectrum for different L_{abs}. The input optical power was 10 ± 3 μW. (d) DC responsivity versus L_{abs} characteristics. Experimental plots with theoretical curve are shown.

5. DYNAMIC OPTICAL RESPONSES OF PhC-PD

Figure 5 shows the operation dynamics of our PD with $L_{abs} = 1.7$ μm, into which we injected an intensity-modulated optical signal with a peak power of 100 μW. As shown in Fig. 5(a), clear eye openings were observed for 10, 20, and 40 Gbit/s non-return-to-zero (NRZ) signals generated with a $2^{31} - 1$ pseudo-random bit sequence. The small-signal responses for different reverse bias voltages are shown in Fig. 5(b). The 3 dB bandwidth was 28.5 GHz when the bias voltage was −12 V. This bandwidth suggests the capability for a bit rate of around 50 Gbit/s for an NRZ signal, which agrees with the observed eye diagram.

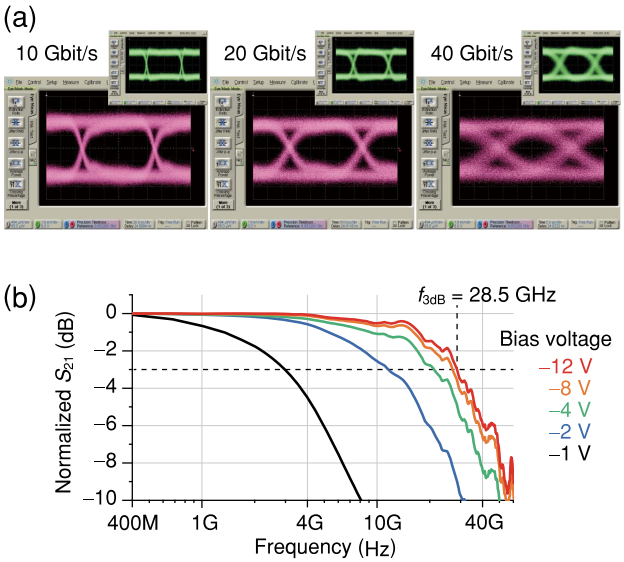

Fig. 5. Dynamic responses for a device with $L_{abs} = 1.7$ μm. (a) Eye diagram for 10, 20, and 40 Gbit/s NRZ optical signals. The green and red waveforms are the input optical signal and the detected electrical signal, respectively. (b) Small signal responses for different reverse-bias voltages. The wavelength was set at the peak of the photocurrent spectrum (1536.7 nm), and the optical peak power was 100 μW.

Several factors are involved in limiting the operation bandwidth; these might include the carrier traveling time across the intrinsic region and the RC time. If we assume a carrier drift velocity of 5×10^4 m/s [22] and a depletion width of 0.5 μm, the estimated carrier traveling time is 10 ps, which may not limit the operation bandwidth. This implies that there was no significant speed limitation caused by carrier trapping at the hetero interface. To explore the RC limitation, we compared the device with different series resistances, which were controlled by varying the length between the absorber and the electrical contact pad W_{ct}, as shown in Fig. 6(a). When the W_{ct} was, for example, 2, 5, and 10 μm, the differential resistances dV/dI under a forward bias condition (2 V) were estimated to be 0.3, 1.0, and 1.7 kΩ, respectively, which roughly correspond to the series resistance R_{pd} of the PD. Figure 6(b) shows the eye diagrams obtained at 20 and 40 Gbit/s for each W_{ct}, for which the reverse bias voltage and optical peak power were fixed at −12 V and 100 μW, respectively. This clearly revealed that the eye diagram was degraded with a larger W_{ct}. This suggests that the greatest limitation as regards the bandwidth must be the RC. When we consider the experimental 3 dB bandwidth of 28.5 GHz for the device with $R_{pd} = 0.3$ kΩ, the equivalent capacitance would be given as 19 fF from $f_{RC} = (2\pi R_{pd} C)^{-1}$. This is close to the simulated capacitance of 12 fF for the entire structure including the electrical pads, as shown in Fig. 3. Since theoretically our structure has an ultrasmall junction capacitance of 0.6 fF when removing the pad and integrating PDs on a chip, the operation bandwidth can be enhanced as long as the carrier traveling time does not impose a limit.

We also have some concern that optical power saturation would occur at a low power level due to the small absorber volume of our PhC-PD. To discuss this, Fig. 7 shows the eye diagrams for a bit rate of 20 Gbit/s obtained when the input optical power was

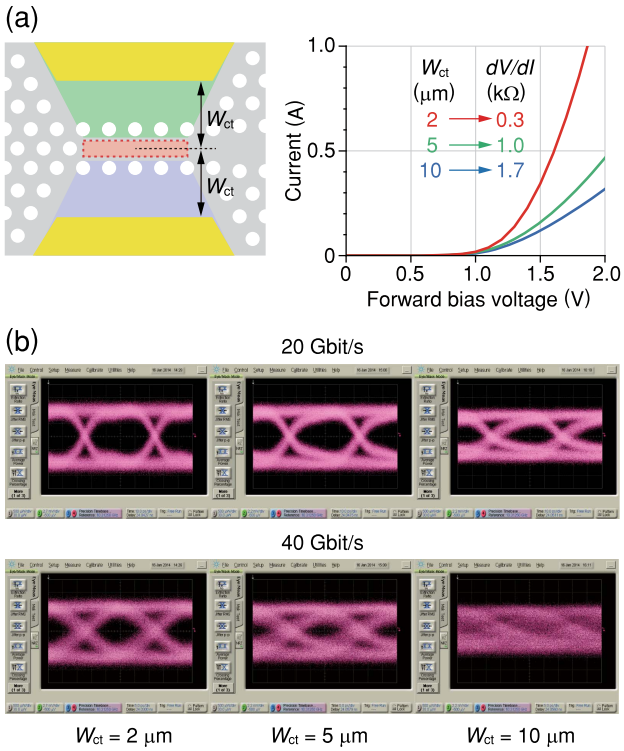

Fig. 6. Response speed limitation on the width of p/n-doped region. (a) The structure of the device and I-V curve for the forward bias voltage. W_{ct} is the distance between the absorber and the electrical contact pad. (b) Eye diagrams for a different W_{ct}. The bit rate was 20 Gbit/s (top) and 40 Gbit/s (bottom).

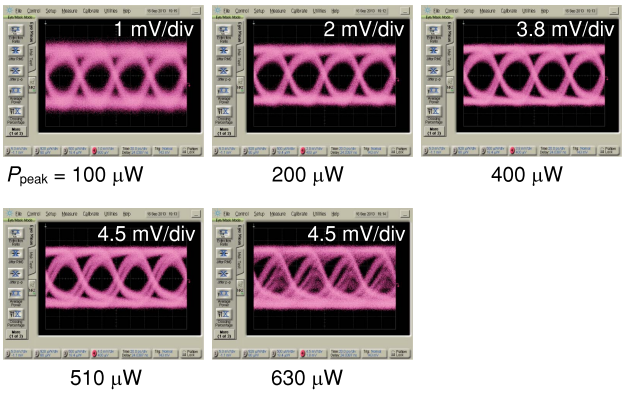

Fig. 7. Optical power dependence of the eye diagram. The optical peak power P_{peak} was changed under a fixed bit rate of 20 Gbit/s.

varied. The output level of the electrical signal increased linearly up to 400 μW, and the waveform is indeed degraded above 500 μW. Since the series resistance was 0.5 kΩ in the present device, the voltage drop in the series resistor can be calculated as 500 μW × 1 A/W × 0.5 kΩ = 0.25 V, which is much lower than the external bias voltage and should not induce degradation of the internal bias field. Another possible reason might be a carrier-induced screening effect, which also destructively weakens the internal bias field and makes the carrier extraction from the absorber slower. If we consider a total volume of 0.11 μm^3 for the absorber and assume a carrier traveling time of 10 ps as mentioned above, the estimated carrier density can be calculated as 3.5×10^{17} cm^{-3} for an input power of 500 μW. It has been reported that the same order of carrier density induces a carrier screening effect for InGaAs PDs [23], and therefore the measured saturation power is reasonable. This power can be translated into a 10 Gbit/s signal saturation energy of 50 fJ/bit. Our target optical energy is 1 fJ/bit for a resistor-loaded PD, as discussed in Section 2, and is sufficiently lower than the saturation level.

Table 1. Comparison with Ge-PDs Based on Various Nanostructures

Structure	Ge Waveguide [11]	Ge Nanowire [24]	Ge Nanowire with Plasmon Antenna [25]	This Work
Absorber length [μm]	4.0	1.5	0.15	1.7
Absorber volume [μm^3]	3.1	0.05	0.0007	0.11
DC responsivity [A/W]	0.8	0.01[a]	0.0001[a]	1.0
3-dB bandwidth [GHz]	45	—	—	28.5

[a]Assumed that light is illuminated from the top of the nanowire/antenna with a spot diameter of 1 μm.

Table 1 compares our device with some nanostructure PDs. A Ge-waveguide PD has a responsivity as high as our PhC-PD and an even higher bandwidth of 45 GHz. Our PD still has room for a higher bandwidth up to the carrier traveling time limit if we remove the parasitic RC components. On the other hand, the absorber volume of our PhC-PD (0.11 μm^3) was 1 order of magnitude smaller than that of a Ge-waveguide PD (3.1 μm^3). This allows our PD to have a much smaller capacitance, as discussed in Section 3. Nano-PDs based on a Ge nanowire [24] and a plasmonic antenna [25,26] offer great potential for reducing both length and volume. However, the light is currently detected by top illumination, and, hence, the light coupling with the absorber is poor. The plasmonic approach also suffers from significant absorption loss due to the metal. Therefore, the responsivity of these nanostructures is currently still too low for practical applications. As a consequence, only our PhC-PD can offer an ultrasmall size and capacitance while maintaining a high responsivity and high speed, which overcomes the conventional trade-off limit.

6. CONFIGURING A RESISTOR-LOADED PhC-PD

As discussed in Section 2, the ultrasmall capacitance of our PD enables us to connect it with a high load resistance to convert photocurrent to voltage while keeping a large RC bandwidth. However, there has never been a report evaluating the on-chip light-to-voltage conversion dynamics of resistor-loaded nano-PDs. The experimental difficulty is that a conventional measurement using an oscilloscope/network analyzer with an additional electrical pad would hinder correct device evaluation, because their impedances are generally lower than the device load, or 50 Ω in most cases. This makes it difficult to measure the voltage across the load. (Note that direct connection with a high-impedance CMOS gate would be available as a photoreceiver in on-chip communication.) In our measurement, we employed an EO probing technique [27], which is, to the best of our knowledge,

the first demonstration of its use for testing nano-PDs. When we prepared the sample for EO probing, our PhC-PD was connected to a load resistor on the same substrate, as shown in Fig. 8(a). The load resistor was incorporated with n-doped InP when the p-i-n junction was formed, and was connected with a gold strip line and electrical pads. We prepared different resistances R_{load} of 1.3–8.8 kΩ for a sample with a gold strip line and a length L_{strip} of 2.5 mm. For comparison with different parasitic capacitances, we also prepared a sample with a shorter strip line and an L_{strip} of 0.2 mm, for which we partly formed a thin platinum strip by using focused-ion-beam-assisted deposition, and used it as a load resistor with R_{load} values of 2.1 and 5.8 kΩ. As shown by the sketch of the PD–resistor circuit in Fig. 8(a), the AC voltage generated on the left side of the load resistor must be detected in EO probing.

The experimental setup for EO probing is shown in Fig. 8(b). Sinusoidal modulated light was injected into the PhC-PD. Photocurrent flows into the load resistor, and generates a modulated electric field (proportional to the voltage) between the strip lines. An EO probe consisting of an optical fiber with an EO crystal (ZnTe), which had an area of 0.25 mm square and that was attached to the tip, was brought toward the strip line. CW light with a wavelength of 1.55 μm was separately injected into the EO probe, at which the light is focused with a spot diameter of 12 μm on the inner surface of the EO crystal. This sensed the modulated electric field via the EO crystal. The light polarization was changed and detected by combining a polarization beam splitter, a balanced photoreceiver, and an RF spectrum analyzer. Before the device measurement, the EO probing voltage for AC voltage applied to the strip line was acquired to obtain the

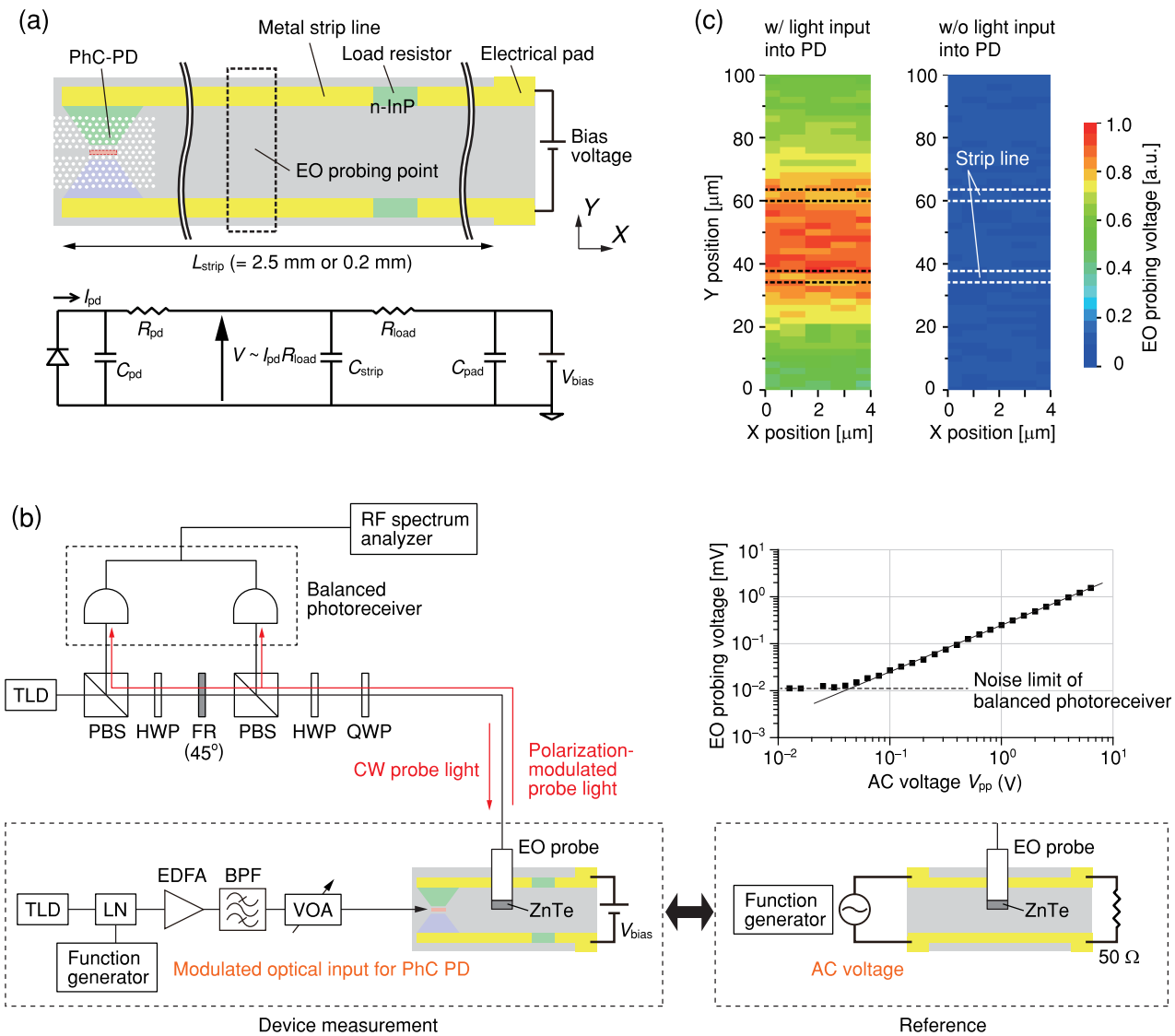

Fig. 8. Resistor-loaded PhC-PD and EO probing measurement setup. (a) Schematic of the sample (top) and corresponding equivalent circuit (bottom). The dashed square indicates the EO probing point. (b) Experimental setup for EO probing measurement. (TLD, Tunable laser diode; LN, Lithium-niobate modulator; EDFA, Erbium-doped fiber amplifier; BPF, Band-pass filter; VOA, Variable optical attenuator; PBS, Polarization beam splitter; HWP, Half-wave plate; QWP, Quarter-wave plate; FR, Faraday rotator) EO probing voltage for AC voltage applied to the reference strip line is shown in the right figure. (c) Spatial mapping of an EO probing measurement around the strip line. The left and right figures are with and without an optical input, respectively. The dashed line denotes the position of the metal strip lines.

correspondence between two voltages. To accomplish this, we tested a reference strip line that was terminated with a 50 Ω resistor, as shown on the right-hand side in Fig. 8(b). A sinusoidal voltage signal with a frequency of 50 MHz from a function generator was directly applied to the reference strip line, and the EO-probing voltage was detected just at the center of strip lines, from we observed a clear proportional relationship. Thereafter, we replaced the reference with a PhC-PD sample to evaluate the photogenerated voltage, as shown on the left in Fig. 8(b). An intensity-modulated light with the same frequency was injected into the PhC-PD under a reverse bias voltage of −4 V, and an EO probing measurement was performed. Figure 8(c) shows the spatial mapping when the EO probe was scanned in the X/Y direction around the strip line. This indicates that the photogenerated voltage between the strip lines was actually detected only when the light was injected into the PhC-PD.

7. DEMONSTRATION OF ON-CHIP LIGHT-TO-VOLTAGE CONVERSION

Several types of resistor-loaded PhC-PD were measured via EO probing to demonstrate the light-to-voltage conversion. Figure 9 shows the light-to-voltage conversion characteristics for PDs with

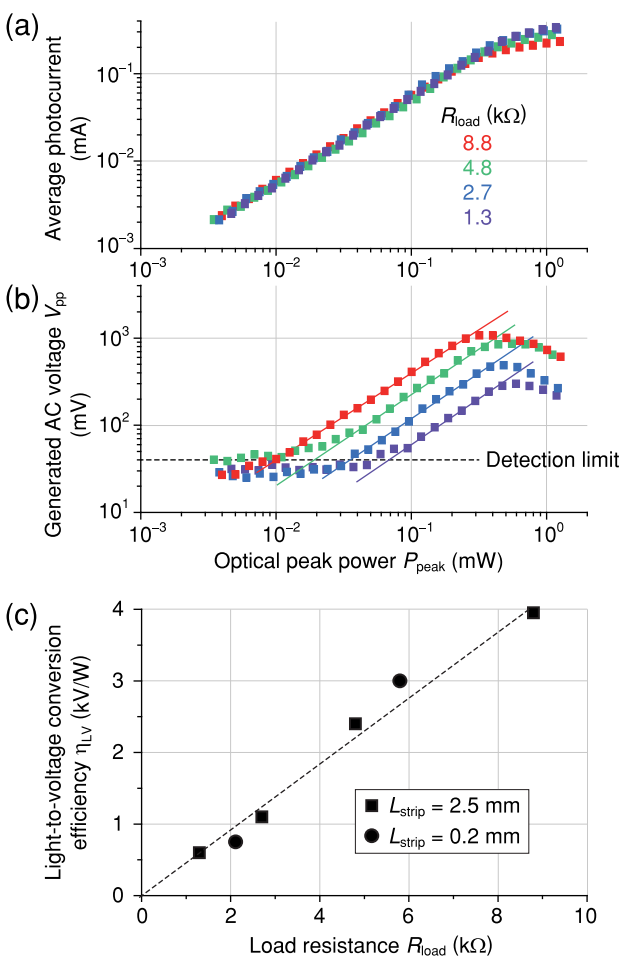

Fig. 9. Light-to-voltage conversion characteristics. (a) Average photocurrent and (b) generated AC voltage as a function of optical peak power. The length of the strip line L_{strip} is 2.5 mm. (c) Light-to-voltage conversion efficiency for different load resistances R_{load}. Square and circle plots denote the results for L_{strip} values of 2.5 and 0.2 mm, respectively.

different R_{load} values. As shown in Fig. 9(a), the average photocurrent was almost the same whatever the R_{load} value, which maintained the responsivity at $\eta_{pd} = 1$ A/W. On the other hand, as shown in Fig. 9(b), the generated AC voltage V_{pp} clearly increased when R_{load} was larger, even for the same photocurrent. The maximum V_{pp} of 1.1 V was obtained before the saturation. Figure 9(c) plots the light-to-voltage conversion efficiency η_{LV} for different R_{load} values, and shows a proportional relationship. There was concern that a large R_{load} would induce a voltage drop due to the photocurrent flowing into the load resistor and reduce the internal bias field across the absorber, which would make the carrier extraction slower and also reduce the generated AC voltage. However, we confirmed a clear proportionality between η_{LV} and R_{load} without any indication of saturation in this R_{load} range. A maximum conversion efficiency $\eta_{LV} = 3.95$ kV/W was achieved for $R_{load} = 8.8$kΩ. These results show that an optical power of 50 μW can generate the required V_{pp} of 200 mV for a CMOS inverter. In addition, then η_{LV} values are maintained for different lengths of strip line, namely, $L_{strip} = 2.5$ and 0.2 mm, and are hence assumed to be determined solely by R_{load}. The modulation frequency was 50 MHz in this test, and therefore the capacitance does not affect η_{LV}.

On the other hand, the maximum available frequency (or operation bandwidth) was strictly limited by RC. In our test sample, a gold strip line and a pad with a much larger capacitance than the PhC-PD were included because they were necessary for EO probing, and they must affect the bandwidth. Hence, the frequency response was carefully investigated to determine each contribution to the bandwidth. In the measurement, the S_{21} parameter was evaluated by assigning a modulated light injected into the PD as an input and the modulated probe light through the EO probe as an output. Figure 10(a) shows the frequency responses for different R_{load} values, in which samples with different L_{strip} values of 2.5 and 0.2 mm were evaluated. The smaller R_{load} and L_{strip}, which resulted in a shorter RC time, apparently increase the bandwidth. The RC-limited bandwidth for $L_{strip} = 2.5$ mm was estimated from $f_{RC} = 120$–750 MHz for R_{load} values of 1.3–8.8 kΩ, while that for $L_{strip} = 0.2$ mm increased up to $f_{RC} = 1.2$–2.7 GHz. Figure 10(b) summarizes the 3 dB bandwidth (blue plots for left vertical axis) as a function of $1/(R_{load} + R_{pd})$. These plots have a linear relation as they are mainly determined by $f_{RC} = [2\pi(R_{pd} + R_{load})C]^{-1}$. The capacitance C consists of both the junction capacitance of the PhC-PD and the parasitic capacitance caused by the strip line and pads. The dashed lines are the theoretical curves obtained by assuming $C = 16$ and 110 fF, which are dominated by parasites, and fit well with the experimental plots.

Another figure we evaluated was the product of η_{LV} and f_{RC}, which are in a trade-off relationship, because they are proportional to R_{load} and $(R_{pd} + R_{load})^{-1}$, respectively. This efficiency–bandwidth product (EBP) [V/W·Hz] (= [V/J]) can indicate the optical energy needed to generate the required voltage, regardless of the bit rate of the optical signal. The EBPs for different R_{load} and L_{strip} values are denoted by green plots on the right vertical axis in Fig. 10(b). A shorter L_{strip} enhances the EBP because f_{RC} increases while η_{LV} remains constant [see Fig. 9(b)]. The EBP values were in the 4–5 × 10^{11} and 2–3 × 10^{12} V/J ranges for $L_{strip} = 2.5$ and 0.2 mm, respectively. As a result, they can be translated to required optical energies of 200 and 33 fJ/bit for $L_{strip} = 2.5$ and 0.2 mm, respectively, to obtain $V_{pp} = 200$ mV

with an NRZ optical signal. For comparison, a commercially available high-speed PD-TIA module (manufactured by Finisar Corp., XPRV2021 with a static power consumption of 0.3 W [28]), has a conversion efficiency of 0.15 kV/W and an EBP of 6×10^{12} V/J. Our PhC-PD has comparable EBP, and more significantly, consumes a static electric power of just 80 μW due only to the dark current (20 μA with $V_{\text{bias}} = -4$ V), although this can be substantially suppressed by blocking the leakage path. The additional dynamic energy caused from the bias voltage supply is also a concern [29], because it induces a dissipation energy due to the phonon scattering of photogenerated carriers. However, it can be also suppressed by optimizing the p/n doping profile to reduce the bias voltage even down to the zero level [30,31].

Finally, we theoretically discuss an ideal case where there is no parasitic capacitance. The bold dashed curves in Fig. 10(b) denote f_{RC} and EBP in an ideal situation calculated by assuming only a PD junction capacitance of $C = 0.6$ fF. This makes the bandwidth higher than 10 GHz, which should be practically acceptable. Subsequently, the expected EBP exceeds 10^{14} V/J, corresponding to a required optical energy of less than 1 fJ/bit. These performance levels significantly surpass the performance of a conventional PD-TIA. Such a situation can be realized by removing the strip line and the pads used in the experiment, because they were needed only for the EO-probing measurement. For on-chip communication, an integrated through-hole-via connection can be expected [32,33], and it might be available even for InP-based devices by using a heterogeneous integration technique [34]. Such close integration between a PD and a CMOS circuit would bring us close to the ideal situation. As a consequence, our experimental and theoretical results for an ultrasmall PhC-PD have revealed the feasibility of an amplifier-less photoreceiver on a chip with a practically acceptable size, efficiency, bandwidth, and power consumption.

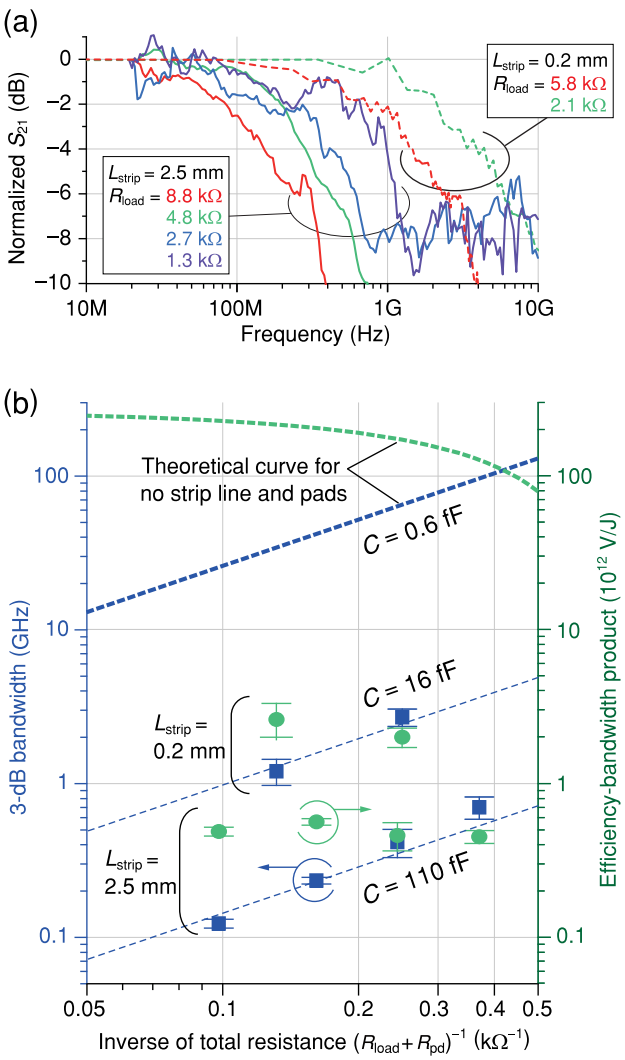

Fig. 10. Dynamics for resistor-loaded PhC-PD. (a) Small-signal responses for different load resistances R_{load} and strip line lengths L_{strip}. (b) 3-dB bandwidth (square plots for left axis) and the efficiency-bandwidth product (circle plots for right axis). The plots show the experimental results, and the dashed curves show the calculated results considering both the PD junction capacitance and the parasitic capacitances. The bold dashed curves are calculated under the assumption of no parasitic capacitances.

8. SUMMARY

Ultralow capacitance nano-PDs are needed for use in configuring a resistor-loaded photoreceiver that does not require an amplifier circuit. However, they have yet to be realized due to the conventional limitation that prevents the combination of a high responsivity and a small junction. We overcame this limit by employing a PhC nanostructure in which a small InGaAs absorber was embedded, which allowed us to reduce the detector length to just 1.7 μm while demonstrating a high responsivity of 1 A/W and an eye opening for a 40 Gbit/s signal. The junction capacitance fell to less than 1 fF and was small enough to enable us to configure an amplifier-less PD by integrating it with a load resistor. To this end, we actually fabricated a resistor-loaded PhC-PD, and successfully demonstrated what, to our knowledge, is the first light-to-voltage conversion to employ an EO-probing measurement, with an efficiency of up to 4 kV/W. This suggests that an optical power of less than 100 μW is enough to drive the CMOS inverter. The gigahertz level operation bandwidth was also evaluated, and it can be enhanced simply by removing the parasitic elements and thus increasing the RC bandwidth above 10 GHz. These demonstrations clearly revealed a promising way of realizing a photoreceiver that operates with an optical energy of less than 1 fJ/bit. The interconnection of our PD with PhC nanolaser sources that can be fabricated on the same substrate would enable us to realize a femtojoule/bit-level optical link. Such a system will provide a high-density photonic network over a many-core CMOS architecture.

Funding. Core Research for Evolutional Science and Technology, Japan Science and Technology Agency (CREST-JST).

Acknowledgment. We thank T. Tamamura, H. Onji, Y. Shouji, and K. Ishibashi for support in fabricating the device. We also thank H. Togo for support in establishing the EO-probing measurement setup.

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