Towards Bendable Piezoelectric Oxide Semiconductor Field Effect Transistor based Touch Sensor

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***Abstract*—This paper reports recent advances related to the piezoelectric oxide semiconductor field effect transistor (POSFET) based touch sensing system research. We reported in past, the POSFETs with basic electronics realized on planar silicon substrates using CMOS technology. However, the planar POSFETs could not be used on 3D or curved surfaces such as the fingertip of a robot. To overcome this challenge we are now investigating the ultra-thin-chip approach for obtaining bendable POSFETs tactile sensing array. This paper presents this approach towards obtaining bendable POSFETs. Furthermore, for the first time the theoretical behavior of POSFETs devices are examined by combining the piezoelectric capacitor model proposed and the physics of underlying metal-oxide-semiconductor (MOS) FETs in the linear and saturation regions. The device characteristic equations are simulated using MATLAB and comparable matching is achieved with the experimental measurements. The model result gives a unique insight into geometrical and material properties of piezoelectric polymer on the electrical properties of transistor for flexible electronics applications. Using this model, the Spice simulation of POSFET device in a single-ended op-amp configuration, and the effect of chip thickness on deflection are presented.**

***Index Terms*—Flexible Electronics, Piezoelectric Effect, POSFET, Tactile Sensing.**

I. Introduction

With the realization of computers and humanoid robots in the early 1980s, the necessity and importance of tactile sensing technology was recognized. Tactile sensing is the process of determining physical properties like shape, size, texture etc. and events by touching or making physical contact to the objects in the world [1]. Although the human body is well adapted to this and can decide how to handle an object, it is quite tough for any robot to do a similar task. For completing the task like holding a pen or breaking eggs, it need well developed and robust tactile sensors. Tactile sensors for robotics application are available in many varieties. They use different types of techniques like smart/engineered materials, transduction mechanisms, organic and inorganic electronics etc. but most of them are limited either due to slow response because of low mobility or due to large area [2]. Contrary to these, MEMS based approach gives an attractive way to miniaturise and integrate transducer directly in the existing well-developed and fast CMOS technology. One of the promising candidates, Piezoelectric Oxide Semiconductor Field Effect Transistor (POSFET), uses piezoelectric thin film as a transducer on its gate area [3] [4]. However, MEMS based tactile sensing devices cannot withstand large pressure/force due to their inherent fragile nature and therefore lacks flexibility and conformability needed for better integration with curved body parts. As flexible electronics are conceived as next generation technologies currently pursued by researchers around the world to support the strongly emerging market in this area [5]. Various approaches to thinning down and transfer to flexible substrate to obtain ultra-thin bendable tactile sensors have been investigated. One possible way to obtain flexible POSFET chips is by following the 'chip-on-flex' concept in which chips are fabricated over planar silicon and then bulk silicon is removed from the backside [6]. Since on achieving thickness below 50 μm Si get more flexible and stable, these sub-50-μm chips are ideal for the futuristic thin-film electronic.

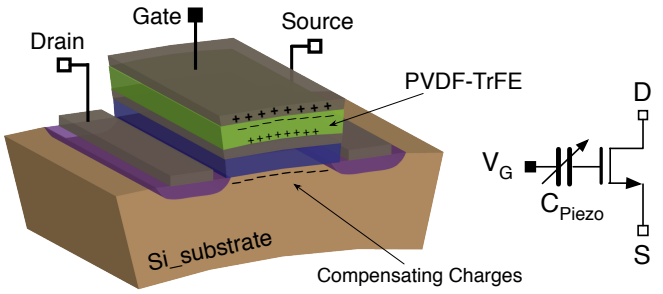

Fig. 1: Structure of bendable POSFET device and its schematic symbol.

II. Piezoelectric Oxide Semiconductor Field Effect Transistor

The structure of proposed bendable POSFET device shown in Fig. 1, which is similar to a planar FeRAM but with piezoelectric polymer layer sandwiched between bottom and top metal gate electrodes [7]. A piezoelectric polymer film, when in the pressure sensing mode, generates a charge displacement on application of a mechanical force/stress which is approximately given as:

$$D_{33} = d_{33}T_3 + \varepsilon_{33}^{T}T_3 \quad (1)$$

D is electric displacement, T is mechanical stress, E is the electric field, ε is dielectric constant under constant stress, and d is piezoelectric constant in thickness mode respectively [8]. The POSFET device is fabricated by spin coating a well known piezoelectric co-polymer poly[(vinylidenefluoride-co-trifluoroethylene] (PVDF-TrFE), over the gate area of MOSFET. The polymer is then poled by applying high voltage across the film at elevated temperature leading to the alignment of the dipoles in one direction. Any change in polarisation charges insides in the polymer due to force application thus modulate the carriers in the channel region of underlying transistor which can be translated to change in current or voltage. Thus, POSFET device is able to directly convert force or pressure stimulus to electrical output, which can be processed with signal conditioning electronics.

III. Modeling

A. Analyitcal Model of Piezoelectric capacitor

Since, the piezoelectric effect of sensor originates from induced polarization. To induce polarization, the dipoles in a semi-crystalline polymer such as PVDF-TrFE must be re-oriented through the application of a strong electric field at elevated temperature. In order to theoretically investigate the effect of poling on electrical characteristics of POSFET, we have proposed a mathematical model. The model combines the hysteresis property of piezoelectric polymer with standard MOSFET characteristics equation. Miller et al. have proposed a simple model, which relates polarization charge density with the applied electric field as [9]

$$P^{+}(E) = P_s \ \tanh\left(\frac{E - E_c}{2\delta}\right) + \varepsilon_F \varepsilon_0 E \tag{2}$$

where

$$\delta = E_c\left(\ln\left(\frac{1+\frac{P_r}{P_s}}{1-\frac{P_r}{P_s}}\right)\right)^{-1} \tag{3}$$

$$P^{-}(E) = -P^{+}(-E) \tag{4}$$

where P_s is saturation polarization, P_r is remnant polarization, E_c is coercive field, $P^{+}(E)$ and $P^{-}(E)$ denotes positive going (lower) branch and negative-going (upper) branch of hysteresis curve respectively and denotes the linear contribution of dipole moment. For PVDF-TrFE, Fig. 2 shows the simulated hysteresis curve with $P_r = 5\ \mu C/cm^2$, $P_s = 2\ \mu C/cm^2$ and coercive voltage of 40 V corresponding to $E_c = 160\ kV/cm$ which are obtained from experimental measurement.

B. Analyitcal Model of POSFET

During poling, the switching polarization charges in polymer, P_{sw} that is defined as the charge switched from one remnant polarization state to the maximum polarization state of the opposite polarity, accumulates as compensation charges at the junction of semiconductor and gate oxide.

$$P_{sw} = P_s + P_r \tag{5}$$

These compensation charges shift the flatband voltage of transistor depending upon the polarity of charges. For NMOS and positive poling, negative charges accumulates and leads to reduction in flat-band voltage.

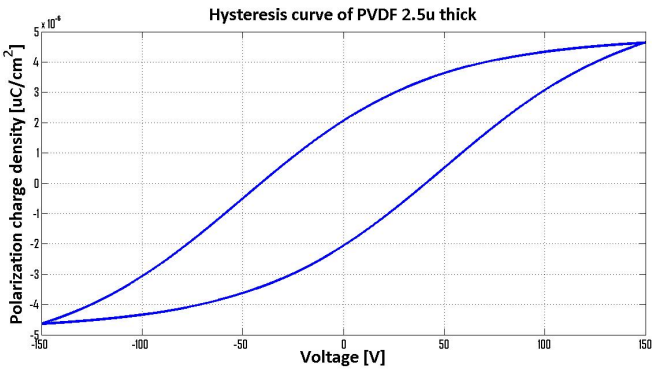

Fig. 2: Simulated Hysteresis curve of PVDF-TrFE.

$$V_{FB_{eff}} = V_{FB} - \left(\frac{P_s + P_r}{C_{ox}}\right) \tag{6}$$

The shift in flat-band voltage change the threshold voltage with same value.

$$V_{th_{eff}} = V_{th} - \left(\frac{P_s + P_r}{C_{ox}}\right) \tag{7}$$

This effective threshold voltage comes in play with the series capacitance of polymer and gate oxide, here on referred as stack capacitance.

$$\frac{1}{C_{stack}} = \frac{1}{C_{ox}} + \frac{1}{C_{PVDF}} \tag{8}$$

Here C_{ox} is the oxide capacitance given by $\frac{\varepsilon_{ox}}{t_{ox}}$ and C_{PVDF} is the capacitance introduced by polymer layer, which can be written $\frac{\varepsilon_{PVDF}}{t_{PVDF}}$. These two modified parameters can be then used within standard MOSFET characteristics equation to get the electrical characteristics of POSFET in linear and saturation region of operation.

$$I_{DC} = \mu_n C_{stack} \frac{W}{L}\left[(V_{gs} - V_{th_{eff}})V_{ds} - \frac{1}{2}V_{ds}^2\right] \quad Linear \tag{9}$$

$$I_{DC} = \mu_n C_{stack} \frac{W}{L}(V_{gs} - V_{th_{eff}})^2 \quad Saturation \tag{10}$$

The device parameters used in simulation are taken from the already fabricated POSFET device and are provided in Table I. Fig.3 (a) and Fig.3 (b) shows the characteristic curve and transfer curve of POSFET device after poling at different gate and drain voltages. Reasonable matching of simulated data has been achieved with the experimental curves.

TABLE I: Parameters Used In Simulation

Parameter	Symbol	Value
Width	W	3276 μm
Length	L	12 μm
Mobility	μ_n	850 $cm^2/V{\cdot}s$
Oxide Thickness	t_{ox}	45 nm
PVDF-TrFE Thickness	t_{PVDF}	2.5 μm
Relative Permittivity of PVDF-TrFE	ε_{PVDF}	12

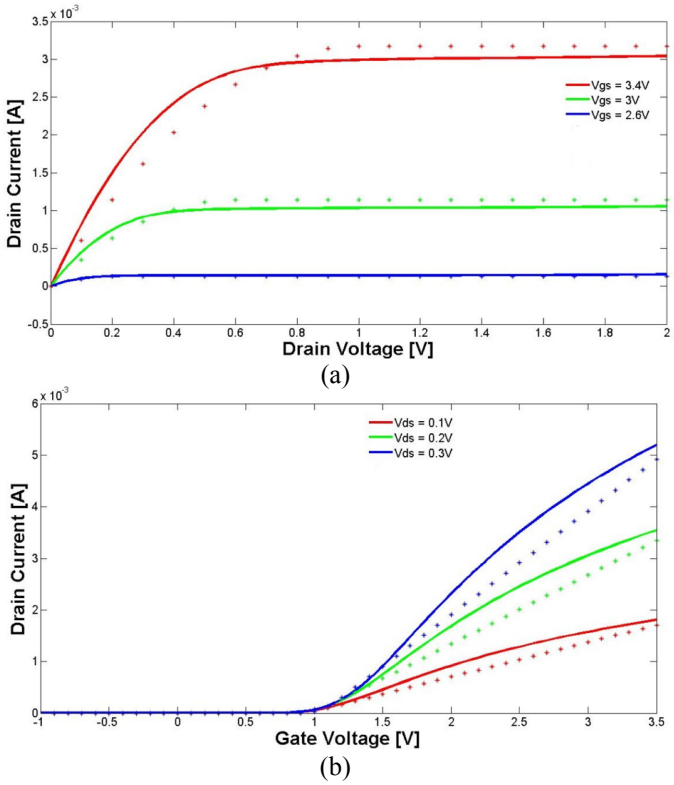

Fig. 3: Output curve of POSFET (simulated [dotted] vs experimental [solid]), drain current as a function of (a) drain voltage and (b) gate voltage.

IV. Design and Layout of Bendable POSFET

The MOS part of the touch sensing devices has interdigitated structure for large trans-conductance and will be fabricated using the single metal, n-MOS technological module of 4 μm p-well CMOS process. The chip size will mostly be 1 cmx 1cm having single sensor, array of sensors, and electronics etc. PVDF-TrFE solution in methyl ethyl ketone will be then spin coated over the wafer and then patterned using the top metal Gold as mask. Fig. 4 shows the cross section of device. Planar POSFET has been reported by Dahiya et al. in past, but due to lack of flexibility, the usage of these tactile sensors are limited to flat areas [3]. In present time there are many post-processing ways and techniques in use which produce thin silicon membrane of thickness ranging from 10 μm - 100 μm. Bulk micromachining using wet anisotropic etching of silicon being one of them is a well-established and cheap way to obtain ultra-thin bendable chips [10].

Since this way needs the patterning of backside oxide, special attention needs to be given to the dimension of mask size. Due to anisotropic nature of etching, the dimensions of the mask needs to be at least $\sqrt{2}H$ times more the dimension of membrane, i.e.

$$W = W_0 + \sqrt{2}H \tag{11}$$

where H is the thickness of the material, which need to be etched away [11].

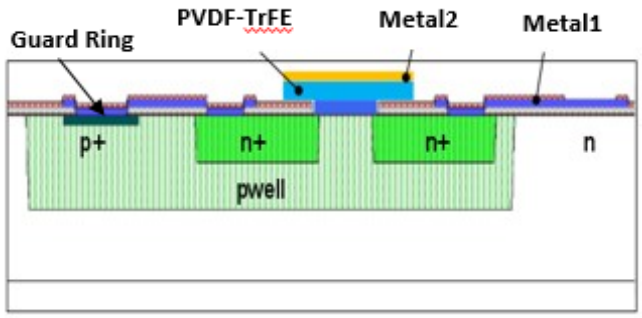

Fig. 4: Cross section view of device layout.

While, on the one hand the thickness of the chip should be as less as possible for better conformability, on the other hand the mechanical properties of silicon membrane also have to be considered before deciding the final thickness of thin tactile sensors. In this area, equations (12) and (13) establishes the relationship between dimension of circular membrane (r), thickness (H), pressure applied (P) with Young modulus (E), and Poisson ratio of silicon (ν) [12]:

$$y = \frac{3P(1-\nu^2)r^4}{16\pi EH^3} \tag{12}$$

This can be simplified for square membrane as:

$$y = \frac{0.0138Pa^4}{Eh^3} \tag{13}$$

From above equations, it is evident that lower the thickness higher the deflection of chip and at the same time is directly proportional to pressure and dimension of membrane.

V. The POSFET-Operational Amplifier

For the sensor integration, a measurement circuit tracks the output of POSFET device as the force stimulus is varied. Instead of using touch sensor as an 'add-on' whose output signal need to be further processed, a more practical solution is to integrate the sensor as a circuit component. However, to reduce the environmental noise entering output has always been a challenge. In this work, a POSFET device as one of

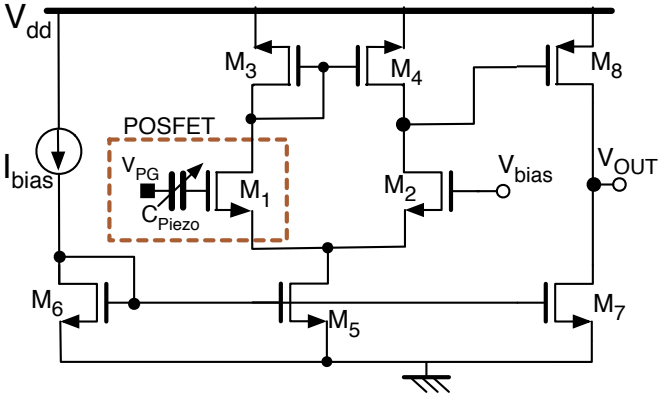

Fig. 5: Schematic of POSFET operational amplifier.

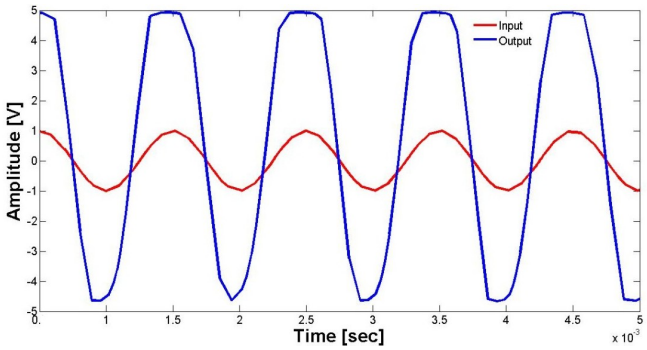

Fig. 6: Input vs Output of POSFET op amp simulated in PSpice.

TABLE II: Aspect Ratio of Transistors Used in PSpice

Transistor	Aspect Ratio (W/L)
M1, M2	3276/12
M3, M4	160/12
M5, M6	80/12
M7	240/12
M8	12

the input transistors in the differential stage of operational amplifier proposed, which it nullify the noise common to both input transistors and rescues the signal difference by directly measuring the input terminals [13]. The circuit functions as follow: When the POSFET op-amp is configured as source follower, any difference in input stage gets amplified at output, so whenever the sensor experience some force stimulus while the other transistor remains at fixed bias voltage, the difference between the two will get amplified and appear at output. Fig. 5 shows the schematic of sensing device in differential amplifier configuration.

The circuit is simulated in PSpice with sine waveform as input and the output curve is shown in Fig.6. Fig. 7 shows the gain and phase plot of amplifier with gain of 42.3 dB and gain bandwidth product of 1.5 MHz which shows the robust nature of proposed configuration.

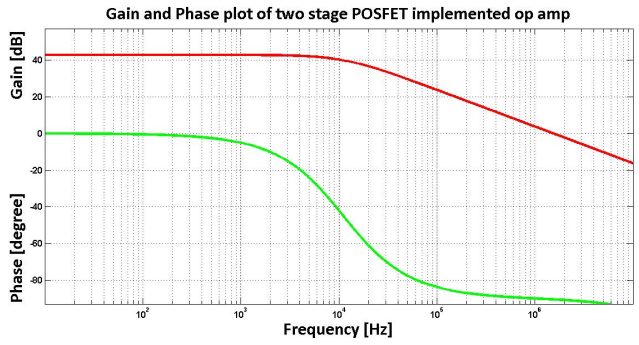

Fig. 7: Gain and phase plot of the simulated operational amplifier.

VI. Conclusion

The development of flexible, fast and robust tactile sensors is the need of the present sensing technology. The work presented in this paper is a step toward that. Firstly, the working principle of POSFET device has been discussed with some theoretically investigation of the electrical properties of the device, showing how the different polarization charge of polymer affects the charge arrangement in semiconductor region. Secondly, we proposed the differential op amp configuration for the tactile sensing device and PSpice implementation with a good gain and bandwidth.

In future, tactile sensing chips with array of sensors, on chip and out of the chip electronics will be fabricated according to the proposed technological module and then major challenge of thinning and handling will be tackled. To move in this direction, we have also studied and presented the chip and wafer level deflection and its relationship with various material and external parameters. Once thinned and packaged, these ultra-thin and bendable tactile sensors will be able to conform themselves as per the requirements without compromising with speed and at the same time will be able to cover large area and thus improving their usefulness.

Acknowledgment

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