InAs FinFETs with H_{fin} = 20 nm fabricated using a top-down etch process

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***Abstract* — We report the first demonstration of InAs FinFETs with fin width W_{fin} in the range 25–35 nm, formed by inductively coupled plasma etching. The channel comprises defect-free, lattice-matched InAs with fin height H_{fin} = 20 nm controlled by the use of an etch stop layer incorporated into the device heterostructure. For a gate length L_g = 1 μm, peak transconductance $g_{m,peak}$ = 1430 μS/μm is measured at V_d = 0.5 V demonstrating that electron transport in InAs fins can match planar devices.**

***Index Terms*—MOSFETs, FinFETs, high-mobility channel, semiconductor-metal interfaces, III-V semiconductor materials.**

I. Introduction

In recent years, the performance potential of III-V N-MOSFETs with InAs or composite InGaAs/InAs channels for future CMOS applications has been demonstrated in the planar quantum well (QW) configuration [1-3]. As the CMOS IC industry moves into the sub-20 nm technology regime, FinFET technologies have shown significant promise [4] (alongside FDSOI [5]), and the aspect ratio trapping technique has been shown to enable the integration of high mobility channel materials onto a 300 mm silicon platform in a fin configuration [6,7]. Much attention has now turned to tri-gate devices with III-V channels. Significant advances in performance and understanding have been made in this area [8-12], including the first example of a replacement fin III-V FinFET on a 300 mm silicon platform [13]. Electron transport metrics such as injection velocity improve with increasing In mole fraction x in $In_xGa_{1-x}As$ approaching $4{\cdot}10^7$ cm/s for InAs [2] making an InAs channel particularly attractive for N-FETs.

We have previously demonstrated a planar InAs QW N-MOSFET technology [1], using MBE-grown device heterostructures lattice-matched to InAs substrates with 6.06 Å lattice constant with electrostatically induced extensions [14,15] and incorporating NiInAs source-drain (S-D) contacts [16]. The planar device heterostructure comprised the InAs channel layer, an $In_{0.05}Al_{0.95}As_{0.20}Sb_{0.80}$ wide bandgap buffer layer to provide quantum confinement of the electrons to the channel and to isolate the channel from the conducting InAs substrate. A major concern when patterning narrow fin features in such a material system is the rapid and uncontrolled oxidation of Al-containing layers of Sb-based semiconductors on exposure to ambient conditions (or, worse, oxidizing or etching chemistries) [17]. Furthermore, isolation schemes are somewhat difficult to realize in 6.06 Å N-MOSFET technologies, due to the natural propensity of exposed InAs surfaces to conduct without proper passivation. Although the chosen material system poses tremendous challenges it is the only option to implement defect free InAs fins of relevant height in a top-down etch process due to relaxation of InAs on semi-insulating InP substrate for thicknesses exceeding 4–5 nm.

In this work, we developed and integrated the growth of an etch stop layer for a fin etch, consisting of 7 nm of pseudo-morphically strained InAlAs between the channel and the buffer (Figure 1(a)), without which structural and electrical integrity of the nm-scale InAs fins could not be maintained. A process flow for depositing the high-k dielectric on {100} and {110} InAs surfaces was thus developed. We present successful demonstration of FinFETs with InAs channel and

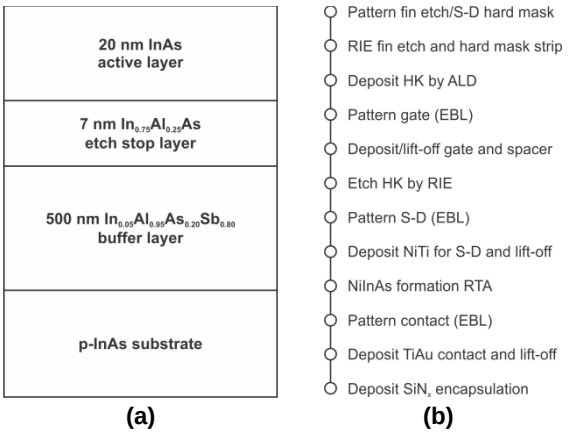

Fig. 1. (a) The layer structure used in this work showing the pseudo-morphic InAlAs etch stop layer and (b) the process flow for the fabrication of InAs FinFETs, starting with the first step after MBE wafer growth.

Manuscript received May 1, 2015

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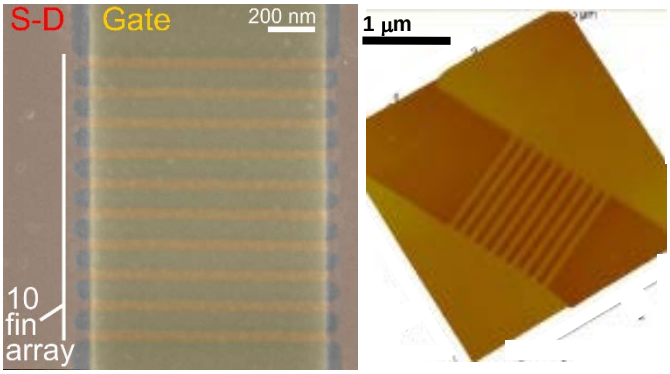

Fig. 2. (a) SEM image of typical InAs FinFET with L_g = 1 μm, showing gate contact, spacer, etched fin array and S-D regions and (b) Data visualization from an AFM scan of the active device area, showing the 10 fin array and the S-D regions.

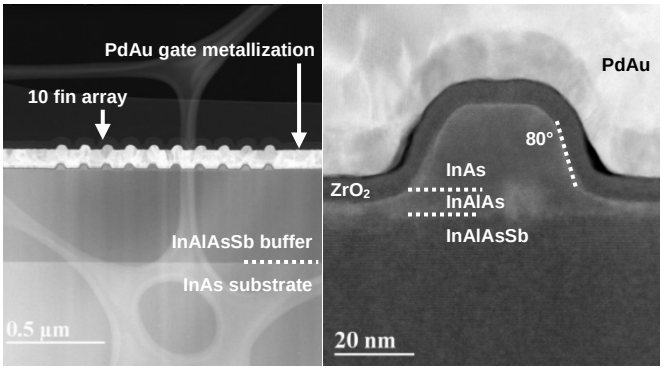

Fig. 3. (a) HAADF TEM cross-section image of typical InAs FinFET with H_{fin} = 20 nm, average W_{fin} = 25 nm and L_g = 1 μm and (b) HAADF TEM cross-section image of a single InAs fin with H_{fin} = 20 nm, W_{fin} = 25 nm, showing InAlAs etch stop layer, InAlAsSb wide bandgap buffer, high-k dielectric and gate metallization. The fin profile sidewall angle is 80°.

H_{fin} = 20 nm, fabricated on lattice-matched epi-layers for low-defectivity channel material and optimum performance. As the first devices of this kind, performance is degraded compared to the scaled and optimized planar technology in [1]. This is primarily due to surface passivation of the fin sidewalls, and process challenges and resulting limitations related to the highly reactive buffer layer, issues which are discussed below.

II. Processing

The layer structure in Figure 1(a) was grown by MBE on a p-doped InAs substrate. A 500 nm thick wide bandgap buffer of lattice matched un-doped $In_{0.05}Al_{0.95}As_{0.20}Sb_{0.80}$ was grown [15] to isolate the 20 nm un-doped InAs active layer, whose thickness ultimately determines the fin height, from the conducting substrate. The quaternary InAlAsSb was employed in preference to the ternary AlAsSb because it presented several improvements: top interface flatness with active layers above it, process and composition repeatability at the epitaxy stage, and increased oxidation resistance. Between the 20 nm InAs active layer and the 500 nm wide bandgap buffer, a pseudo-morphically strained $In_{0.75}Al_{0.25}As$ layer was inserted, the composition of which was chosen to maximize the thickness of the layer while still providing confinement of the carriers at the back side of the fin channel. The active area (fin and S-D regions) was patterned using HSQ resist and electron beam lithography (EBL). An inductively coupled plasma (ICP) CH_4:H_2:Cl_2:O_2 etch process was used to etch the fins, stopping in the InAlAs layer, maintaining acceptable sidewall profile and minimizing HSQ etch mask consumption. In this process step, care was required to avoid exposing the underlying InAlAsSb buffer layer. Following this, the HSQ was removed using a low power SF_6 RIE step. InAs active layer exposed surface preparation was conducted by removing the native oxide before controlled oxygen termination [18] followed by ALD deposition of a 5 nm ZrO_2 layer to form the gate dielectric. A Pd gate metal contact was then defined by EBL of a PMMA bilayer, electron beam evaporation (e-beam) and lift-off. Silicon nitride spacers were then fabricated using an ICP-CVD SiN_x deposition process and an SF_6:N_2 RIE process [19]. The high-k layer was then etched self-aligned to the gate and spacer using a $SiCl_4$ RIE process. Source regions were defined in a two-step process using the scheme described in [15]. First, EBL was used to define NiTi contacts which were annealed to form a low resistivity NiInAs metallic phase. Then, a TiAu contact layer to the NiInAs was defined by EBL and lift-off , Finally a 50 nm SiN_x layer was deposited as encapsulation and to form electrostatically induced extensions by pinning the surface Fermi energy inside the conduction band, thus inducing a sheet charge in the InAs QW. A schematic of the full process flow is shown in Figure 1(b).

III. Results and Discussion

An SEM image of a typical device prior to contact processing is shown in Figure 2(a), where the fins, gate and S-D regions can be seen. The spacer region formed at the edge of the gate metallization is also visible. The AFM scan of Figure 2(b) more clearly shows the 10 fins between the source-drain regions. A TEM cross-section of the intrinsic device is shown in Figure 3. A lower magnification image where the 10 fin array is clearly visible is given in Figure 3(a), showing the PdAu gate metallization, the buffer layer and the substrate. A high magnification image of the cross-section of one fin is shown in Figure 3(b). The InAs fin

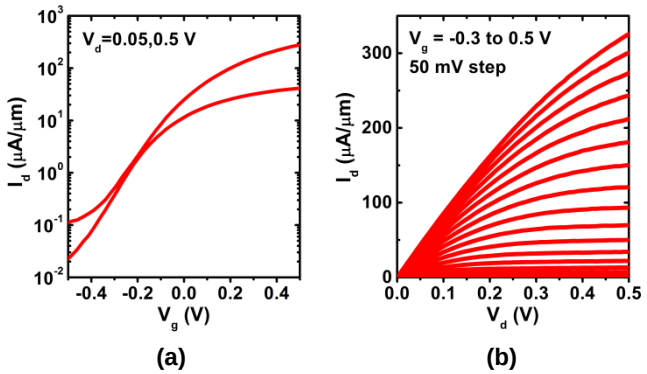

Fig. 4. (a) I_d-V_g of a typical device with L_g = 1 μm, W_{fin} = 25 nm, exhibiting S_{min} = 148 mV/dec and g_m = 650 μS/μm, both at V_d = 0.5 V. (b) I_d-V_d of the same device with V_g = -0.25 V to 0.50 V in steps of 50 mV.

height H_{fin} = 20 nm and average width W_{fin} = 25 nm. Evidence of

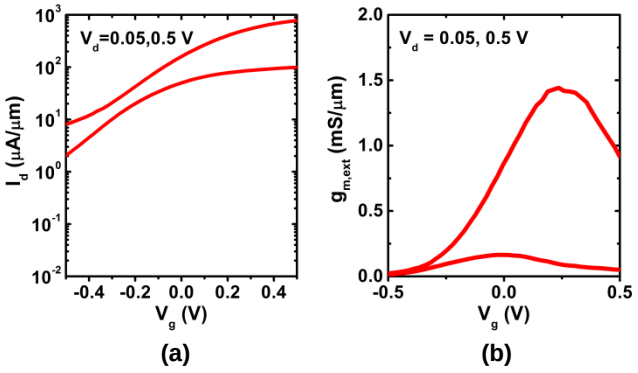

Fig. 5. (a) I_d-V_g of a typical device with L_g = 1 μm, W_{fin} = 35 nm, exhibiting S_{min} = 310 mV/dec and g_m = 1430 μS/μm, both at V_d = 0.5 V. (b) g_m-V_g of the same device.

some over-etch into the InAlAs etch stop layer during fin formation can be seen. A small degree of rounding at the top of the fin suggests partial consumption of the hard mask and the slightly sloping sidewalls are indicative of the trade-off between etch depth control (to stop in the InAlAs layer) and etch process anisotropy [20].

In this study, InAs FinFET devices with fin widths between 25–35 nm were realized. Each device comprised 10 fins, each of which were of height H_{fin} = 20 nm, and the gate length, L_g = 1 μm. The source-drain regions were 3 μm wide, and the length of the un-gated fin extension and source-drain extensions were both 50 nm, giving a total gate-to-source distance of 100 nm. The access resistance of the device (the extrinsic resistance), not accounting for the un-gated fin extensions was measured to be R_{acc} = 230 Ω.μm, based on evaluation of a TLM series of planar structures without gates and without any fin etch between the contacts. For the high-k gate stack, the EOT = 1.2 nm.

Figure 4 shows I_d-V_g at 50 mV and 0.5 V drain bias, and I_d-V_d characteristics of a typical InAs FinFET device with W_{fin} = 25 nm. Data are normalized to the combined perimeter of ten fins, as measured by TEM. Minimum sub-threshold swing S_{min} = 148 mV/dec was observed at V_d = 0.5 V. The minimum measured drain current $I_{d,min}$ = 110 nA/μm, at V_g = -0.5 V. On-resistance R_{on} = 1200 Ω.μm and Q = g_m/S = 4.4 [21]. The gate current is below $2 \cdot 10^{-8}$ A/μm over the entire measurement range. Drain-induced barrier lowering DIBL = 27 mV/V, comparing well with the planar data at similar gate length [1] (30 mV/V).

Figure 5 shows I_d-V_g characteristics of a typical InAs FinFET device with W_{fin} = 35 nm. At V_d = 0.5 V, this device demonstrates minimum sub-threshold swing S_{min} = 310 mV/dec and peak extrinsic g_m = 1430 μS/μm. The minimum measured drain current $I_{d,min}$ = 8 μA/μm, at V_g = -0.5 V. On-resistance for this device R_{on} = 503 Ω.μm and Q = g_m/S = 4.8. The gate current is below $2 \cdot 10^{-8}$ A/μm over the entire measurement range. The off-state degradation in this device is attributed to reduced gate control related to the relaxed fin width and the difference in D_{it} profiles on the {100} and {110} surfaces. The difference between on-state performance of the two devices can be attributed to processing induced effects in the extrinsic source-drain regions. After high-k etch on the narrower fins, some of the conducting volume is lost because of the over-etch required to ensure complete removal of the high-k in the S-D region Thus a higher $g_{m,ext}$ but degraded subthreshold slope is observed in the W_{fin} = 35 nm device and a reduced $g_{m,ext}$ but better subthreshold slope is obtained for the W_{fin} = 25 nm device.

Sub-threshold performance is degraded compared to the planar technology in [1] due to (a) higher D_{it} of the non-optimized high-k interface related to the RIE fin etch process and the {100}, {110} surfaces on the fin, and (b) process challenges and resulting limitations related to the highly reactive buffer layer. On-state performance is degraded compared to the planar technology [1] due to the higher access resistance. For comparison of this work with published state-of-the-art devices, Table I benchmarks key parameters for III-V FinFETs.

TABLE I
BENCHMARK OF III-V FINFET DEVICES

Ref.	InAs mole fraction	H_{fin} (nm)	W_{fin} (nm)	L_g (nm)	g_m (μS/μm)	S (mV/dec)
[7]	0.7	25	50	100	280	190
[8]	0.53	40	40	60	1100	95
[9]	0.53	20	30	80	1800	82
[10]	0.7	10	20	120	1620	114
[11]	0.53	16	40	200	-	150
[12]	0.53[a]	9	40	30	1640	84
This work	**1.0**	**20**	**25** **35**	**1000** **1000**	**650** **1430**	**148** **310**
[1][b]	*1.0*	-	-	*130*	*2720*	*85*

Quoted g_m and S values extracted at V_d = 0.5 V on the same device where given, otherwise not reported.
[a]Mole fraction averaged over total fin height, including InAs quantum well (3 nm) and $In_{0.3}Ga_{0.7}As$ cladding layers (6 nm in total).
[b]Planar device, included for comparison. InAs channel quantum well thickness is 10 nm.

IV. CONCLUSION

We report on the fabrication process flow and results from the first demonstration of an unstrained InAs FinFET with H_{fin} = 20 nm. Measured $g_{m,peak}$ = 1420 μS/μm is comparable to that obtained for planar InAs channel devices [22] with identical L_g = 1 μm and similar EOT (1.2 vs. 1.0 nm) suggesting that electron transport properties such as field effect mobility in fins of dimensions in the 25–35 nm range match planar InAs technology.

ACKNOWLEDGMENT

The authors would like to thank Dr. Y.C. Sun of TSMC for support and the staff of the James Watt Nanofabrication Centre at the University of Glasgow for their fabrication support.

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