A Self-Sufficient Digitally Controlled Ring Oscillator Compensated for Supply Voltage Variation

Mehdi Terosiet, Sylvain Feruglio, Farouk Vallette, Patrick Garda
UPMC Univ. Paris 06, LIP6,
CNRS UMR7606, F-75005, Paris, France
Email: Mehdi.Terosiet@lip6.fr

Olivier Romain
Univ. of Cergy-Pontoise, ETIS,
CNRS UMR8051, F-95014,
Cergy-Pontoise, France

Julien Le Kernec
Kuang-Chi Institute of Advanced Technology
Shenzhen, Guangdong, P.R.China

***Abstract*—A self-sufficient Giga-Hertz digitally controlled ring oscillator for clock distribution network is presented in this paper. It features a high supply insensitivity in order to mitigate the additional jitter due to supply noise. This is achieved by inducing a mutual compensation between the oscillation frequency parameters that are affected by the supply voltage variations. The proposed method can be easily implemented and takes advantage of the deep sub-micrometer effects peculiar to topical CMOS technologies. We demonstrate by simulations that this approach remains efficient over process variations despite the reliability issue of short channel MOS transistors.**

I. Introduction

In modern integrated systems, balanced trees are commonly used to ensure the System-on-Chip (SoC) synchronization. They are implemented with appropriate propagation delays and their complexity increases with the chip dimensions. Moreover, with the continual increase of the operating frequencies, losses in transmission lines poses a severe power consumption problem and both skew and jitter become comparable to a clock cycle which can imply possible computation errors [1].

An alternative to the conventional balanced tree is the active clock distribution network, presented in [2]. It consists to divide the chip in several isochronous zones, each zone has its own local oscillator which is tuned so as to present the same phase as the neighbouring oscillators. In its digital version, nodes of the network use All-Digital Phase-Locked Loops (ADPLL) [3] in order to ensure the synchronization. Thus, the global synchronism is achieved through local synchronizations.

This implementation allows solving the skew issue since clock wires are reduced to the maximal distance in an isochronous zone. However, the high density of digital circuits in topical SoC induces the emergence of switching-noise ($\partial i/\partial t$ noise), IR-Drop, crosstalk and so on [4]. They have a significant impact on local oscillators. Based on ring oscillator topology for their wide tuning range and their compactness [5], their main drawbacks are the high sensitivity to power supply and substrate noises that are the main jitter contributors [6]. Therefore, the clock reliability issue is partially solved but remains dependent on jitter performance.

This paper describes the implementation of a low supply sensitivity Digitally Controlled Oscillator (DCO). The originality of the compensation technique is that it takes advantage of deep sub-micrometer effects, especially the quasi-linear relation between the overdrive voltage and the drain current, peculiar to topical process. Moreover, this technique allows avoiding the use of any extra-circuit (on/off-chip) for dynamic re-calibration [7] and thus, saves more die area.

This article is organized as follows. The second section reviews the I-V model of short channel MOSFETs in order to ease the understanding of the proposed compensation technique. Section III introduces the DCO architecture, details the building blocks and finally, establishes an analytical expression of the oscillation frequency as a function of the input word. Section IV focuses on the supply voltage compensation. In section V, the simulation results of the proposed DCO are presented and compared to some of the most relevant published works. Finally, the last section summarizes and concludes this study.

II. Alpha-power law I-V model

In this section, we introduce the expression of the MOSFET drain current, in the saturation region, that will be used throughout this paper.

The Shockley model fails to reproduce the characteristics of the recent MOS transistors. The drain current is now influenced by short channel effects and has been the subject of several studies [8]–[11]. It is now better described by an alpha-power law model and, according to [11], it can be expressed as

$$I_{ds} = \nu_{sat} W P_s (V_{gs} - V_{th})^{\alpha} \text{ for } V_{ds} > V_{ds\,sat} \quad (1)$$

where ν_{sat} is the saturation velocity, W is the MOSFET width, P_s is a technology-specific constant, V_{gs} is the gate-to-source voltage, V_{th} is the threshold voltage and α is the velocity-saturation index (close to 1 in case of short-channel length transistors).

Thus, the transconductance of a short channel transistor is defined by

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \quad (2)$$

$$g_m = \nu_{sat} W P_s \alpha (V_{gs} - V_{th})^{\alpha - 1} \quad (3)$$

By considering the strong inversion operation and that α is close to 1, it can be approximated by

$$g_m \simeq \nu_{sat} W P_s \quad (4)$$

978-1-4577-1846-5/11/$26.00 ©2011 IEEE

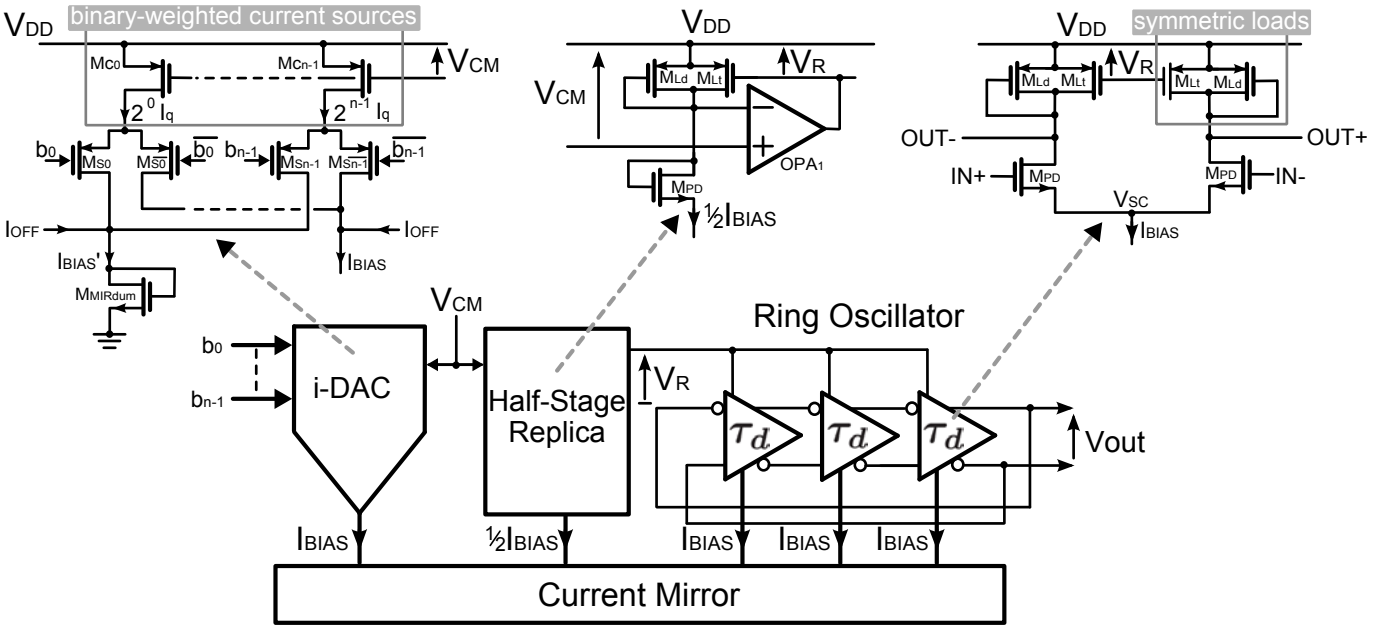

Fig. 1. Structure of the DCO.

III. DCO ARCHITECTURE

Fig. 1 depicts the DCO architecture. The core is the ring oscillator. In order to achieve low supply and substrate sensitivity, it is based upon differential delay stages with symmetric loads [12], [13]. Basically, its oscillation frequency is given by

$$f_{osc} = \frac{1}{2N\tau_d} \tag{5}$$

with

$$\tau_d = \lambda R_{eff} C_{eff} \tag{6}$$

where N is the number of stage and τ_d stands for their time-delay in which, λ is a dimensionless coefficient (close to 1) and R_{eff} and C_{eff} are respectively the stage output resistive and capacitive loads [14].

In order to tune the oscillation frequency, we assume that C_{eff} is invariant and we adjust R_{eff}, the symmetric loads based upon the association of M_{Ld} and M_{Lt}, through the control voltage V_R and the control current I_{BIAS}.

V_R is generated by the half-stage replica which includes an OpAmp (OPA_1). The negative feedback loop, introduced by OPA_1, maintains the voltage V_{CM} across the symmetric loads replica flowed by $I_{BIAS}/2$, by adjusting the gate voltage of M_{Lt}. Thus, the oscillation frequency becomes

$$f_{osc} = \frac{1}{2N\lambda C_{eff}} \frac{I_{BIAS}}{2V_{CM}} \tag{7}$$

where R_{eff} is replaced by $2V_{CM}/I_{BIAS}$.

The control current I_{BIAS} is provided by the high-speed current-steering DAC (i-DAC) [15]. This element is the interface between the digital input word and the oscillator which is an analogue system by nature. In addition to an offset current I_{OFF}, it provides a binary-weighted current to the differential delay stages (and to the half-stage replica) as a function of the input word. According to the state of $b_i/\overline{b_i}$ $(0 < i < n-1)$, steady currents are steered by the differential switch pairs $M_{Si}/M_{\overline{Si}}$ from the current sources M_{Ci} either to the current mirror or to a dummy load M_{MIRdum}. Therefore, the dependence of f_{osc} on the digital input word can be finally expressed by

$$f_{osc} = \frac{1}{4N\lambda C_{eff} V_{CM}} [I_{OFF} + I_q \sum_{i=0}^{n-1} b_i 2^i] \tag{8}$$

Notice that binary-weighted current sources are obtained by applying a binary-weighted aspect ratio on M_{Ci} MOSFETs. As an example, $W_{M_{Cn-1}} = 2^{n-1} W_{M_{C0}}$ for the same channel length.

IV. SUPPLY VOLTAGE COMPENSATION

It is known that differential inverters, associated to the half-stage replica bias circuit, helps to reduce the supply voltage sensitivity [16]. However, it can't be effective if I_{BIAS} and V_{CM} are dependent to V_{DD}. Indeed, by considering that a variation on the supply voltage occurs and by using Eq. (7), the frequency variation can be expressed as

$$\Delta f_{osc} = \frac{1}{4N\lambda C_{eff}} \left[\frac{I_{BIAS} + \Delta I_{BIAS}}{V_{CM} + \Delta V_{CM}} - \frac{I_{BIAS}}{V_{CM}} \right] \tag{9}$$

where ΔI_{BIAS} and ΔV_{CM} are the variations induced by a change of the supply voltage. Then, the condition for Δf_{osc} tends to 0 is

$$\Delta I_{BIAS} V_{CM} - I_{BIAS} \Delta V_{CM} \mapsto 0 \tag{10}$$

By introducing a direct dependence between V_{CM} and I_{BIAS} so that a voltage variation introduces a proportional current variation in the same direction, as in Eq. (11), a mutual compensation can be obtained.

$$\Delta I_{BIAS} = g_{vi} \Delta V_{CM} \tag{11}$$

In Eq. (11), the term g_{vi}, which is introduced to establish the dependence, is equivalent to a transconductance and an efficient

compensation is achieved under the following condition:

$$\Delta f_{osc} = 0, \text{ for } g_{vi} = \frac{I_{BIAS}}{V_{CM}} = \frac{I_{OFF}}{V_{CM}} + \frac{I_q}{V_{CM}} \sum_{i=0}^{n-1} b_i 2^i \quad (12)$$

We propose an implementation of g_{vi} in Fig. 2. V_{CM} is generated by a beta-multiplier reference [17] and biases the binary-weighted current sources, as in Fig. 1, it also biases the p-MOSFET M_{R9} which generates I_{OFF}.

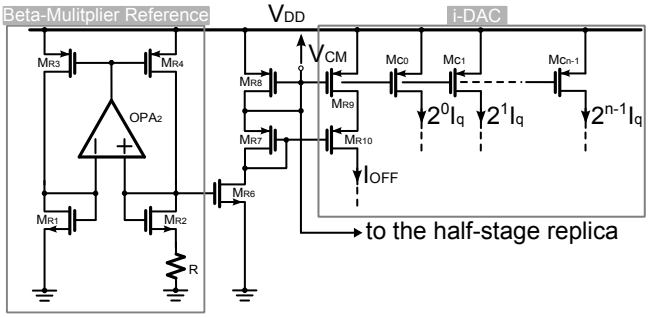

Fig. 2. Circuit which establishes the dependence between V_{CM} and I_{BIAS}.

Therefore, we can express I_{BIAS} as

$$I_{BIAS} = I_{OFF} + I_q \sum_{i=0}^{n-1} b_i 2^i \quad (13)$$

$$= \nu_{sat} P_s (V_{CM} - V_{th})^{\alpha} [W_{R9} + \sum_{i=0}^{n-1} b_i 2^i W_{C0}] \quad (14)$$

By relying on Eq. (4), the effective transconductance of the set M_{R9} and M_{Ci} MOSFETs is

$$g_{vi_{eff}} \simeq \nu_{sat} P_s [W_{R9} + \sum_{i=0}^{n-1} b_i 2^i W_{C0}] \quad (15)$$

Due to the threshold voltage of transistors, compared to the target ideal transconductance of Eq. (12), it remains a residual error, that we call ε, which is given by

$$\varepsilon = g_{vi_{eff}} - g_{vi} \quad (16)$$

$$= \nu_{sat} P_s [W_{R9} + \sum_{i=0}^{n-1} b_i 2^i W_{C0}] \left(\frac{V_{th}}{V_{CM}} \right) \quad (17)$$

ε increases with respect to the input code, however, it can be minimized through the ratio V_{th}/V_{CM}. Furthermore, the high operation frequency and the fine resolution that are some of the most important criteria in DCO designs, imply that W_{C0} will be commonly much smaller than W_{R9}. Consequently, the variation of ε can become significant only when a large number of bits is used.

V. Simulation Results

In this section, we present the implementation details of the DCO for its incorporation into the clock distribution network. Through simulation results obtained with Eldo(-RF) associated to the BSIM4 MOS transistor model, we show its transient operation and check its supply voltage sensitivity with respect to the previous section. Finally we compare the achieved performances to those of the most relevant published works.

The controlled oscillator was implemented in the STMicroelectronics 65nm CMOS process, with the HPA_LP MOS transistors proposed in the Design-Kit and a supply voltage of 1.2 V. The operating frequency range was intended to be from 1.8 to 2.2 GHz with a maximal frequency step of 2 MHz. Hence, in order to stand the process variation issue, it was implemented to operate from 1.6 to 2.6 GHz as it is recommended in [18]. These requirements imposed a number of 9 control bits. The ring oscillator was built with 3 delay stages (e.g. N=3). Finally, to ensure a wide lock-range of ADPLLs (the network nodes), the i-DAC's transfer characteristic must be monotonous. Integral Non-Linearity and Differential Non-Linearity are not really important, since non-linearities are continuously corrected by the feedback loop of the ADPLL [19]. In this way, a segmented implementation of current sources was essential to prevent the non-monotonous risk at the mid-code transition and so as to reduce the glitch energy [20]. Thus, the six MSBs are thermometer-coded while the three LSBs were implemented in a binary-weighted code. Notice that the concept of the compensation technique remains true even if the input word is segmented.

Fig. 3 illustrates the time domain behaviour of the controlled oscillator. The first chronogram is the current I_{BIAS} provided by the i-DAC which is updated at 250 MHz. The second one is V_R, the voltage which controls the symmetric loads. It decreases as I_{BIAS} increases so as to increase the drivability of M_{Lt}. The last one is the output voltage, after a differential-to-single-ended converter (not represented in Fig. 1), as we can see the oscillation frequency increases as a function of the current I_{BIAS}.

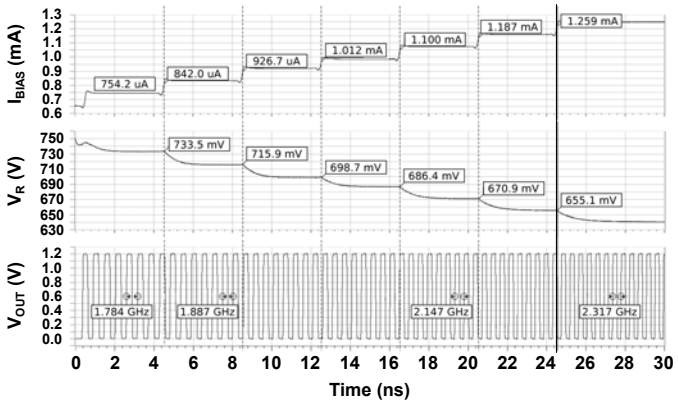

Fig. 3. Transient behaviour of the DCO.

Fig. 4 represents the oscillation frequency as a function of the input word, for a supply voltage equal to 1.0 V, 1.2 V (the nominal value) and 1.4 V. These curves were obtained with a discrepancy of 0.6% of V_{CM} from its nominal value (in Typical condition), for 1.0 V <V_{DD}< 1.4 V and, with W_{R9}/W_{C0}=90. In typical condition, the maximal deviation is about 2.7% on the whole operating range, for V_{DD} =1.0 V, compared to the nominal curve ($TT - V_{DD} = 1.2V$). This demonstrates the efficiency of the supply voltage compensation that we propose.
Moreover, with the process corner curves (SS, TT and FF), it

also shows that the compensation remains effective over process variations, despite the reliability issue of nanometer transistors. The gap between the curve $SS - V_{DD} = 1.0V$ and the two other SS curves is due to the cascode current source I_{OFF} which fails to achieve a high equivalent resistance in these conditions.

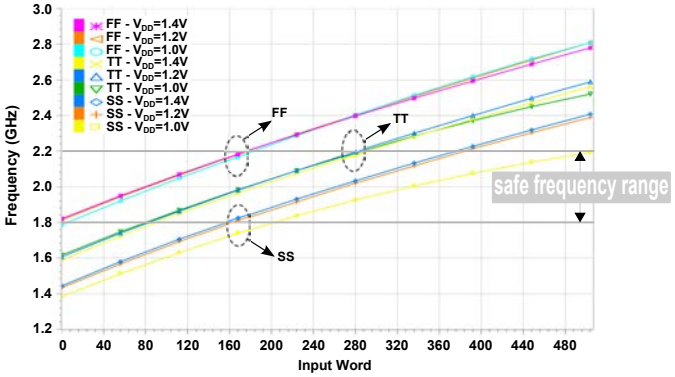

Fig. 4. Simulated characteristics of the DCO, for 1.0 V < V_{DD} < 1.4, in typical and worst cases.

In order to evaluate the suitability of our proposal with respect to the supply sensitivity issue, we established a performance comparison with some of the most relevant implementations of the state of the art. It is summarized in Table I.

TABLE I
PERFORMANCES COMPARISON WITH PRIOR STATE OF THE ART DESIGNS

	[21] (measurement)	[22] (measurement)	This work (simulation)
Technology	130 nm	90 nm	65 nm
Supply Voltage	1.2 V	1.2 V	1.2 V
Frequency (GHz)	0.3-1.3	0.18-0.6	1.8-2.2
Supply Sensitivity : $(\Delta f/f)/(\Delta V_{DD}/V_{DD})$	0.48	0.2	0.38

It is worth to say that we compared our simulation results to the measurements made in [21], [22]. Thus, to be fair, we report in Table I our worst supply sensitivity ($(\Delta f/f)/(\Delta V_{DD}/V_{DD})$) which was obtained for the curve $SS - V_{DD} = 1.0V$ with an input code equal to 511, the curve $TT - V_{DD} = 1.2V$ was taken as the reference. The supply sensitivity in [21] and [22] were measured respectively for 1.0 V < V_{DD} < 1.4 V and a variation of 5% on a 1.8 V nominal supply voltage.
Notice that in TT condition, our simulated supply sensitivity is less than 0.1 within 1.0 V < V_{DD} < 1.4 V.

VI. Conclusion

We propose an original approach to enhance the robustness of digitally controlled ring oscillators with respect to the supply voltage sensitivity. This approach takes advantage of the short channel effects exhibited by the topical MOS transistors and offers the benefit to be easily implemented. Thence, a self-sufficient digitally controlled ring oscillator was implemented in the STMicroelectronics 65nm CMOS process. It is controlled by 9 bits and operates from 1.6 GHz to 2.6 GHz. It achieves a supply sensitivity less than 0.1 on the whole range, for a supply voltage ranging from 1.0 V to 1.4 V. In addition, the supply sensitivity of about 0.38 over process variations demonstrates the efficiency of our proposal.

VII. Acknowledgment

This work is supported by the French National Agency of Research (ANR) through the HODISS project, directed by D. Galayko.

References

[1] W. Ryu et al. Over GHz Low-Power RF Clock Distribution for a Multiprocessor Digital System. *IEEE Trans. on Advanced Packaging*, vol. 25 issue 1:pp. 18–27, 2002.
[2] V. Gutnik et al. Active GHz Clock Network Using Distributed PLLs. *IEEE J. of Solid-State Circuits*, vol. 35 issue 11:pp. 1553–1560, 2000.
[3] R.B. Staszewski et al. Digitally Controlled Oscillator (DCO)-Based Architecture for RF Frequency Synthesis in a Deep-Submicrometer CMOS Process. *IEEE Trans. on Circuits And Systems - II*, vol. 50 issue 11:pp. 815–828, 2008.
[4] O. Valorge et al. A Simple Way for Substrate Noise Modelling in Mixed-Signal ICs. *IEEE Trans. on Circuits And Systems - I*, vol. 53 issue 10:pp. 2167–2177, 2006.
[5] T. Miyazaki et al. A Performance Comparison of PLLs for Clock Generation Using Ring Oscillator VCO and LC Oscillator in a Digital CMOS Process. *IEEE Asian and South-Pacific Design Automation Conf.*, -:pp. 545–546, 2004.
[6] F. Herzel et. al. A Study of Oscillator Jitter due to Supply and Substrate Noise. *IEEE Transaction on Circuits And Systems - II*, volume 46 issue 1:pp. 56–62, 1999.
[7] H.S. Jeon et al. Fast Frequency Acquisition All-Digital PLL Using PVT Calibration. *IEEE Int. Symp. on Circuits And Systems*, -:pp. 2625–2628, 2008.
[8] T. Sakurai. Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas. *IEEE J. of Solid-State Circuits*, vol. 25 issue 2:pp. 584–594, 1990.
[9] W.S. Lau. An Explanation of the Dependence of the Effective Saturation Velocity on Gate Voltage in Sub-0.1 um Metal-Oxide-Semiconductor Transistors by Quasi-Ballistic Transport Theory. *Elsevier - Microelectronics Reliability*, vol. 48:pp. 1641–1648, 2008.
[10] J. Rabaey. *Low Power Design Essantials*. Springer, 2009.
[11] J.C. Ku et. al. On the Scaling of Temperature-Dependent Effects. *IEEE Trans. on Computer-Aided Design of Integrated Circuits And Systems*, vol. 26 issue 10:pp. 1882–1888, 2007.
[12] J.G. Maneatis. Low-Jitter Process-Independent DLL and PLL based on Self-Biased Techniques. *IEEE J. of Solid-State Circuits*, vol. 31 issue 11:pp. 1723–1732, 1996.
[13] V. Kratyuk et. al. Analysis of Supply and Ground Noise Sensitivity in Ring and LC Oscillators. *IEEE Int. Symp. on Circuits And Systems*, vol. 6:pp.5986–5989, 2005.
[14] S. Docking et al. A Method to Derive an Equation for the Oscillation Frequency of a Ring Oscillator. *IEEE Trans. on Circuits And Systems - I*, vol. 50 issue 2:pp. 259–264, 2003.
[15] A. Van Den Bosch et al. A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter. *IEEE Journal of Solid-State Circuits*, volume 36 issue 3:pp. 315–324, 2001.
[16] J. Carnes et. al. Design and Analysis of Noise Tolerant Ring Oscillators Using Maneatis Delay Cells. *IEEE Int. Conf. on Electronics, Circuits And Systems*, -:pp.494–497, 2007.
[17] F. Maloberti. *Analog Design for CMOS VLSI Systems*. Kluwer Academic Publihers, 2001.
[18] B. Razavi. A Study of Phase Noise in CMOS Oscillators. *IEEE J. of Solid-State Circuits*, vol. 31 issue 3:pp. 331–343, 1996.
[19] I.C. Hwang et. al. A Digitally Controlled Phase-Locked Loop with a Digital Phase-Frequency Detector for Fast Acquisition. *IEEE J. of Solid-State Circuits*, vol. 36 issue 10:pp. 1574–1580, 2001.
[20] A. Rodriquez-Vasquez et al. *CMOS Telecom Data Converters*. Kluwer Academic Publishers, 2003.
[21] B.M. Moon et al. Monotonic Wide-Range Digitally Controlled Oscillator Compensated for Supply Voltage Variation. *IEEE Trans. on Circuits And Systems - II*, vol. 55 issue 10:pp. 1036–1010, 2008.
[22] J. Lin et al. A PVT Tolerant 0.18 MHz to 600 MHz Self-Calibrated Digital PLL in 90 nm CMOS Process. *IEEE Int. Solid-State Circuits Conf.*, vol. 1:pp. 488–541, 2004.