Monolithic Integration of an Active InSb-Based Mid-Infrared Photo-Pixel with a GaAs MESFET

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***Abstract*— Medium wavelength infrared detectors are of increasing importance in defense, security, commercial and environmental applications. Enhanced integration will lead to greater resolution and lower cost focal plane arrays. We present the monolithic fabrication of an active photo-pixel made in InSb on a GaAs substrate that is suitable for large-scale integration into a focal plane array. Pixel addressing is provided by the co-integration of a GaAs MESFET with an InSb photodiode. Pixel fabrication was achieved by developing novel materials and process steps including isolation etches, a gate recess etch and low temperature processes to make Ohmic contacts to both the GaAs and InSb devices. Detailed electrical and optical measurements in an FTIR demonstrated that the photodiode was sensitive to radiation in the 3 to 5 μm range at room temperature, and that the device could be isolated from its contacts using the integrated MESFET. This heterogeneous technology creates great potential to realize a new type of monolithic focal plane array of addressable pixels for imaging in the medium wavelength infrared range.**

***Index Terms*—Monolithic integration, medium wavelength infrared photodetector, GaAs, InSb, imaging, focal plane array.**

I. Introduction

Medium wavelength infrared (MWIR) or mid-IR detection technologies have a wide range of applications in gas sensing, security, defense, medical diagnosis, environmental and astronomical observations [1]. Antimonide-based semiconductors such as InSb, InAlSb, InAsSb and type-II InAs/GaSb superlattices are especially suitable for achieving high performance MWIR photodetectors due to their small band gap or unique band-structure alignments [2-4]. In order to make an imaging device, such as a focal plane array (FPA), it is required that the photodiodes must be individually addressable using row and column decoding. For imaging at visible wavelengths this can be readily achieved by integration of silicon photodiodes and switching MOSFETS in a complementary metal oxide semiconductor (CMOS) process to form arrays of active pixels [5]. FPAs working in the MWIR require the integration of a small band gap semiconductor array of isolated photodiodes with a separate CMOS addressing chip known as a read-out integrated circuit (ROIC). Each photodiode must be individually connected to its own addressing circuit on the ROIC [6]. In order to make one-to-one connections between each photodiode and the addressing circuit on the ROIC, flip-chip bonding is used. Although this method has successfully produced large format FPAs, flip-chip bonding remains a difficult technology to scale when larger arrays of smaller pixels are desired for high resolution cameras at lower cost. The interconnections (indium bump bonds) and substrate alignment will both become more challenging. Furthermore, because of the large thermal expansion mismatch between the III-V and silicon chips, the resulting devices may only withstand a narrow range of operation and storage temperatures. If not carefully suppressed, considerable stress would be applied to the indium bumps during thermal cycles resulting in the possibility of connection failure [7]. Substrate thinning is a possible method to decrease the thermal mismatch [6], but at the expense of fabrication complexity.

Recently, antimonide-based photodetectors have been grown on a GaAs substrate by molecular beam epitaxy (MBE) and reported to have comparable performance to the devices grown on more expensive InSb and GaSb substrates [8-10]. In addition to providing a cost saving substrate, GaAs can be used as a functional material to fabricate transistors and realize an addressing circuit for the photodetectors. Although InSb-based transistors have been demonstrated [11], it is challenging to implement a device that can be fully turned off, therefore the GaAs MESFET is required to make an addressable pixel. Some similar designs where InAs photodiodes and InGaAs laser diodes were monolithically integrated with a GaAs MESFET have already been demonstrated [12, 13]. However, these devices are only suitable for use in the near and short wavelength infrared (SWIR) range (< 3 μm), and require

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complex regrowth technology. Antimonide-based photodetectors, which are sensitive in the MWIR range, have never been successfully integrated with GaAs MESFETs before. Several challenges must be overcome to make such a device system possible.

In this work we require to make a MESFET adjacent to an InSb photodetector on a heterogeneous semiconductor substrate in order to form an active switchable pixel. The pixel architecture that we have successfully demonstrated is illustrated in Fig. 1. As can be seen in Fig. 1 several etches are required in order to: define the photodiode; expose the MESFET device layers; define the MESFET mesa; and form the MESFET gate recess. Furthermore, two distinct Ohmic contact methods are required to make the photodiode and the MESFET. All of the process steps must be achieved without exceeding a temperature of approximately 200 ˚C since antimony desorption will damage the device at higher temperatures [14, 15]. In order to make this possible we developed Ohmic contact structures suitable for low temperature annealing on a heterogeneous substrate. Electrical and optical characterization of the final integrated pixel device confirms the possibility of monolithic integration of GaAs based read-out circuits with InSb-based MWIR detectors.

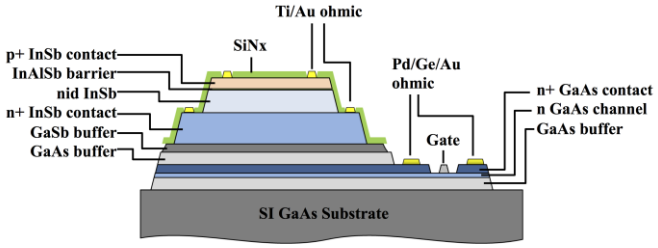

Fig. 1. A sketch of the cross-section of the monolithically fabricated GaAs MESFET and InSb MWIR detector (not to scale).

Section II of this paper describes the layer structure of the integrated wafer and the device fabrication processes. Section III presents the characterization results of the pixel elements, MESFET I-V characteristics and the DC behavior of the InSb photodiode. The switching performance of the integrated pixel device was also evaluated in response to IR illumination. Conclusions from the work to date are presented in Section IV.

II. DEVICE FABRICATION

The layer structure used for this study was grown on a 3-inch semi-insulating (SI) GaAs substrate by MBE. Using a SI-GaAs substrate, a 500 nm thick undoped GaAs buffer layer, followed by a 200 nm thick Si doped GaAs channel layer with a donor density (N_D) of 1×10^{17} cm^{-3} was grown. A 300 nm thick layer of GaAs with $N_D = 2\times10^{18}$ cm^{-3} was grown as a contact layer. A further 500 nm thick undoped GaAs buffer layer was grown to separate the MESFET active layers from the antimonide-based materials. In order to ease the large lattice mismatch (14.6 %) between GaAs and InSb, a 300 nm undoped GaSb buffer layer was then grown to allow relaxation of the strain. Photodetector performance is strongly reliant on successfully mitigating lattice mismatch and the relaxation layer is critical to producing low defect density in the subsequently grown InSb layers. These details are shown in Fig. 2. Finally as shown in Fig. 1, a non-equilibrium InSb photodiode structure was grown including a 3 µm thick Te doped n+ contact layer, a 2.5 µm thick non-intentionally doped absorption layer, a 20 nm $In_{0.15}Al_{0.85}Sb$ barrier layer and a 500 nm thick Be doped p+ contact layer. The barrier layer between the p+ and the absorption layer was grown since it has been reported to block the flow of electrons between the two layers, therefore reducing the diode leakage and allowing operation at higher temperature [16]. The n-contact layer of the InSb photodiode was chosen to be 3 µm thick in order to further reduce the number of defects and threading dislocations, that tend to appear much more frequently near to the interface between the GaSb buffer and the InSb [17].

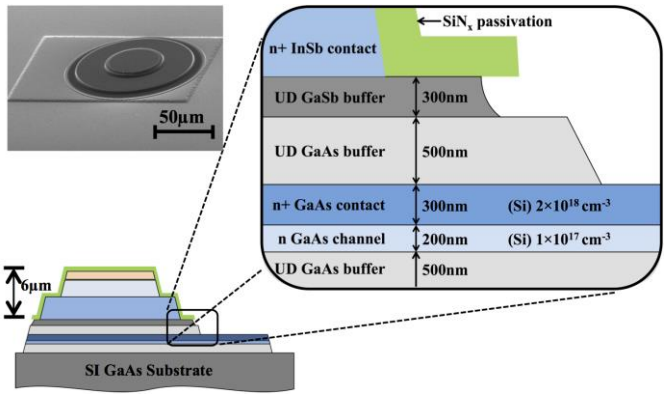

Fig. 2. Schematic diagram and scanning electron micrograph of a device after buffer layer etching and mesa isolation.

The InSb materials were etched using a citric acid – hydrogen peroxide etchant (33:2:80 $C_6H_8O_7$:H_2O_2:H_2O by weight) to define the 45 µm diameter active area of the InSb photodiode at a rate of 20 nm/min. A photolithographic mask was used. Owing to its low etch rate (< 1nm/min) in the etchant, the GaSb buffer was used as an etch-stop layer permitting separate definition of the MESFET. The defined photodiode mesas were then passivated using low temperature inductively coupled plasma (ICP) deposited SiN_x.

In order to make the MESFET, the SiN_x passivation layer also functioned as a mask for GaSb buffer etching. Electron beam lithography (EBL - suitable for process prototyping) and PMMA resist was used to define the mask pattern. The SiN_x was etched using SF_6 in an Oxford-instruments System 100 RIE machine. We then used standard photoresist developer (Microposit MF-319) to etch the GaSb. The MF-319 does not etch GaAs hence the etch stopped uniformly above the MESFET device layers.

300 nm thick MicroChem polymethylglutarimide (PMGI) resist was then coated on the samples. After EBL and resist development, the samples were placed into a 13:1:156 orthophosphoric acid:H_2O_2:H_2O, by weight, solution to etch the GaAs buffer layer and reach the heavily n-type doped contact layer of the MESFET. In a further mask step, PMGI resist and the same etchant were then used for the mesa isolation of the

MESFET. Fig. 2 shows the cross-sectional view of a typical sample, illustrating the etch profiles that were obtained.

Having completed these etches for exposing the MESFET layer and device isolation of the photodiode and the MESFET, it was then necessary to form Ohmic contacts to both the photodiode and the MESFET. As already described, low resistance Ohmic contacts for the GaAs MESFET must be made by annealing at a temperature that is low enough to avoid degradation of the photodiode. A summary of the annealing temperature and electrical results for typical contact materials on GaAs is given in Table I.

TABLE I
SUMMARY OF OHMIC CONTACT DATA

Metallization	Anneal Temp (℃)	Resistivity (Ω cm²)	Ref
Ni/AuGe	>360	$<1 \times 10^{-6}$	[18]
Ge/Ni/Al	500	1.4×10^{-6}	[19]
Cu/Ge	400	6.5×10^{-7}	[20]
Pd/Ge	250-325	0.8×10^{-6}	[21]
Pd/Ge/Au	150-175	1×10^{-6}	[22]

Clearly, Pd/Ge/Au is currently the only reported metallization system that can achieve good Ohmic behavior for an annealing temperature below 200℃. Although this Ohmic contact system has been applied to the fabrication of devices such as heterojunction bipolar transistors (HBT) and solar cells [23, 24], no attempt at using the process in conjunction with an antimonide-based device has been made.

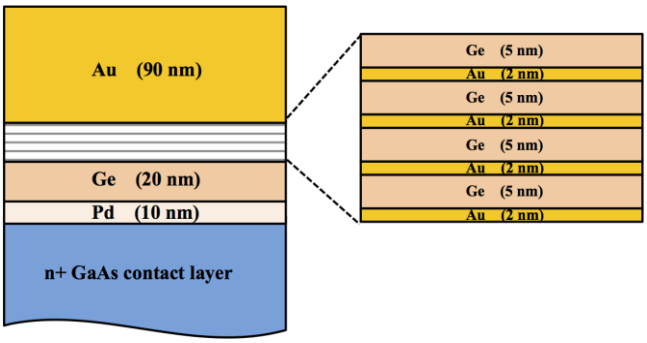

Fig. 3. A schematic diagram of the metallization system used for Ohmic contact formation. The diagram on the right is an expanded view of the Au/Ge stack that was incorporated.

In this work a superlattice-like Au/Ge stack layer was inserted into the Pd/Ge/Au contact layer structure as shown in Fig. 3. Using this method the interdiffusion of Au and Ge could be optimized more precisely by adjusting the relative thickness of the Au and Ge layers in the Au/Ge stack. The layer thicknesses that we used are shown in Fig. 3.

The Ohmic contact patterns for the source and drain of the MESFET device were defined using EBL and a bi-layer PMMA process optimized for metal lift-off. A short O_2 plasma ash was used to remove any PMMA residue after resist development. Prior to metal evaporation the GaAs native oxide was removed by dipping the sample into 1:4 HCl:H_2O, by weight, followed by a DI water rinse. The Ohmic contact metals were then deposited by evaporation and the source and drain contacts to the MESFET were formed by lift-off.

We annealed the MESFET contacts at 180 ˚C. At this low temperature it is possible to use a conventional laboratory oven such as would be used for pre-baking resists. Previous work [22] carried out the annealing in an inert gas (nitrogen). Since we do not have a suitable oven to control the gas environment, we developed an alternative method that gave consistent Ohmic contact performance and simultaneously prepared the resists for the next lithography stage.

Approximately 900 nm thick MicroChem LOR 10A resist was spun on the sample (see Fig. 4a). The sample was then baked in a 180 ℃ oven for 1hr which had the dual purpose of annealing the Ohmic contacts and pre-baking the resist. The LOR 10A was not removed, but rather was retained as the first layer of a bi-layer resist process that was used for MESFET gate formation. The same bi-layer PMMA resist that was used for the Ohmic contact metallization was then coated on to the LOR 10A layer. The PMMA layers are each baked for only 5 minutes at 180 ˚C, further contributing to the overall thermal budget of the contact anneal. The resistivity of the contacts was independently assessed using a circular transmission line model pattern [25]. A resistivity of approximately 2×10^{-6} Ω cm^2 was achieved.

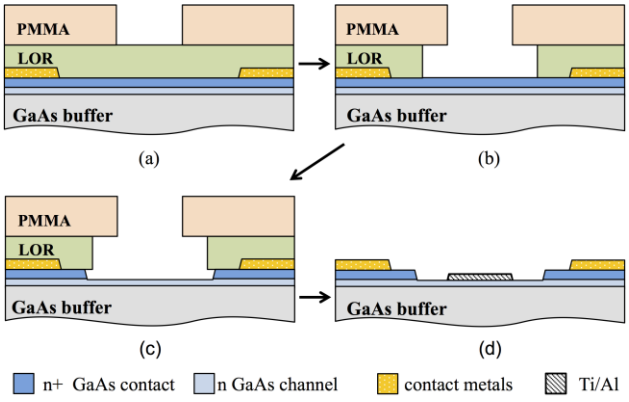

Fig. 4. An illustration of LOR/PMMA gate recess resist, etch and metallization technology. (a) PMMA development (b) LOR development (c) Gate recess etch (d) metallization and lift-off.

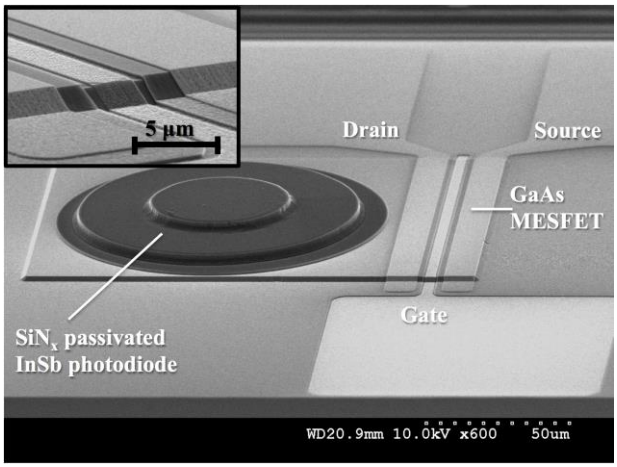

Fig. 5. A scanning electron micrograph of the fabricated MESFET with 3 µm gate length and 100 µm width.

The MESFET gate was then written using EBL. The combination of the LOR 10A and PMMA gives rise to a considerable undercut as shown in Fig. 4 (the smaller undercut in the two PMMA layers is not shown). Two development stages were required: standard MIBK:IPA for the PMMA and then MF-319 for the LOR 10A. Gate recess etching was then carried out using a 30:1:33, by weight, $C_6H_8O_7$:H_2O_2:H_2O citric acid etch. Since the recess etch requires precision in order to land on the channel layer, an iterative approach was used. The current flow through drain and source pads was monitored using a probe station after each iteration until the measured saturation current reached approximately 30 mA saturation current at V_{ds} = 3 V, at which it was determined that the highly doped contact layer was removed. Finally, in this self-aligned gate process, 20 nm of Ti and 100 nm Al was evaporated then lifted off in Microposit 1165 stripper to form the Schottky gate of MESFET. Fig. 5 shows a scanning electron micrograph (SEM) of the fabricated MESFET. The MESFET dimensions were 3 µm long by 100 µm wide.

After completion of the MESFET, Ohmic contacts were made on the InSb photodiode. After a lithographic step windows were etched into the SiN_x passivation layer using the same SF_6 plasma etch as described previously. The contact metals were composed of 20 nm Ti and 100 nm of Au. No anneal was needed.

The final fabrication step was used to form interconnects between the MESFET and the photodiode. Since there is a considerable etch step (> 6 µm) that metal must straddle without breaking, we developed an intermediate step using polyimide to provide a smoothing section between the lower MESFET and upper photodiode regions of the device. 2 µm of Dupont PI-2545 polyimide was spin-cast on to the sample. The polyimide provided a continuous gentle ramping region at the etch step edge. Via holes through the polyimide were then made where connections were required using PMMA, EBL and a MF-319 etch. An interconnection mask was then defined using a bi-layer of PMMA and EBL, followed by evaporation of 300 nm Au and lift-off. Fig. 6a shows a micrograph of the completed circuit. The circuit diagram is shown in Fig. 6b.

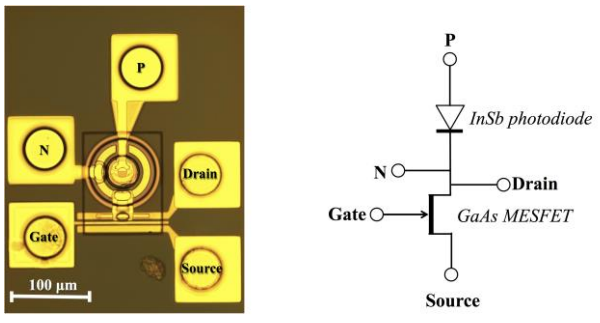

Fig. 6. (a) An optical micrograph and (b) equivalent circuit diagram of an integrated photo-pixel device.

III. Results and Discussion

For test purposes, each pixel has several test-point pads so that the MESFET and the photodiode could be independently probed. These pads would not be present in a fully fabricated array. In each test pixel, there are five metal pads: P, N, Gate, Drain and Source. Note that in the complete circuit the nodes Drain and N are short-circuited by the metal interconnection.

An Agilent 4155C semiconductor analyzer was used to characterize the DC behavior of the MESFET. Fig. 7 shows the I-V characteristics of a typical fabricated MESFET with 3 µm gate length and 100 µm width. The transistor shows a maximum saturation current of approximately 18 mA for V_{ds} > 1.5 V with V_{gs} = 0 V. V_{gs} = -3.5 V is required to pinch-off the channel and turn off the transistor. The transconductance as a function of applied gate voltage is shown in Fig. 8 for several voltages applied between drain and source V_{ds}. The results are comparable to the previously published GaAs MESFET with similar gate length and channel doping level [26].

Since InSb MWIR detectors are generally zero biased or reverse biased with a small voltage, normally less than 300 mV, the MESFET will operate in the linear region when integrated with the photodiode. Fig. 8 also shows the drain-source resistance of the fabricated MESFET as a function of V_{gs} with V_{ds} = 0.1 V. The transistor shows an ON/OFF resistance ratio up to 10^6 with a resistance that varies from 50 Ω in the ON state to a maximum of approximately 50 MΩ in the OFF state. This large variation in transistor output resistance shows consistent results with the reported GaAs MESFET switching device used for an InGaAs detector array [27].

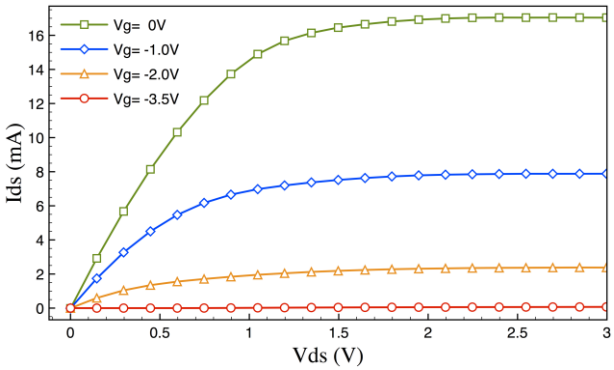

Fig. 7. The current–voltage (I_{ds} –V_{ds}) characteristics of the fabricated MESFET.

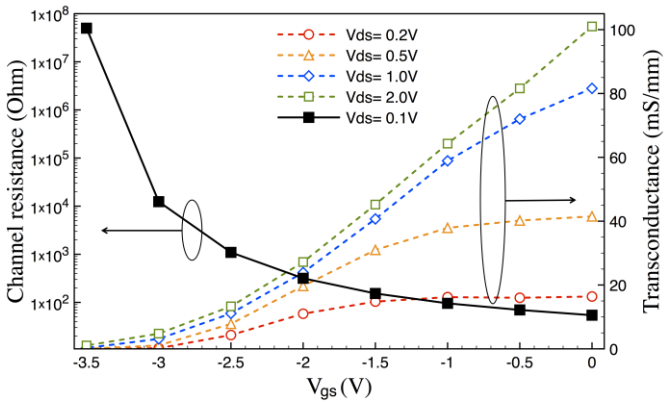

Fig. 8. The MESFET drain-source resistance and transconductance as a function of V_{gs}.

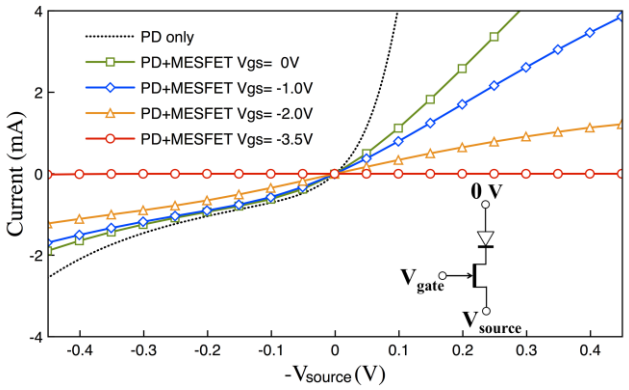

Fig. 9. The current–voltage characteristics of a photo-pixel device with a 45 µm diameter circular InSb photodiode.

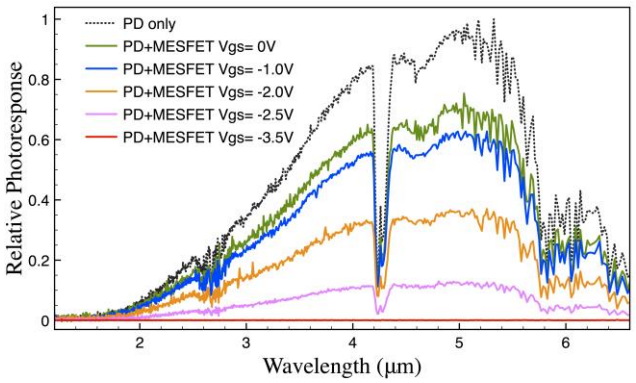

Fig. 10. The relative spectral response of the photo-pixel device under various gate bias conditions.

I-V curves for the InSb non-equilibrium photodiode, by itself, at room temperature were obtained by measuring the current through the two pads labeled P and N in Fig. 6. As shown in Fig. 9 in the "PD only" curve, a circular InSb photodiode with 45 µm diameter shows a rectifying behavior. The high reverse leakage current is commonly observed in InSb detectors because of the large number of thermally excited carriers across the band gap that is only 0.17 eV. The zero bias "resistance.area" product (R_0A) is a known figure of merit for photodiodes, with a higher value indicating a better device. The R_0A product, with no MESFET in series, obtained in this study is $1.2\times10^{-3}\ \Omega\ cm^2$. Previously published work on InSb photodiodes grown on GaAs substrates yielded values of $0.46\times10^{-3}\ \Omega\ cm^2$ for a 30 µm diameter circular diode fabricated on an epi-structure without a barrier layer [28]. A higher value of $0.92\times10^{-3}\ \Omega\ cm^2$ was reported for a 14.5 µm square diode fabricated on a structure where a barrier layer was introduced [29]. InSb photodiodes grown on InSb (100) substrate produced R_0A values, at room temperature of approximately $1\times10^{-3}\ \Omega\ cm^2$[30]. Thus, the performance of our InSb photodiode is comparable with results obtained from devices grown on InSb substrates and better than previously reported results for InSb PDs grown on GaAs substrates. The data also supports the choice of a p+ barrier between contact and absorption regions in the present work.

The complete photo-pixel device containing both the photodiode and the MESFET was characterized by measuring the current flow between the pad P and the MESFET source as a function of the gate-source voltage, V_{gs}. The pad P of the MESFET was connected to signal ground which was 0 V, as shown in the inset circuit diagram of Fig. 9. The voltage labeled V_{source} was swept from 0.5 V to -0.5 V, with $V_{gs} = 0$ V using the Agilent 4155C semiconductor parameter analyzer. In forward bias, the MESFET dominates the I-V characteristic since the resistance of the photodiode is much smaller than that of the MESFET ON resistance that is approximately 50 Ω. However, when the pixel is reverse biased, the photodiode resistance is greater than the MESFET ON resistance and the pixel I-V characteristic follows the photodiode only I-V curve, showing a rectifying behavior. When V_{gs} is decreased so that the transistor turns off, the I-V characteristic, as can be seen in Fig. 9, shows a fall in the current as V_{source} is swept. A residual current of a few nanoAmps is measured. As observed from the characterization of the MESFET alone, a V_{gs} of -3.5 V is required to switch off the photo-pixel circuit.

Having satisfied ourselves that the MESFET was capable of turning off the pixel, we then measured the detected photo-response of the circuit under illumination. A Bruker Vertex 70 FTIR spectrometer was used to measure the relative photo-response of the photo-pixel device. The measurement was done at room temperature and standard atmosphere. Fig. 10 shows several scan results obtained from same photo-pixel device for various values of V_{gs}. No voltage was applied between pad P and the source of the transistor (zero bias). The spectra we obtained spanned the wavelength range from 1.3 µm to 6.7 µm. The photo-response was detected using a current preamplifier connected to the node V_{source}. The peak in the response was at 5.1 µm with a full width at half maximum (FWHM) of 2.6 µm, which is consistent with results from InSb photodiodes operating at room temperature [29]. The sudden drop of the curve at approximately 4.2 µm is because of the absorption caused by CO_2 in the atmosphere. The less obvious signal drop at 2.6 µm and 5.8 µm are attributed to water absorption. The measured photo-response decreases in amplitude as the V_{gs} of the MESFET is reduced. When approaching the pinch-off point of the MESFET, the photo-response is eliminated. As a result, the entire pixel is turned off and isolated. These results are consistent with the data that we took for the MESFET and the photodiode in isolation, with the transistor effectively controlling the flow of photo-generated carriers in the circuit.

IV. Conclusion

For the first time, a monolithically integrated active photo-pixel for use in the MWIR has been demonstrated. The device hybridizes an InSb photodiode that is sensitive in the MWIR with a GaAs MESFET. The device that we present is based on the heterogeneous growth of GaAs MESFET and InSb photodiode device layers on a SI GaAs substrate. Successive process steps permit independent fabrication of the two devices side-by-side on the surface of the sample, and their interconnection, to form a complete pixel circuit. In order to make this device integration possible we developed a number of new processing steps, including a low temperature Ohmic

contact process to the GaAs MESFET so that no damage was observed in the InSb device layers.

The MESFET showed excellent switching behavior with an ON resistance of as little as 50 Ω and an ON/OFF resistance ratio of 10^6. The photodiode showed typical sensitivity for an InSb device in the 1.3 μm to 6.7 μm wavelength range, with the absorption spectra for atmospheric CO_2 and H_2O clearly visible at room temperature. These characteristics were demonstrated in the completed pixel circuit.

Using a device such as the new photo-pixel that has been demonstrated in this work we anticipate that it will be possible to fabricate large scalable focal plane arrays without the need for flip-chip bonding to a ROIC. Future work will enable the demonstration of a working array and circuit, and investigate the industrial feasibility of the technique, with particular attention to power budget and costs. The SI GaAs substrate method used in this work is suitable for the growth of a number of III-V materials with mid-IR detecting capabilities, therefore alternative semiconductor layer structures could also be investigated for use at room temperature or below.

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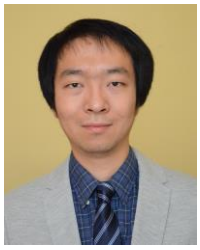

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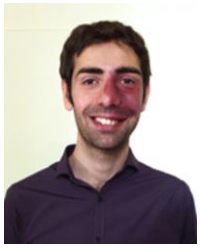

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