RF Operation of Hydrogen-Terminated Diamond Field Effect Transistors: A Comparative Study

Stephen Russell, Salah Sharabi, Alexandre Tallaire, and David A. J. Moran

***Abstract*— Three sets of different gate-length field-effect transistors (250, 120, and 50 nm) have been defined on homoepitaxial hydrogen-terminated diamond with the 50-nm device being the smallest gate length diamond transistor fabricated to date. DC- and small-signal RF measurements were undertaken to compare the operation of these gate nodes. RF small-signal equivalent circuits were generated to contrast individual components and better understand the operation at various gate dimensions. Scaling the gate length to smaller dimensions leads to an increase in the cutoff frequency of these devices although parasitic elements are found to dominate at the shortest gate length of 50 nm, limiting the outstanding potential of these devices.**

***Index Terms*— Field-effect transistor (FET), homoepitaxial diamond, hydrogen terminated, RF performance.**

I. Introduction

DIAMOND possesses several intrinsic material properties that would make it an ideal substrate for high-power RF electronic devices. Its wide bandgap (5.47 eV), high intrinsic breakdown field (predicted to be >10 MV/cm), and high thermal conductivity (>20 W/cm · K) allow for high-power operation with suitable means to distribute heat away from devices [1]. High intrinsic electron and hole mobility (3800 and 4500 $cm^2/V \cdot s$, respectively) also suggest the potential for high-frequency operation [2]. Doping of diamond has proved to be challenging however. Conventional methods such as ion implantation and diffusion are yet to yield a substitutional dopant capable of high levels of carrier activation with reasonable mobility at room temperature. An alternative method employing a quasi-2-D hole gas made possible by hydrogen termination of the diamond surface has been utilized by several groups over the last two decades to produce p-type diamond field-effect transistors (FETs) [3]–[9]. The highest cutoff frequency yet achieved for this technology of 53 GHz was recently demonstrated by Russell *et al.* [10] for a 50-nm gate length L_g hydrogen-terminated diamond FET that utilizes this doping strategy.

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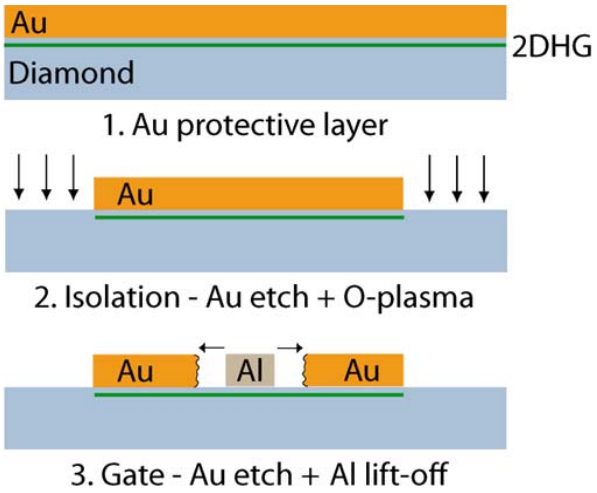

Fig. 1. Process flow of the device fabrication.

Several adverse effects upon device performance have previously been observed when scaling the L_g of H-terminated diamond FETs to these short dimensions. These include issues with access resistance becoming dominant, output conductance being increased, and shifting of the threshold voltage [10], [11]. This paper demonstrates and discusses the effect of scaling to sub-300-nm dimensions by the comparison of three gate nodes (250, 120, and 50 nm) and comparing both the dc and RF performance of each.

II. Experiment

The FET devices in this paper were produced using a single homoepitaxial diamond substrate supplied by Element Six Ltd. The substrate was grown via chemical vapor deposition, was (001)-oriented, and measured 4.7 × 4.7 mm. An initial surface clean in boiling aqua regia followed by H_2SO_4/HNO_3 was performed to remove nondiamond carbon contaminants from the substrate surface. Hydrogen termination was performed in hydrogen plasma for 30 min at 580 °C.

An 80-nm-thick layer of Au was deposited on the substrate for use as a sacrificial layer (SL) to protect the H-terminated diamond surface during device fabrication and simultaneously provide an ohmic contact between the H-terminated diamond and Au due to the unpinned nature of the H-terminated diamond surface and high Au work function. An electron beam lithography process with three masks (including alignment marker definition) as shown in Fig. 1 was employed to produce

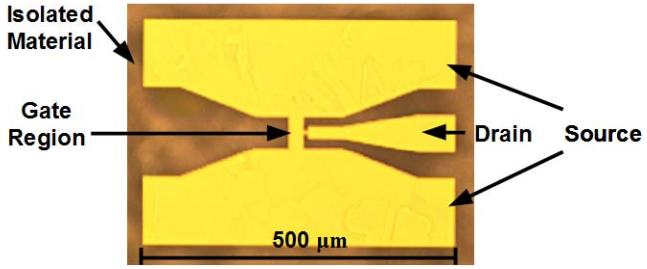

Fig. 2. Optical microscope image of an isolated region in the RF device structure.

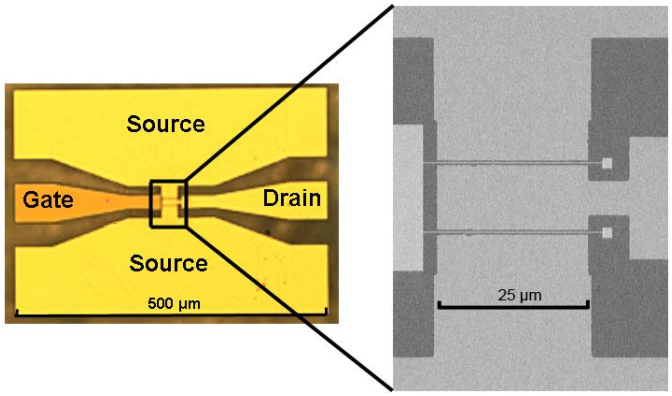

Fig. 3. Optical microscope image of a finished RF FET (left) with an SEM image of the FET gate region (right).

FETs suitable for RF characterization. Initially the Au SL was deposited before the definition of electron beam alignment markers and deposition around the Au SL on the edges of the substrate.

Next, isolation regions around the edges of each RF device were defined via electron beam lithography followed by a selective wet etch with a KI/I_2 solution. The Au-etched regions were exposed to oxygen plasma to remove the hydrogen termination and leave oxygen-terminated insulating diamond around the device and measurement pads, electrically isolating them. Current measured between isolated pads after this procedure was below the noise floor of the measurement system (100 pA). Fig. 2 shows an optical microscope image of the FET plus pads after isolation.

Finally, the FET gates and their connecting measurement pads were patterned simultaneously again via electron beam lithography. This process whereby the Au SL is selectively etched is a well-established procedure for fabrication of FETs on the hydrogen-terminated diamond surface [12], [13]. The same Au wet etch was used to undercut the resist profile and define the source–drain gap and Au ohmic contacts simultaneously, as shown in Fig. 1. An unfortunate side effect of this process is an increased line-edge roughness of the Au ohmic contact. This procedure is used, however, as it has been suggested previously that the KI/I_2 solution has a negligible effect on the H-terminated diamond leaving the surface conductivity unaffected [12], [13]. Al/Au (25 nm/25 nm) was deposited for the gate metal on to the exposed surface to form the 2×25 μm two-finger gate layout with L_g of 250, 120, and 50 nm, as shown in Fig. 3.

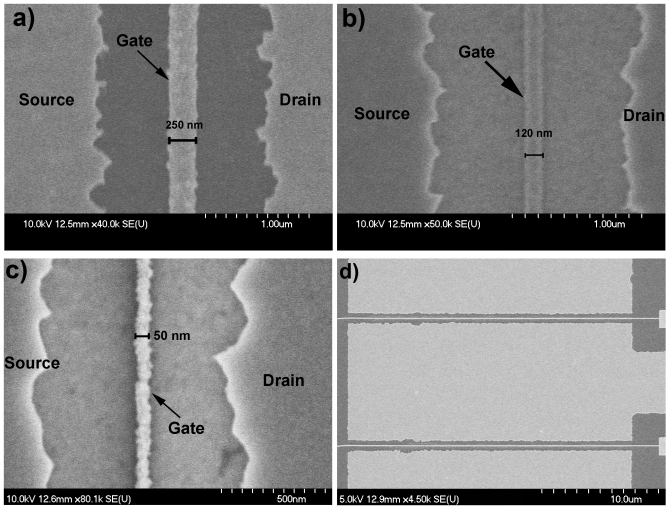

Fig. 4. SEM images of (a) 250-nm, (b) 120-nm, (c) 50-nm gates, and (d) dual-gate overview with an etched source–drain gap visible.

In parallel with FET devices, RF calibration structures were also fabricated. One structure was left with no active device in the center as an open RF calibration test structure and an extra layer of lithography was employed to deposit metal over another to create a short structure for deembedding of measurement pad contributions from the RF results.

Fig. 4 shows the SEM images of three different devices showing the source–drain gap to be $\sim$1.65 μm ($\pm$0.2 μm) for the 250- and 120-nm devices and $\sim$1 μm ($\pm$0.2 μm) for the 50-nm device (using an estimate of the ohmic contact edge due to its rough nature). This suggests that when L_g is reduced to 50 nm, the Au-etch solution may undercut the gate resist profile at a slower rate.

III. Results

The homoepitaxial diamond substrate utilized for these devices showed <0.2-nm rms roughness as measured by atomic force microscopy after hydrogen termination. A sheet resistance of $\sim$11 kΩ/sq and contact resistance of 5 $\Omega \cdot$mm were extracted from transmission-line-model (TLM) test structures. A sheet carrier concentration of 1.0×10^{13}/cm^2 and a hole mobility of 69 cm^2/V$\cdot$s were found from Hall measurement using van der Pauw test structures.

The dc characterization of the complete FETs was undertaken with the output characteristics for each L_g shown in Fig. 5. The gate voltage was not reduced below -2 V_{gs} due to concerns over drain current degradation with repeat measurement, as observed in [13] and [14]. Gate leakage current measured in each case was below the noise floor of the measurement system (100 pA) over the inspected bias range.

In the case of the 250-nm L_g device, the drain current does not begin to saturate until $V_{ds} = -5$ V indicating a substantial R_{ON}. The saturation current is -240 mA/mm for a V_{gs} of -2 V. The 120-nm device begins to saturate at slightly lower $V_{ds} = -4$ V with a saturation current of -360 mA/mm at -2 V_{gs}, while perhaps surprisingly, the 50-nm device requires a more negative source–drain bias to approach a saturated drain current at $V_{ds} = -9$ V with

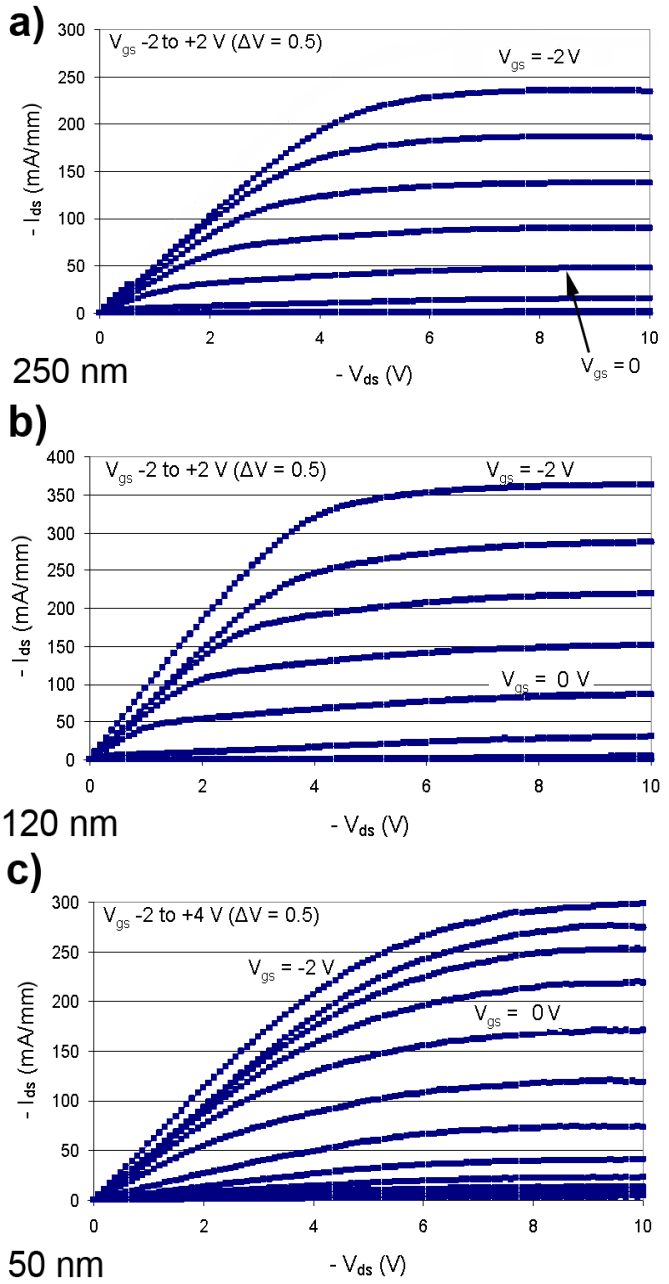

Fig. 5. Output characteristics for (a) 250-nm, (b) 120-nm, and (c) 50-nm L_g.

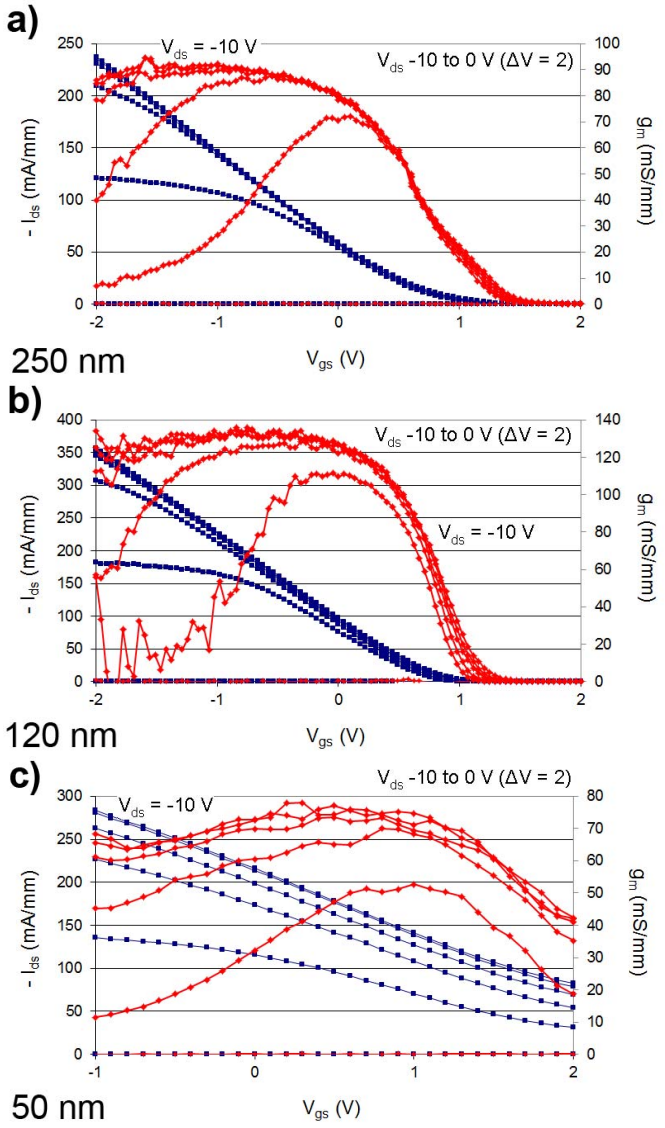

Fig. 6. Transfer (blue) and transconductance (red) characteristics for (a) 250-nm, (b) 120-nm, and (c) 50-nm gate devices.

a saturation current of -300 mA/mm at -2 V_{gs}, although from SEM inspection, these devices possessed a smaller source–drain gap.

The transfer and transconductance characteristics for these devices are shown in Fig. 6. Extracting linearly from the transfer characteristics, the threshold voltage is $+0.75$ V for $L_g = 250$ and 120 nm, while for $L_g = 50$, the device the threshold voltage is clearly far more positive. Further measurements indicated the device may still be turned OFF at a V_{gs} of $+4$ V. Peak transconductance was found to be 92 mS/mm for $L_g = 250$ nm with a plateau occurring between $V_{ds} = -7$ and -10 V with $V_{gs} = -1$ and -2 V. For the 120-nm device, a similar plateau occurs between $V_{ds} = -7$ and -10 V with $V_{gs} = -0.5$ and -1.5 V giving a peak transconductance value of 137 mS/mm. Finally for the 50-nm device, once again there is a plateau between $V_{ds} = -7$ and -10 with $V_{gs} = -0.5$ and $+1.5$ V giving a peak transconductance of 78 mS/mm.

These results are summarized in Table I, showing a comparison of dc figures of merit for each L_g.

TABLE I
SUMMARY OF DC FIGURES OF MERIT

	250 nm Device	120 nm Device	50 nm Device
Peak Drain Saturation Current (mA/mm) (at -2 V_{gs}, -10 V_{ds})	-240	-360	-325
Threshold Voltage (V)	+0.75	+0.75	+4
Extrinsic Peak Transconductance (mS/mm)	92	137	78

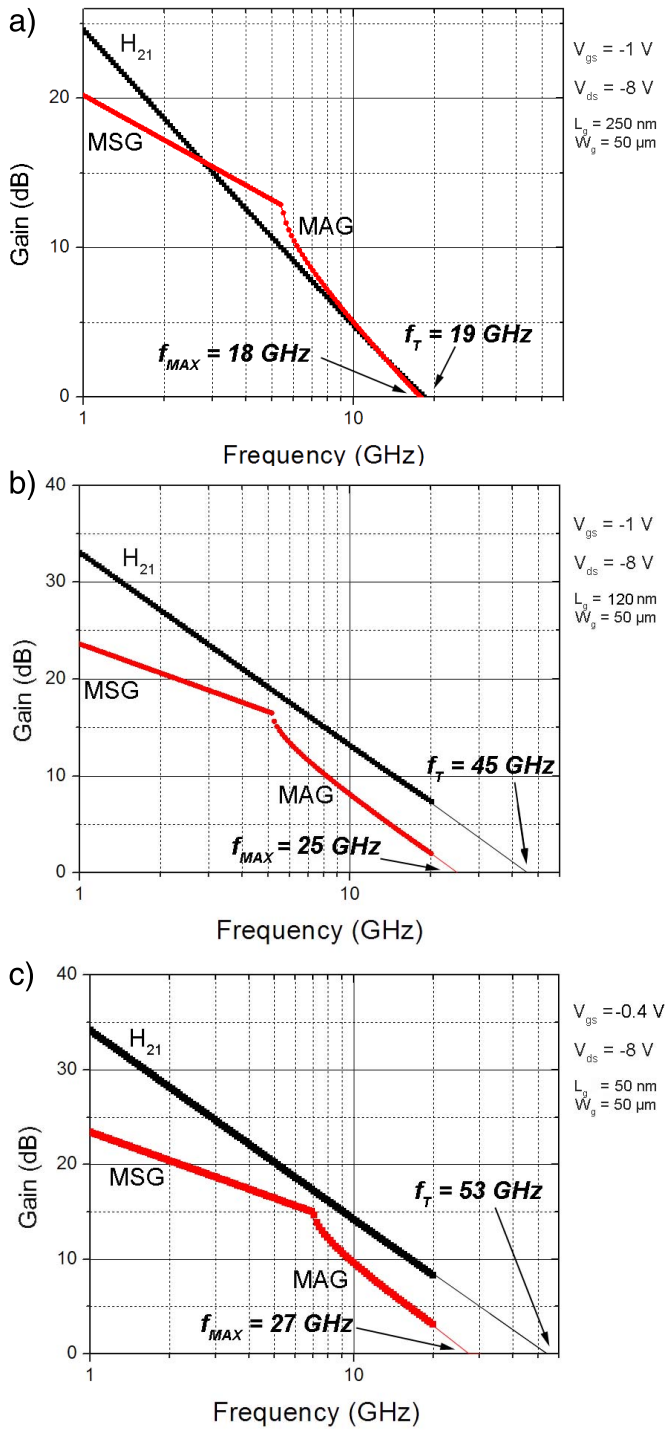

Fig. 7. RF figures of merit for (a) 250-nm (b) 120-nm, and (c) 50-nm L_g.

RF characterization was then performed on fresh devices of the same range of gate lengths. S-parameter data was measured between 1 and 20 GHz with a bias point of $V_{\rm ds} = -8$ V chosen for each L_g and $V_{\rm gs} = -1$ V for the 250- and 120-nm L_g devices and -0.4 V for the 50-nm device to attempt to match the peak transconductance during each measurement. Fig. 7 shows deembedded values of f_T and $f_{\rm MAX}$ for each L_g extracted from the graphical plots of gain versus frequency.

A two-step deembedding procedure using on-wafer fabricated open and short structures was employed for these devices to represent the parallel and series elements of the measurement pads, as described elsewhere [15] and as demonstrated in [16]. In the case of the open structure, the entire device under test is missing so as to extract the equivalent circuit including extrinsic values, rather than deembed all the way to the gate and give an unrealistic view of the device.

TABLE II
EQUIVALENT CIRCUIT DATA

Circuit Element	250 nm Device	120 nm Device	50 nm Device
g_m^* (mS)	6.82	17.00	8.75
R_{ds} (kΩ)	1.60	0.90	0.37
R_i (Ω)	14.12	16.09	27.20
C_{gs} (fF)	45.06	39.76	15.20
C_{gd} (fF)	2.35	1.80	0.30
C_{ds} (fF)	3.89	3.10	5.02
R_g (Ω)	184.01	508.00	370.40
R_s (Ω)	144.13	97.30	125.00
R_d (Ω)	144.6	97.30	119.00

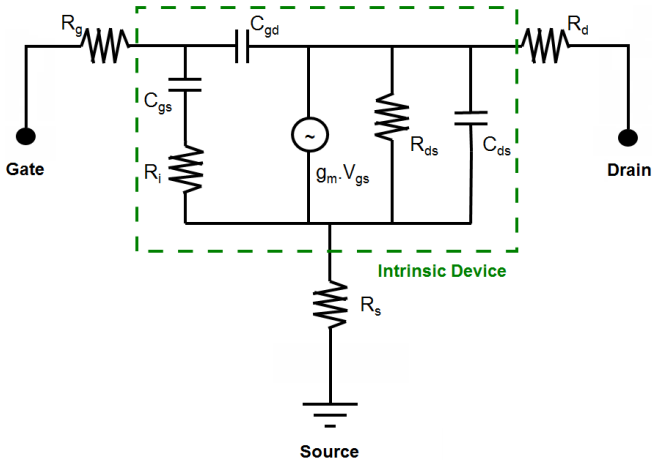

Fig. 8. Simplified equivalent circuit for the RF FET device.

TABLE III
EFFECT OF SCALING ON FET FIGURES OF MERIT

Circuit Element	250 nm Device	120 nm Device	50 nm Device
f_T Extrinsic (GHz)	19	45	53
f_T Intrinsic (GHz)	23	65	90
Extrinsic Percentage of Intrinsic Value	83	69	59
f_{MAX} Extrinsic (GHz)	18	25	27
f_{MAX} Intrinsic (GHz)	27	42	43
Extrinsic Percentage of Intrinsic Value	67	60	63

Table II summarizes a relevant equivalent circuit device data extracted from each RF FET using the Agilent Advanced Design System software, as displayed in Fig. 8.

To begin with a broad estimation of extrinsic parameters could be made from test structure data, e.g., R_s and R_d from TLM results. Then intrinsic parameters were extracted based on the method presented in [17]. After model optimization, the total error between modeled and measured S-parameters was only 0.1% within the measured frequency range.

Table III summarizes the extracted RF figures of merit from each of these devices.

The extrinsic values from Table III are extracted linearly from the plots in Fig. 7. Equations (1) and (2) are used to determine the intrinsic f_T and f_{MAX} figures

$$f_T^{\mathrm{int}} = \frac{g_m}{2\pi \cdot C_g} \tag{1}$$

$$f_{\mathrm{max}}^{\mathrm{int}} = \frac{f_T^{\mathrm{int}}}{2}\left(\frac{R_{\mathrm{ds}}}{R_g + R_i}\right)^{\frac{1}{2}}. \tag{2}$$

The value of the intrinsic RF transconductance is given by g_m, C_g is the total intrinsic gate capacitance, i.e., $C_{\mathrm{gs}} + C_{\mathrm{gd}}$, v is the average carrier velocity beneath the gate, L_g is the gate length, R_{ds} is the output resistance, R_g is the gate resistance, and R_i is the intrinsic channel resistance, as shown in Fig. 8 [18]. The values extracted from the equivalent circuit data were then utilized to determine the intrinsic FET performance for each gate length.

IV. Discussion

The significant R_{ON} observed from dc FET measurements arises due to the ohmic contact consisting of Au deposited directly on to the H-terminated diamond surface leading to a significant contact resistance (5 $\Omega \cdot$mm). The Au wet etch cannot precisely control the source–drain spacing that also leaves rough contact edges that although require further optimization are comparable with other devices in this technology [6], [7].

As expected, scaling of FET L_g leads to an improved RF performance, as observed by the figures of merit extracted from Fig. 7 and the values in Table III. L_g is not the only variable involved however, as the significant access resistance as well as output conductance in these devices limits the extrinsic figures of merit. The equivalent circuit data reveals more insight into the individual components and the effects of scaling upon this technology. Intrinsic RF transconductance follows the same trend as in the dc measurement, increasing when scaling from 250–120 nm but then decreasing when scaled to 50 nm, most likely due to short-channel effects limiting the control the gate has over the channel.

Total gate capacitance scales as one would expect, reducing with L_g although not scaling linearly with the reduced gate dimensions. It should be stressed that the equivalent circuit values have been extracted for the specified bias point, thus the field profile, and hence charge distribution beneath the gate will vary slightly for each gate length. Due to the varying gate dimensions, there may also be a different ratio of oxidized to nonoxidized Al at the periphery of each gate that may alter the effective gate length accordingly. With the 50-nm device, the total gate capacitance has reduced to the point that despite the reduced intrinsic transconductance, the ratio of the two is still large enough to yield increased intrinsic f_T and f_{MAX} values compared with larger gate lengths.

Access resistance as well as output conductance will have a large impact on extrinsic performance, and is the reason why the 50-nm L_g device sees the extrinsic f_T to reach only 59% of its intrinsic value [10]. The large access resistance associated with all these devices clearly has less effect at the larger L_g. R_{ds} also effects the extrinsic performance; as L_g is reduced, so is its value due to the onset of short channel effects. The gate resistance R_g, has a substantial impact on both the intrinsic and extrinsic values of f_{MAX}, as the gates used here are not of a T-gate design. A slightly anomalous result may be seen in the 120-nm device, where the gate resistance is significantly larger than the 50-nm device. Following inspection of the devices by scanning electron microscopy, this is suspected to be due to the top Au layer peeling off the Al/Au gate-stack on a number of these devices. This may be addressed in future devices using a thicker gate metallization. Although this may give a slightly lower f_{MAX} value than one would expect, the entirety of the gate is intact and contacting the channel (as evidenced by the total gate capacitance value and the fact the transistor fully turns OFF), and hence does not significantly affect the value of f_T.

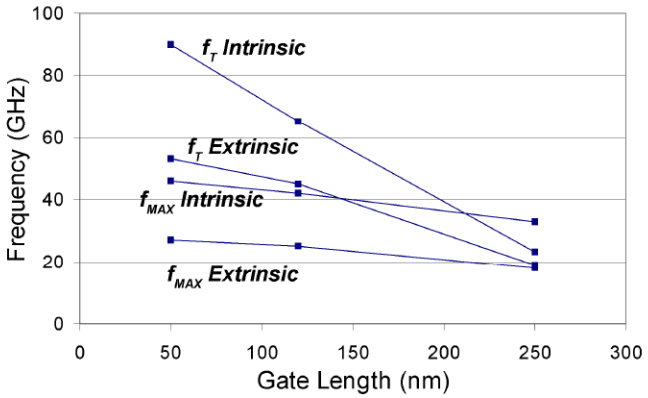

Fig. 9. Comparison of RF figures of merit with scaled L_g.

A clear picture of the impact of scaling upon this technology can be observed in Fig. 9, which summarizes the effects of scaling on the RF figures of merit, showing the increased impact of access resistance and output conductance down to the reduced L_g of 50 nm. The observed increase in output conductance with the reduced gate length may be attributed to short channel effects and hence be intrinsic to the H-diamond FET structure. Therefore, if continued improvement in the RF performance of this technology is to be achieved, then new techniques to reduce the access resistance in these devices should be prioritized.

Research has already begun to address these issues as well as attempting to improve the reliability of diamond FETs with [19] showing the ability to almost fully preserve the Surface Transfer Doping (STD) affect by the use of NO_2 and Al_2O_3, and more recently work [20] showing the ability to not only preserve but also enhance the STD process using MoO_3 as an alternative electron acceptor material. It will be important in the future to incorporate these new materials into a more standard and repeatable fabrication procedure less volatile to processing, negating the need for an Au SL and etch, which leaves the rough ohmic contacts as visible in Fig. 4.

V. Conclusion

Several different L_g hydrogen-terminated diamond FETs have been reported on the same homoepitaxial diamond substrate. RF diamond FETs with sub-300-nm gate lengths

have been discussed to see the limitations imposed from parasitic contributions and analysis of these through equivalent circuit extraction. The 120-nm L_g device with $f_T = 45$ GHz is the highest value achieved at this gate dimension on a single crystal diamond substrate, while the 53-GHz value for the 50-nm device is the highest f_T reported for any diamond based transistor to date. This demonstrates that homoepitaxial material is a viable option for diamond FETs.

Despite the improvements in the frequency performance of diamond RF FETs brought about by the reduction of L_g, it is clear there is a need for improvements to the FET fabrication process before any further improvement can be made in this regard. This is due to the access resistance and output conductance becoming dominant at the 50-nm node.

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