Tactile Sensing Chips With POSFET Array and Integrated Interface Electronics

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***Abstract*— This paper presents the advanced version of novel piezoelectric oxide semiconductor field effect transistor (POSFET) devices-based tactile sensing chip. The new version of the tactile sensing chip presented here comprises of a 4 × 4 array of POSFET touch sensing devices and integrated interface electronics (i.e., multiplexers, high compliance current sinks, and voltage output buffers). The chip also includes four temperature diodes for the measurement of contact temperature. Various components on the chip have been characterized systematically and the overall operation of the tactile sensing system has been evaluated. With new design, the POSFET devices have improved performance [i.e., linear response in the dynamic contact forces range of 0.01–3 N and sensitivity (without amplification) of 102.4 mV/N], which is more than twice the performance of their previous implementations. The integrated interface electronics result in reduced interconnections which otherwise would be needed to connect the POSFET array with off-chip interface electronic circuitry. This paper paves the way for CMOS implementation of full on-chip tactile sensing systems based on POSFETs.**

***Index Terms*— POSFET, CMOS, tactile sensing.**

I. Introduction

TOUCH sensing plays an important role in various application domains such as robotics, electrotextiles, prosthetics, and medical instrumentation. Over the years, significant efforts have been made to develop tactile/touch sensors using different materials, and transduction methods and structures [1], [2]. The suitability of these sensors to above application domains depends on a number of features including sensor size, sensor response time, and physical features such as bendability or conformability of the sensor patch etc. [3], [4]. For example, many times the sensors are big in size and considering also the associated electronics, they may not be suitable for parts like fingertips of a robot, where large numbers of sensors are needed. For this reason, Micro-Electro-Mechanical Systems (MEMS) based miniaturized touch sensors with on-chip electronics have been explored in past [5], [6]. The MEMS based touch sensors are realized with diaphragms and cantilevers and are generally sensitive [7]. They can detect contact forces (∼0.25 N) that are at best equal to the lowest forces experienced by humans in normal manipulation tasks (∼0.15 – 0.9N) [2]. Similarly, mechanical flexibility has been achieved in touch sensing schemes by using Organic Field Effect Transistors (OFET) [8]–[12], fibers [13], and Flexible Printed Circuit Boards [14], [15] for conformable tactile skin to measure parameters such as pressure, contact force and temperature. Silicon (Si) technology has also been explored for miniaturized touch sensors [16]–[18]. With precision down to sub-micron scale and the high quality of materials the Si technology offers avenues for developing high-performance miniaturized sensors with possibility of accommodating the electronics on same chip - leading to a full on chip tactile sensing system. Recent developments on Si based ultra-thin bendable chips have also opened avenues for conformable tactile sensing chips [19]–[21]. The tactile sensing system on chip will be a potent solution for reducing the number of wires, which is needed in application such as robotic hands to improve dexterity.

The touch sensing chip reported here explores above opportunities offered by Si technology. This work advances our research on POSFET tactile sensing [16], [17], [22], [23], by realizing on the same Si die a 4 × 4 array of POSFET devices, four temperature diodes for the contact temperature measurement, and the Interface Electronic (IE) circuits i.e. multiplexers, current mirrors, high compliance current sinks and voltage output buffers. The integrated interface electronics also results in reduced wires which otherwise would be needed to connect the POSFET array with off-chip readout circuitry. This is a significant advantage for applications such as robotics where wiring between sensors and electronics is considered a major issue. The chip presented here has been fabricated by using CMOS technology. The results discussed in this paper significantly extend our work presented at 2013 IEEE Sensors Conference [24]. The new results presented in this paper include systematic characterization of on-chip electronics and the response of POSFET chips.

Manuscript received March 31, 2014; revised June 15, 2014 and August 4, 2014; accepted August 5, 2014. Date of publication August 13, 2014; date of current version August 21, 2014. This work was supported in part by the European Commission under Grant PCOFUND-GA-2008-226070-Trentino, PITN-GA-2012-317488-CONTEST, and in part by the Italian MIUR Project PRIN 2007 Tactile Sensing System for Humanoid Robots Using Piezo-Polymer-FET Devices. The associate editor coordinating the review of this paper and approving it for publication was Prof. David A. Horsley.

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Digital Object Identifier 10.1109/JSEN.2014.2346742

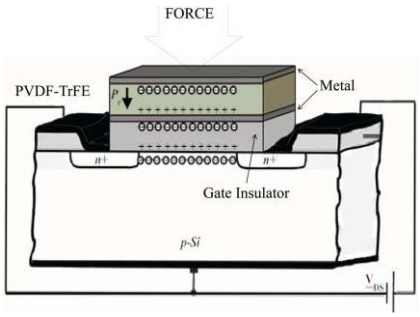

Fig. 1. The working of POSFET touch sensing device.

This paper is organized as follows: The concept of POSFET touch sensing device is presented in Section II. The design of various components on the advanced version of POSFET tactile sensing chip are presented in Section III and explained in the following sections. Section IV describes the fabrication of tactile sensing chip and the characterization of various on-chip electronic components is presented in Section V. The evaluation of POSFET devices in terms of their response to external force stimuli is given in Section VI. Finally, the concluding Section VII summarizes the results and presents future directions.

II. The Concept of a POSFET Device

A POSFET touch sensing device has the structure similar to the one shown in Fig. 1 and Fig. 2 (a). The POSFET devices are fabricated by spin coating piezoelectric polymer P(VDF-TrFE) (Poly (vinylidenefluoride trifluoroethylene)) film on the gate area of MOS devices and polarizing the polymer film in situ i.e. applying the polarization field across the polymer after it has been deposited on the gate area of Metal Oxide Semiconductor (MOS) device. The piezoelectric polymer film is therefore an integral part of the device. The remnant polarization (P_r) of the polarized polymer results in an intrinsic electrical dipole equivalent to fixed charges $\pm$Q, as shown in Fig. 1. In real devices, either through external connections or parasitic resistance of the P(VDF-TrFE) capacitor, the free charge is redistributed on to compensate the electrical dipole. When external force is applied on the POSFET device, additional charges (which are proportional to the applied force) reflect into the channel, thereby modulating the induced channel. In this way the (contact) force is directly reflected as the variation in channel current of the POSFET devices – which can be further processed by on-chip electronic circuitry such as the one presented in this work.

Similar approaches, but using extended gates, have been reported in the past for pressure and touch sensing [18], [25], [26]. In the extended gate approach, the gate terminal of a MOS device is connected to a large electrode or to an extended gate that is located elsewhere on the chip (Fig 2b). Like POSFETs, the extended gate approach too brings the sensor and conditioning electronics closer and hence the overall response is better than the conventional approaches where the sensor and conditioning electronics are placed apart. However, extended gates introduce a large

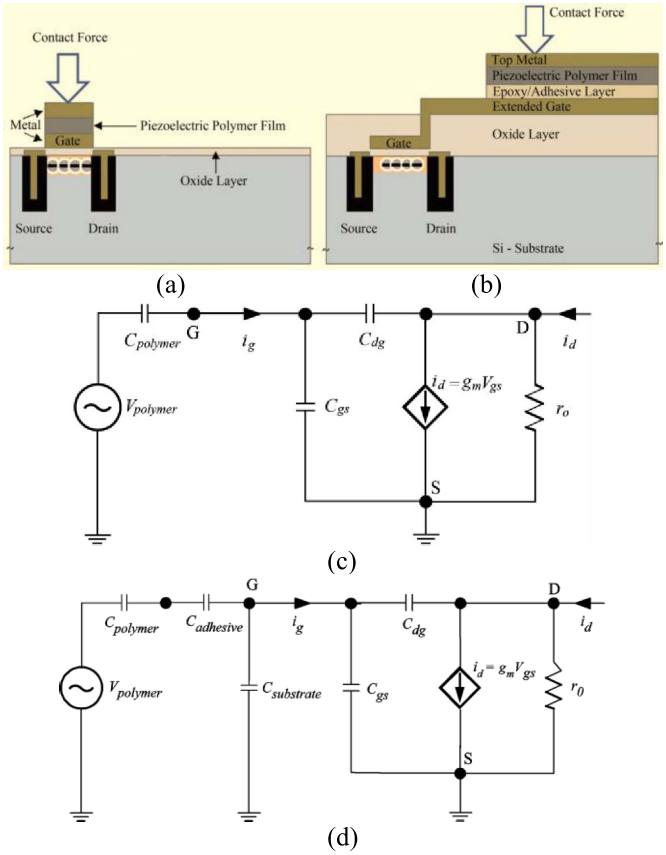

Fig. 2. The comparison of (a) POSFET and (b) extended gate devices [1]. The small signal equivalent of (c) POSFET and (d) extended gate devices. The piezoelectric layer is shown by its approximate electrical equivalent i.e. the voltage source $V_{polymer}$ in series with the capacitance $C_{polymer}$.

substrate capacitance, as shown in the small signal equivalent (assuming a common-source configuration of MOS) in Fig 2d. The substrates capacitance attenuates the voltage available at the gate terminals of MOS transistors, as evident from Eq. (1) and (2). Using the small signal equivalent of POSFET (Fig 2c) and extended gate devices (Fig 2dc) the amount of generated voltage in the piezoelectric polymer layer ($V_{polymer}$) that is transferred to gate terminal of MOS transistor (V_g) is:

$$\frac{V_g}{V_{polymer}} = \frac{C_{polymer}}{C_{polymer} + C_{gs} + C_{gd}(1 + A_v)} \tag{1}$$

and the voltage transferred to gate in case of extended gate devices (Fig 2d) is:

$$\frac{V_g}{V_{polymer}} = \frac{C_{polymer}}{C_{polymer} + \left(\frac{C_{polymer}}{C_{adhesive}} + 1\right)[C_{gs} + C_{sub} + C_{gd}(1 + A_v)]} \tag{2}$$

where, A_v is the intrinsic gain of transistor, and C_{gs} and C_{gd} are gate–source and gate–drain capacitances of MOS device respectively. C_{sub} is the substrate capacitance mainly due to the oxide layer under the extended gate and $C_{adhesive}$ is the capacitance due to the epoxy or any other adhesive to

adhere a separately prepared piezoelectric polymer film on to extended gates. Both C_{sub} and $C_{adhesive}$ make denominator of Eq. (2) higher than that in Eq. (1) and hence for the same $V_{polymer}$, the V_g is higher in POSFETs. In other words, the substrate capacitance C_{sub} (which has larger value in case of extended gate devices) and the capacitance due to epoxy $C_{adhesive}$ result in lesser voltage at the gate terminal of MOS device.

Assuming MOS transistors with similar designs in both the POSFETs (Fig. 2(a)) and the extended gate device (Fig. 2(b)), the gains with former over the latter can be approximated by dividing Eq. 1 and Eq. 2 as:

$$\frac{V_{g\_posfet}}{V_{g\_exgate}} = \frac{C_{polymer}+\left(\frac{C_{polymer}}{C_{adhesive}}+1\right)[C_{gs}+C_{sub}+C_{gd}(1+A_v)]}{C_{polymer}+C_{gs}+C_{gd}(1+A_v)} \quad (3)$$

The voltages V_{g_posfet} and $V_{g\_extgate}$ are the voltages at the gate of POSFET and extended gate based device respectively. For the comparison, the piezoelectric polymer is assumed to have same thickness and area. In other words, $C_{polymer}$ is assumed same in both the cases. Since MOS transistors are also assumed to be similar in both cases, the capacitances C_{gs} and C_{gd} are also same in both schemes. For transistors operating in saturation region, the capacitance C_{gd} can be considered equal to zero and C_{gs} can be considered equal to about $(2/3)C_{ox}$, where C_{ox} is the oxide capacitance of transistor [27], [28]. With above assumptions, Eq. 3 can be written as:

$$\frac{V_{g\_posfet}}{V_{g\_exgate}} = \frac{C_{polymer}+\left(\frac{C_{polymer}}{C_{adhesive}}+1\right)\left[\frac{2}{3}C_{ox}+C_{sub}\right]}{C_{polymer}+\frac{2}{3}C_{ox}} \quad (4)$$

For the POSFETs presented in this work the C_{ox} is $45pF$ and they have been designed to have a taxel (i.e. P(VDF-TrFE)) area of $0.9mm \times 0.6mm$. With $\sim 2.5\mu m$ thick P(VDF-TrFE) film present over the active area, the $C_{polymer}$ is $16pF$. The dielectric constant of 8 for P(VDF-TrFE) is used to obtain $C_{polymer}$ [29], [30]. For a $4000\mu m$ long and $50\mu m$ wide metal interconnect connecting the lower metal of the piezoelectric film (or the active area of extended gate devices), located in the center of the chip, with the gate of MOS device at periphery of the chip, as in [18], the C_{sub} is $\sim 55pF$. This is calculated by assuming a 500 nm SiO_2 (as with POSFETs in this work) underneath interconnects and the active area of extended gate device. The SiO_2 dielectric constant (i.e. 3.9) is used to obtain C_{sub}. Epoxy or urethane is typically used as adhesive in microfabrication, as in [18]. Assuming $10\mu m$ thick adhesive present over the active area of extended gate, as shown in Fig. 2(b), the value of $C_{adhesive}$ is about $3pF$. A dielectric constant of 6, typical of epoxies, has been used to obtain $C_{adhesive}$. Substituting above values in Eq. 3, the voltage V_{g_posfet} in current POSFETs is slightly more than 12 times higher than $V_{g\_extgate}$ in extended gate based device. This will further increase if, for example, thickness of epoxy is higher or if the C_{sub} is higher - both of which are absent in POSFETs. In previous version of POSFETs C_{ox} was $105pF$. The values of other capacitances for an extended gate active area similar to the previous implementation of POSFETs (i.e. $1mm \times 1mm$) [16], [17] are: $C_{adhesive} = 5pF$; $C_{sub} = 85pF$; $C_{polymer} = 24pF$. Using the values in Eq. 4, the voltage V_{g_posfet} in previous implementations of POSFETs would be about 10 times higher than $V_{g\_extgate}$ in extended gate based device.

In above analysis the taxel area is assumed to be in the center of the chip. In case of an array, the taxel area or the extended gates would be distributed over the chip. This means the C_{sub} would vary for sensors and hence the responses of extended gate devices over the chip would vary for the same input force. From electronics viewpoint, the capacitances C_{sub} and $C_{adhesive}$ along with extended gate may result in a higher RC time constant and make the extended gate devices slower. Thus, benefits of closely located sensor and electronics are not fully exploited with extended gate approach. With piezoelectric polymer on the gate of the MOS, the POSFETs are relatively free from the substrate capacitances. The presence of piezoelectric film on the gate of POSFETs also means that they occupy a smaller die area than the extended gate devices and the saved Si area can be used to accommodate on-chip electronics, as demonstrated here.

The voltage $V_{polymer}$ as a function of the applied mechanical stress can be estimated from $V_{polymer} = d_{33}T_3 s/\varepsilon_0\varepsilon$ [26], [31], where s is the thickness of piezoelectric films, d_{33} is the longitudinal piezoelectric coefficient, T_3 is the applied mechanical stress, ε_0 the dielectric permittivity of vacuum, and ε the relative permittivity of the piezoelectric film. Therefore, depending on the type of piezoelectric material and its physical dimensions, a wide variation is expected in the sensitivity of sensors based on above methods. In fact, this is true for the extended gate based devices reported in the literature. For example, the sensitivity of $70\mu m$ thick ferroelectret based sensing devices in [26] $0.1mV/Pa$ and that of $40\mu m$ thick PVDF (Polyvinylidenefluoride) based devices in [18] is $70mV/gmf$. The variations in the design of MOS devices in these cases make it difficult to compare them.

A further advantage of integrated POSFET is the reduced number and length of wires and interconnects, which clearly result in a reduced susceptibility to electrical noise of the sensor and a better SNR. The quantitative comparison of noise contribution in the two configurations is difficult to assess because it strongly depends on the final system arrangement (i.e. environmental noise, design and length of connecting wires, etc.) but it is evident that the on-chip implementation does not suffer from the noise injected by the connecting wires in configurations with off-chip amplification or extended gate.

III. Design of Tactile Sensing Chip Components

The tactile sensing chip has been designed to be used in robotics, in particular for the fingertips of humanoid robot, which requires tactile sensing structures with high spatio-temporal response. For example, the spatial acuity comparable with that of human fingertips ($\sim 1mm$) is needed [1], [2], [32]. Similarly, the sensors should be

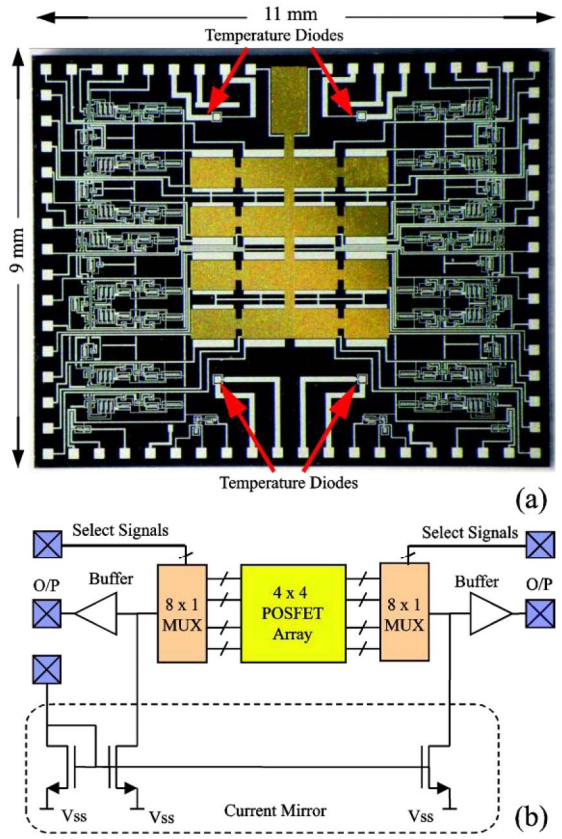

Fig. 3. (a) Image of the tactile sensing chip with on-chip IE, fabricated using CMOS technology. (b) The scheme of tactile array and on-chip electronics.

able to respond to the range of contact forces similar to that experienced by humans in normal manipulative tasks ($\sim$0.15–0.9N) [1], [2]. Humans can differentiate vibrations up to about 700 kHz [32]. Further, the tactile sensing structure should be multifunctional, i.e., they should be able to measure multiple contact parameters such as contact force, temperature, etc. The design of POSFET devices-based tactile sensing chips, shown in Fig. 3, has been influenced by above criterion. The IE comprises of basic circuit elements (multiplexers, current mirrors, high compliance current sink and output buffers) only as one of the goals is to evaluate the effect of the unique challenges related to POSFET fabrication on the working of on-chip circuitry. An important step in the working of POSFETs is to orient the dipoles in the piezoelectric material. Termed as poling, this step requires application of about 200V (at a rate of about 70$V/\mu m$) across the polymer film present on the gate of MOS in POSFET [31]. Application of such high voltage on the chip could damage the electronics on the chip. Therefore only basic electronics was included on the chip to understand the effect of poling on the working of interface electronics as well as the POSFETs. The successful outcome, as evidenced by the results presented in the following sections, paves the way for the on-chip implementation of the complete tactile sensing system. The fabricated tactile sensing chip consisting of 4 $\times$ 4 POSFETs, four temperature diodes, and the IE circuitry is shown in Fig. 3. The design of these components is presented below.

A. Design of POSFET Devices

The POSFET devices have been designed to have an active area of 0.9mm $\times$ 0.6mm, which is comparable with the spatial-acuity of human fingertips ($\sim$1mm). The n-MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices have been designed to have an aspect ratio (W/L) of about 273 for large transconductance (g_m). The large value of channel width (W) is obtained by designing POSFET with a serpentine like or interdigitated gate structure [22], [23]. The value of the aspect ratio is limited by the sensor area and the design factors such as the source/drain resistance. High W/L provides a gain close to unity in current configuration, with minimal influence of spread of process parameters. The length of source and drain diffusions have been modified in the new design from about 10 squares to 2. Considering typical sheet resistance as $\sim$60Ω/sq, the source/drain resistance in the new design is $\sim$120Ω. The parasitic resistance is thus reduced by a factor 5 and reflects a significant improvement of the actual trans-conductance over the previous implementations [16], [17]. The reduced channel area in the new design results in 2$\times$ improvement of PVDF capacitance versus gate capacitance ratio with respect to the previous implementation. This results in improved sensitivity, as also expected by the theory of FGMOS (Floating Gate MOS) systems (see Eq.1) [33]. In operative conditions the transistor is used in source follower configuration, using either a pull-down resistor or a current sink with current mirrors connected to source, while the FET (Field Effect Transistor) gate i.e. the lower electrode of P(VDF–TrFE) is floating and the top contact is short-circuited to drain. The chosen source–follower configuration does not provide signal amplification like a common-source configuration. A source follower configuration was chosen rather than a common-source gain stage, as with less than unity gain it also allows using POSFETs over wider range of forces needed in robotic applications. Further, source-follower configuration is helpful in minimizing the inherent devices mismatch related the sensors output variations.

B. Design of POSFET Arrays

The POSFET array comprises of 4$\times$4 touch sensing devices to map the contact forces applied in the chip area. The overall size of the chip is 9mm $\times$ 11mm, with 1mm center-to-center pitch of sensor elements, which can be further scaled down. With center-to-center distance of 1 mm the spatial resolution of tactile sensing array is similar to that of human fingertip. In order to reduce the number of interconnects and the contact pads, each row of the array shares the drain contact, as shown in Fig. 3a. The integrated array design allows us to implement a high density sensors array – which makes the POSFET tactile sensing chips suitable for applications such as manipulation and exploration of objects using robotic hands and fingers, where human like tactile spatiotemporal response is desired.

C. Design of Temperature Diodes

Four diodes implemented on the tactile sensing chip (Fig. 3a) make it multifunctional i.e. provide the tactile sensing

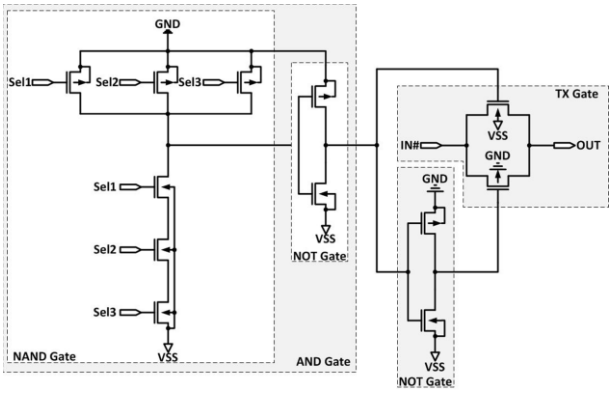

Fig. 4. The scheme of the analog CMOS multiplexer addressing circuitry.

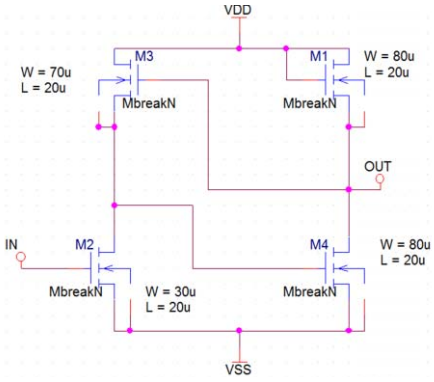

Fig. 5. The scheme of the buffer circuit.

chip the capability to measure contact force as well as contact temperature. Further, the temperature diodes provide the information related to any variations in the chip temperature which, if needed, could be used to compensate the temperature variations related changes in the response of POSFET devices. The diodes are realized with n+ regions implanted on p-well diffusions with $118\mu m \times 118\mu m$ junction area. The diodes are designed to work with $100\mu A$ forward current in order to exploit the diode temperature coefficient.

D. Design of Basic Electronics on the Chip

The basic electronic circuitry on the tactile sensing chip comprises of multiplexers, current mirror (i.e. high compliance current sink) and output buffers (Fig. 3b). The on-chip current sink bias the POSFETs in the common drain configuration. The supply voltage V_{ss} has been set to $-3.3V$ to be compliant with the external off-the-shelf components. This value can be decreased effectively down to $-5V$ and lower. The bias sink circuit has been implemented by a simple current mirror. The details of high-compliance current sink that may be used for full on-chip integration of biasing circuitry are explained in [23]. To properly test the on-chip circuitry, the current is set externally to the chip. The current sink value I_{bias} has been set to $100\mu A$. In order to minimize POSFETs access and response time, the tactile sensing array has been arranged in two 4×2 sub-arrays (see Fig. 3b). Each sub-array is addressed independently from the other by 8×1 multiplexer. In order to minimize Si area, each current sink is time-multiplexed among the POSFETs of the sub-array, i.e. only one POSFET at a time is addressed.

The address circuitry (an analog CMOS multiplexer) is shown in Fig. 4. To decrease circuit complexity, the addressing 8×1 multiplexer has been implemented by a 3 input NAND gate with an active pull-up network; the NAND output is subsequently buffered by two inverters which generate the direct and negate signals to control one of the CMOS transfer gates of the analog multiplexer. The propagation time of the analog multiplexer is in the order of $20\mu sec$. The timing has been organized in such a way that two POSFETs (one for each sub-array) can be addressed simultaneously: when a POSFET output is being accessed by the external circuitry, another one in the other sub-array is addressed is such a way that the transient time of the second POSFET will be elapsed when such POSFET will be accessed by the external circuitry as well. At that time, next POSFET in the former sub-array will be selected and so on. In this way, the switch-on POSFET transient time does not add to the POSFET address time.

The POSFET voltage output is buffered by the two-stage buffer circuit shown in Fig. 5. The configuration uses a two stage common source amplifier with a feedback on active load of the first stage to set the closed loop gain near to unity. The on-chip directly drives the output pad and decouples the POSFETs from the output of the chip.

IV. Fabrication of the POSFET Chip

The detailed CMOS fabrication process of the POSFET chips is explained elsewhere [22], [23]. In brief, the process is based on a non-standard $4\mu m$ CMOS technology with Al gate and nMOS transistors on p-well. The process has been implemented on n-type wafers with resistivity (10 to 12) Ωcm. The fabrication starts with boron implant and diffusion to create deep p-wells to insulate the n-type devices. Based on simulation and testing the p-well is $7.7\mu m$ deep with sheet resistance $3k\Omega/sq$. Implant of phosphorus and boron in p- and n-channel stop regions is performed in order to avoid short-circuits between different structures. Then, after growing a 500*nm*-thick field oxide, source and drain regions are defined and implanted using BF_2 and double As/P doping for *p*-type and *n*-type respectively, with a resulting sheet resistance of about $60\Omega/sq$. Gate region is opened and threshold adjustment is performed. A Si_3N_4/SiO_2 double layer with equivalent thickness 45*nm* is used as gate dielectric. The double layer dielectric is inherited from the template technology, originally developed for integrated chemical sensors [34]. A single layer SiO_2 gate dielectric would provide similar device properties. A 500*nm*-thick layer of LPCVD (Low-Pressure Chemical Vapor Deposition) LTO (Low Temperature Oxide) SiO_2 is deposited for electrical insulation, followed by contact hole realization and patterning of Al wires. Then, the FET section of the device is completed with the deposition of a second layer of 300*nm* of LPCVD LTO to insulate Al wires, with openings for electrical contacts. Then, $\sim 2.5\mu m$ thick P(VDF-TrFE) piezoelectric film is spin coated on the wafer and top metal (Cr/Au) is then deposited

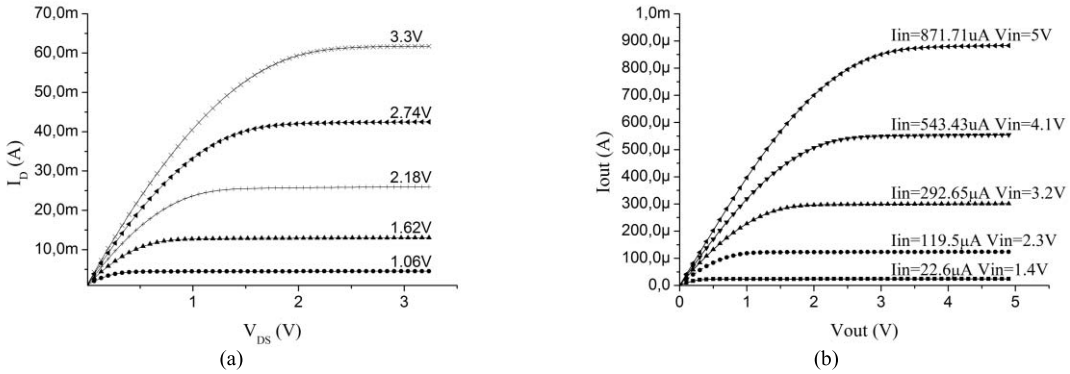

Fig. 6. (a) ID-VDS characteristic of POSFET device. (b) I_{in}-V_{out} characteristic of the current sink at various input bias voltages.

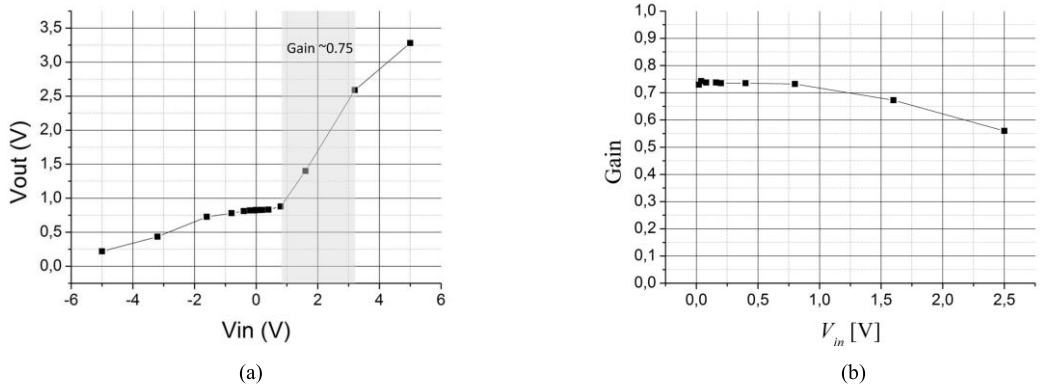

Fig. 7. (a) Buffer response at various V_{in} voltages. (b) Buffer gain at various amplitudes of the sinusoidal input signal V_{in}.

by e-gun evaporation and further defined over the gate area of POSFET only. The metal is also used as mask during subsequent plasma etching of the polymer. After deposition of P(VDF-TrFE), it was polarized by applying a polarization voltage of $200V$ across it in four cumulative steps of $50V$. To prevent potential breakdown of on-chip electronics and the POSFETs, the Si substrate and all metallization below the piezoelectric film were set to ground during the polarization phase. In doing so, the electronics under the piezoelectric film did not experience high polarization voltage. Poling was performed at $85°C$, to reduce the voltage needed for polarization. The fabrication steps related to deposition and processing of piezoelectric polymer film are similar to those reported in [35].

V. Characterization

The performance of various on-chip electronic circuits (i.e. multiplexer, buffer, current sink, and POSFETs) have been evaluated and analyzed first separately and then altogether.

A. POSFET Device

The FET transducers characteristics were obtained from experimental measurements before performing the full electronic system characterization. The main FET parameters extracted from measured data are the threshold voltage $V_{th} = 0.4V$, parameter $K = \mu C_{ox} W/L = 14e^{-3} A/V^2$ (in strong inversion and saturation) and the channel length modulation parameter $\lambda = 0.01V^{-1}$. The I_D-V_{DS} characteristic of the POSFET is shown in Fig. 6(a).

B. Current Sink

The output I-V characteristic of the current sink obtained from experimental measurements is shown in Fig. 6(b). Keithley 236 source measure unit (SMU) was used to source the bias voltage and to measure the input current. The Keithley 2400 source meter (SM) was used to sweep the output voltage and measure the output current. The bias voltage (i.e. $V_{in} = V_{GS} = V_{DS}$ of the current sink diode-connected transistor) was swept from $1.4V$ to $5V$ and then the input current was fixed. The threshold voltage (V_{th}(sink) $= 0.7V$) for current sink was obtained graphically from the I_D-V_{GS} characteristics. It may be noticed that the current sink provides an output resistance of $\sim 28M\Omega$ (i.e. $R_o = 1/(\lambda|I_o|)$) above $V_{MIN} (= V_{DS}(\text{sat}) = V_{GS} - V_{th}(\text{sink}))$ when $V_{in} = 1.4V$ ($I_{sink} = I_{DS} = I_o = 22.573\mu A$). While the output resistance decreases to $\sim 211k\Omega$ ($I_o = 871.71\mu A$) when $V_{in} = 5V$.

C. Buffer

The output buffer was also characterized separately to evaluate the circuit performance. The results from static experimental analysis of buffer circuit are given in Fig. 7(a). The plot was obtained by setting $V_{SS} = -5V$ and $V_{DD} = 5V$,

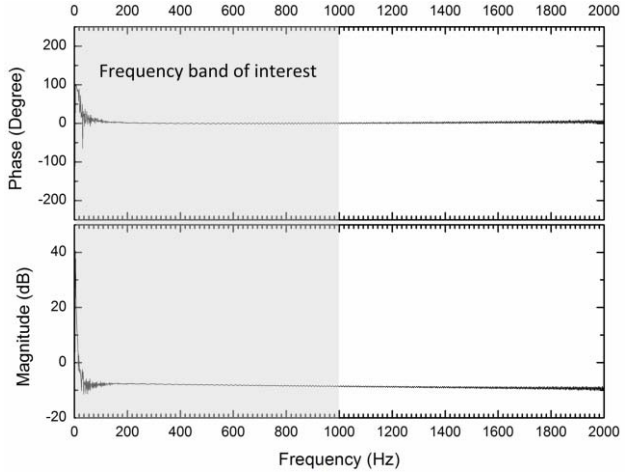

Fig. 8. Buffer frequency response; frequency sweep from $0.1Hz$ to $2kHz$, constant amplitude of $0.5V$ and offset at $2V$.

and by sweeping V_{in} from $-5V$ to $5V$. Fig. 6(a) shows also that the voltage gain is $\sim$0.75 in a range spanning from $0.8V$ to $3.2V$.

A dynamic analysis was also performed to evaluate the response of the buffer to sinusoidal input signal at fixed frequency and varying amplitudes. The sinusoidal signal frequency was set to $23Hz$ and the offset was set to $2V$ (approximately at the center of the shaded area where the gain is more or less constant - as shown in Fig. 7(a)). The results of the analysis are graphically reported in Fig. 7(b). It can be noticed the gain remains approximately constant as long as the amplitude of the input signal is below $\sim 1V$.

Figure 8 shows the frequency response of the buffer circuit. A sinusoidal frequency sweep from $0.1Hz$ to 2 kHz, constant amplitude of $0.5V$ and offset at $2V$ was input to the buffer and the corresponding output was measured and reported in Fig. 8. It can be noticed that the buffer gain is almost constant in the tactile frequency band of interest (i.e. $1Hz - 1$ kHz).

D. Multiplexer

Different experimental tests were performed to evaluate the performance of the multiplexer (MUX). The MUX have been supplied at $-5V$. In order to generate the analog input signal to the MUX input terminal and the digital logic levels to control the MUX selectors, a Labview^{TM} program has been developed to control a NI DAQ board PCI-6071E. The input waveform to the MUX input terminal was a sinusoidal signal of frequency equal to $78Hz$, as shown in Fig. 9(a). The stacked plot reports the selected MUX input (i.e. no.7, selected by setting the respective logic level for each selector) and the corresponding output of the MUX. The experimental test was performed to verify the selectors' truth table.

Different input waveforms were applied to the MUX to verify the MUX response at various input signals. Each input signal has a frequency of $78Hz$, amplitude of $-1.45V$ and offset of $-2.5V$. The signals have been acquired by means of the NI DAQ board PCI-6071E at the sampling frequency of 2 kHz and number of samples equal to 100. Each selector

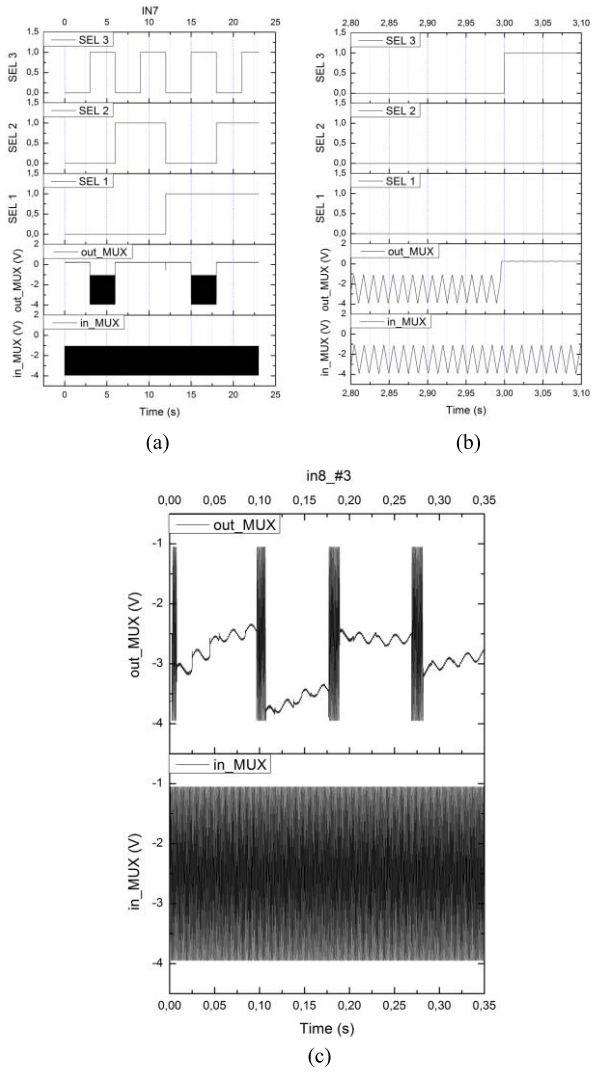

Fig. 9. Stacked plots show, respectively: selectors digital logic levels (i.e. SEL1, SEL2, SEL3); MUX output; MUX input. (a) The plot shows the response of the MUX when input no. 7 is selected and (b) the MUX response for the input triangle signal case; (c) MUX response for a sinusoidal input signal at $804Hz$ and selector switching time of $10ms$.

changed its logic state every 3 seconds. Fig. 9(b) shows the MUX response for the triangle case.

A sinusoidal signal was applied to the numbered 8 input terminal of the integrated MUX. The applied sinusoidal waveform amplitude was set to $-1.45V$, offset to $-2.5V$ and the frequency were set to $804Hz$. The sampling frequency of the DAQ board was set to 30 kHz. The selector switching time was set to $10msec$. Figure 9 (c) illustrates the response of the MUX when the sinusoidal signal described above is applied. As it can be noticed, the switching time is too small to allow settling of the MUX output, showing a transient when the transmission gate should be in the open state (i.e. transistors turned off).

VI. Experimental Evaluation

The tactile sensing chip with on-chip IE circuits, comprising of multiplexer, current sink, output buffer and one POSFET

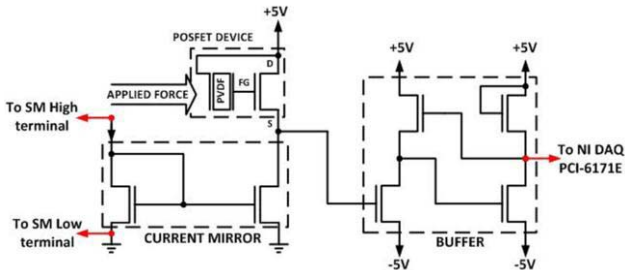

Fig. 10. The scheme for experimental measurement.

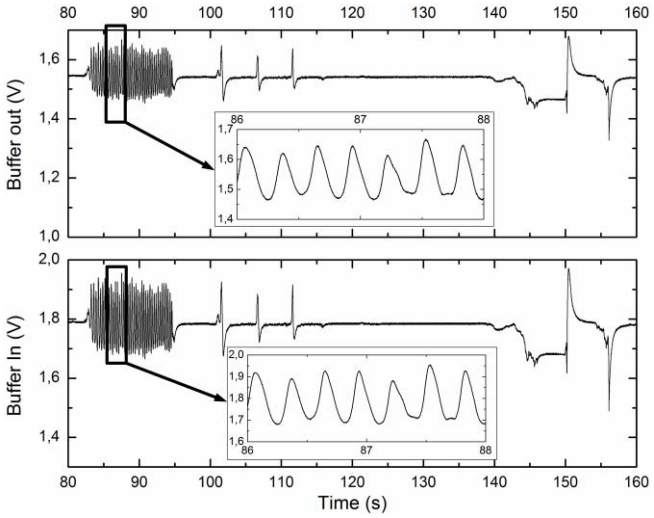

Fig. 11. The output response of the POSFET (of row 1 and column 1) at different manually-applied stimuli. Inset shows the magnified image of the POSFET response.

device, was also tested by using the circuit schematic shown in Fig. 10. The current sink biases the POSFET in the common-drain configuration. The current sink has been externally biased by a source meter at $2.3V$. The current sink input current I_{in} measured by the source meter, was equal to $109\mu A$. The measured current sink output voltage sets the POSFET source terminal to $1.8V$ ($V_{DS} = V_{DD} - V_s = 3.2V$), indicating a current flowing into the POSFET device of about $65\mu A$ (as can be seen from Fig. 6(b)). According to the buffer characteristic of Fig. 7(a), the output voltage of about $1.55V$ has been measured.

The time response of one POSFET device was observed in an experimental test. The MUX selectors were set to enable only the POSFET of row 1 and column 1. The POSFET device has been manually excited and the measured voltage buffer input and output time responses are shown in Fig. 11. In particular, three different manual stimuli have been applied sequentially: (1) sinusoidal like; (2) three single pressure-release stimuli (stimuli (1) and (2) have been applied using the tip of a pencil acting on the single POSFET); (3) a cylindrical metal weight (with base area larger than the chip) was put on the whole POSFET array (i.e. all the POSFETs were stimulated at the same time), but only the response of the POSFET of row 1 and column 1 was measured. Fig 11 reports the POSFET of row 1 and column 1 output response.

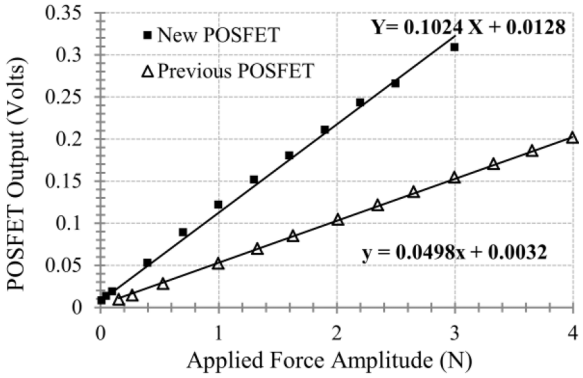

Fig. 12. The response of an on chip POSFET device with different normal forces and comparison with the previous POSFET device response [16]. The response of new POSFET matches with that having similar design and reported in [22].

The output signal is about 0.8 times the input signal as expected (i.e. the buffer voltage gain was measured to be $0.75V/V$).

The response of POSFET device was also observed by applying a dynamic force (sinusoidal, $1Hz$-$1kHz$) in normal direction on the device, as per scheme given in [22]. The maximum voltage outputs of POSFET device for a normal dynamic force in the range $0.01N$-$3N$ are shown in Fig 12. This test range is already wider than the contact forces experienced by humans in normal manipulation tasks i.e. ($\sim$0.15–0.9N) [1], [2]. The response is linear with sensitivity of POSFET devices equal to $102.4mV/N$, which is more than twice the value reported earlier [16]. The experimental conditions were similar to our previous works and the response of POSFET matches with that in [21]. These results indicate that the POSFET devices are capable of detecting contact forces as low as 0.01 N ($\sim$1 *gmf*) [23], with negligible delay between input force and the output voltage.

The observed improvement in the POSFET response can be also be analyzed with Eq. 1, which gives approximate voltage transferred from piezoelectric polymer to the gate terminal of MOS transistor. The ratio of approximate voltages available at the gate terminal of POSFETs in this work and the previous version of POSFET is:

$$\frac{V_{g\_posfet1}}{V_{g\_posfet2}} = \frac{C_{polymer1}}{C_{polymer2}} \times \frac{C_{polymer2} + C_{gs2} + C_{gd2}(1 + A_{v2})}{C_{polymer1} + C_{gs1} + C_{gd1}(1 + A_{v1})} \quad (5)$$

The variables with subscripts '1' and '2' in Eq. 5 refer to the POSFET in this work and its previous implementation respectively. For transistors operating in saturation region, the capacitance C_{gd1} and C_{gd2} can be considered equal to zero and C_{gs1} and C_{gs2} can be considered equal to $(2/3)C_{ox1}$ and $(2/3)C_{ox2}$, respectively [27], [28]. Thus, Eq. 5 can be written as:

$$\frac{V_{g\_posfet1}}{V_{g\_posfet2}} = \frac{C_{polymer1}}{C_{polymer2}} \times \frac{C_{polymer2} + \frac{2}{3}C_{ox2}}{C_{polymer1} + \frac{2}{3}C_{ox1}} \quad (6)$$

The values of various capacitances in Eq. 6 are: $C_{polymer1} = 16pF$; $C_{polymer2} = 24pF$; $C_{ox1} = 45pF$ and $C_{ox2} = 105pF$.

Using these values the voltage $V_{g\_posfet1}$ is about 1.4 times higher than $V_{g\_posfet2}$. Considering also the effect of reduced parasitic resistance, the observed improvements in the sensitivity is compatible with the theory. Therefore, reduced parasitic resistance and improved capacitance ratio in the new POSFETs resulted in the improved sensitivity.

VII. Conclusion

The development and the experimental evaluation of the new advanced version of a CMOS tactile sensing chip comprising of an array of 16 POSFET devices and the on-chip Interface Electronics, has been presented in this work. The improved POSFET device design along with on-chip electronics lead to improved response sensitivity that is more than twice that of the previous version. Various IE circuit blocks have been evaluated and their operation and performance assessed. The IE blocks are fully compliant with the operating constraints of the POSFET devices; the optimal setting of the POSFET operating point can be simply achieved as it has been experimentally proved. The simplicity and lesser Si area of the IE circuit implementation are of great importance for the optimization of the system implemented on-chip.

We demonstrated that the IE can be effectively implemented on the same chip of the POSFET array in a standard CMOS technology and due to the effectiveness of the circuit implementation the design can be easily scaled to a greater number of POSFET devices. This result paves the way to the on-chip implementation of the tactile system i.e. basically the Analog-to-Digital converter and the serial digital communication interface. This goal will be addressed in the future research. The systematic characterization of on-chip electronics carried reported in this work will help us advance this research further.

For applications such as robotics, integrated tactile system implemented with CMOS technologies will be of great advantage as this will further allow the reduction of wiring complexity by implementing on-chip local data processing and multiplexing. Such approach will also make it easy to handle the large amount of tactile data.

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