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Development of planar pixel modules for the ATLAS high luminosity LHC tracker upgrade

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A B S T R A C T
The high-luminosity LHC will present significant challenges for tracking systems. ATLAS is preparing to upgrade the entire tracking system, which will include a significantly larger pixel detector. This paper reports on the development of large area planar detectors for the outer pixel layers and the pixel endcaps. Large area sensors have been fabricated and mounted onto 4 FE-I4 readout ASICs, the so-called quad-modules, and their performance evaluated in the laboratory and testbeam. Results from characterisation of sensors prior to assembly, experience with module assembly, including bump-bonding and results from laboratory and testbeam studies are presented.

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1. Introduction
The Large Hadron Collider will undergo a series of upgrades over the next decade, increasing both the energy and the luminosity, culminating in the Phase-II upgrade that will deliver an unprecedented instantaneous luminosity of $5 \times 10^{34}$ cm$^{-2}$ s$^{-1}$ at an energy of 14 TeV, with the aim of delivering 3000 fb$^{-1}$ to ATLAS over 10 years. The extended LHC running will exceed the lifetime of the current ATLAS tracker. The increase in the instantaneous luminosity will increase the multiplicity of pp interactions from $\sim 55$ at the Phase-I luminosity to $\sim 140$ requiring a tracking detector with greater granularity to maintain the occupancy at $\sim 1\%$, which has been shown to give good tracking performance with the current tracker. The integrated luminosity will require the trackers to operate after integrated fluences of $2 \times 10^{26}$ 1 MeVn$_{eq}$ cm$^{-2}$ at the inner radius. It is proposed to develop and construct a new tracker for ATLAS over the next 10 years [1] ready for the start of Phase-II operation around 2024. The proposed layout is shown in Fig. 1.

This paper focusses on the development of large area pixel modules for the outer barrel layers and forward disks of the pixel system. These areas will be exposed to a maximum integrated fluence of $1.8 \times 10^{25}$ 1 MeVn$_{eq}$ cm$^{-2}$ and 0.9 MGy [1]. The leading silicon based technology for this region is n-in-p as it has demonstrated radiation hardness at these levels and can be manufactured at a scale and cost suitable for particle physics experiments. To cope with the increased occupancy the pixel size is reduced from 50 $\mu$m $\times$ 400 $\mu$m, as used in the current detector, to 50 $\mu$m $\times$ 250 $\mu$m. To minimise material, the active area of the pixel modules should be $\geq 90\%$ and the thickness of the modules should be reduced by thinning the modules i.e. both the sensors and readout ASICs to 150 $\mu$m or less. The upgraded pixel system will be significantly larger than the current system, increasing in area from 1.7 m$^2$ to 8.2 m$^2$, corresponding to an increase in the number of channels from 80 million to 638 million.

2. Sensor design
The construction of the upgraded pixel system, which has an area about 4 times larger than the current system, requires the yield and cost of pixel sensor production to be optimised. This can be partially addressed by using large area readout ASICs and sensors as this reduces the cost of bump-bonding, which scales approximately with the number of chips processed rather than by the total area. The “quad” sensor is a large area sensor that is compatible with the geometry of the outer barrel layers and forward disks of the upgraded pixel tracker, and is read out with 4 FE-I4 readout ASICs [2]. It has an active area of 40.4 mm $\times$ 34.4 mm for “test” FE-I4s and

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40.4 mm × 34 mm for “production” FE-I4s. As discussed in
the introduction, it is important to maximise the active area of
the sensor and avoid inactive regions at the borders of the
FE-I4 chips. Long pixels of 450 μm are added to bridge the gap
along the long pixel direction. Sets of ganged pixels are used to bridge the gap
along the short pixel direction. Two designs of ganged pixels were
made for the “test” and “production” FE-I4 chips. The “test” chips
have an additional row of test circuits, and extend the length of the
FE-I4 by about 100 μm along the short pixel direction, while the
“production” chips have had the additional circuitry removed.
Depending on the design 4 or 6 pixels were added in the region
between the FE-I4s and connected via top metal layer to pixels that are
bump-bonded to the FE-I4. This results in an ambiguity in the hit position
that will have to be resolved in reconstruction. The sensors have been manufactured on 300 μm thick 10 kΩ cm⁻¹
p-type Si 6" wafers by Micron Semiconductor Ltd.¹ with the segmented side made using a heavily doped n-type implant and p-spray isolation. The wafers contained five quad sensors and eight
electrical systems with a geometry corresponding to a single FE-I4. The layout
of the sensor has been measured on the wafer based on
measuring the current-voltage (I–V) curve. Sensor yields of 97% for
quad sensors, based on evaluating 35 devices from 7 wafers, and
78% for single devices, based on evaluating 49 devices from
the same 7 wafers, have been achieved, using the criteria that the
leakage current measured at 50 V above the depletion voltage (70 V) is
less than 1.5 μA and there is no sharp breakdown. The I–V
for the quads and single chip sensors from a typical wafer is shown in
Fig. 3. On the wafer, the devices are biased via a punchthrough
structure. The leakage currents of the quad sensors at 20 °C were
measured to be ~ 500 nA at a bias voltage of 100 V, corresponding to
~ 40 nA cm⁻². After assembly into a module, when the pixels
are biased through the FE-I4, the current is found to be ~ 100 nA, corresponding to 8 nA cm⁻² and which is comparable to the
currents measured for single chip modules of ~ 3 nA cm⁻² [3].
This indicates that the punchthrough bias structure needs to be
optimised and a new design was implemented on a later wafer
design [4]. As mentioned above, it is important to maximise the active area of the sensor. The guard-ring represents a significant
inactive area on the sensor. To investigate if this can be reduced,
two guard ring designs were implemented: a standard design
with 7 guard rings, corresponding to an inactive edge distance of 450 μm and a design with 5 guard rings, corresponding to an
inactive edge distance of 300 μm. The reduced guard ring design
could lead to increased leakage current or lower breakdown
voltages, but no difference in the I–V between the two designs
was observed.

3. Module assembly

The quad modules were assembled at VTT² where both the
FE-I4 and sensor wafers had under bump metallisation, UBM, and
PbSn solder bumps deposited. The four FE-I4 chips were then
flipped on to the sensor, one at a time, and a tack bond formed.
The assembly was then moved to a reflow oven, where the assembly was heated to 260 °C [3]. As discussed in the introduc-
tion the target thickness for both the sensor and the FE-I4 is
around 150 μm to minimise the material. For the first attempt to
assemble a module with a thinned sensor and readout chip, one of
the FE-I4 and sensor wafers was back thinned to 200 μm after
the UBM and bumps were deposited. The I–V of the sensors was
monitored throughout the process and no significant differences
were observed between the measured on-wafer I–V curve prior to
UBM deposition and after processing and dicing [3].

Power and data connections were made via a hybrid flex
supplied by the University of Bonn that was glued to the rear of
the sensor and wire bond connections made between the hybrid
and the FE-I4. The assembly was then mounted on a PCB and the
end of the flex connected to the PCB via wire bonds, as shown in
Fig. 4. The assembly was then operated using the USBpix readout
system. This provides the control sequences required to configure
and readout the FE-I4 and a switch on the PCB allowed each chip
to be characterised. A chip was tuned to a threshold of 3200 e and
1600 e. Tuning to 1600 e with a bias of 100 V applied, gave a
measured threshold of 1645 e with a standard deviation of 32 e, and
a noise of 133 e, comparable to that measured for single chip
modules [3]. The noise map and distribution are shown in Fig. 5.
The bump yield of the thinned module was evaluated by compar-
ing the noise distribution after tuning with and without bias
applied. The channels for which the noise does not decrease when
the bias is applied are assumed to be disconnected. A large fraction
of channels around the edge of the module were found to be
disconnected, giving a bond yield of around 75%. This has been
attributed to the bowing of the FE-I4 die during the reflow process
when bump bonding. Similar bond yields were found with single chip modules [3].

3.1. Bump-bonding for thinned module assembly

The difficulties of low bump-bonding yield when manufacturing
modules using thinned readout wafers are well known. Thinned
devices have been made by I2M for the ATLAS IBL project using a
support wafer and laser release method [5], but this process is not
optimal for the large production required for the outer barrel and
forward disk modules. An alternative method to address the issue of
the bowing of the FE-I4 during solder based bump bonding is being
investigated with Cea-Leti.³ After deposition of a TiCu UBM and
Cu micro-pillars with SAC solder bumps, the FE-I4 wafer will be
thinned and a compensating layer will be deposited on the rear of
the chip. This thin layer compensates for the bowing of the chip due
to the mismatch in the coefficient of thermal expansion between
the elements of the CMOS circuitry: metal, oxide and passivation
layers, and the bulk silicon when undergoing high temperature
processing such as solder based bump bonding. In addition to

¹ Micron Semiconductor Ltd, www.micronsemiconductor.co.uk.
addressing the issue of chip bowing during production, this will also make modules more robust against thermal shocks in the experiment. As a first step in evaluating this process a set of single chip sensors, manufactured by Micron Semiconductor Ltd [4], had UBM deposited and were then bump-bonded by Advacam to full thickness FE-I4s that had been processed by Cea-Leti. The preliminary studies of the bump-bond yield on three full thickness single chip modules was found to be \( > 99.9\% \). The next step of this programme is to evaluate the bow of thinned chips as a function of temperature to estimate the thickness of compensating layer required. A compensating layer can then be deposited on the rear of thinned FE-I4 chips, which can then be bump bonded to sensors and the bump yield evaluated.

The origin of the issue of bump-bonding thinned devices is the bowing during the high temperature solder reflow process. An alternative method using indium based connections is being investigated at the Science and Technologies Facilities Council (STFC) and has been used in the construction of the ATLAS and CMS pixel systems [6,7]. Indium bump bonding can be made using room temperature compression or thermo-compression. STFC has developed an indium process that has shown \( > 99.9\% \) good electrical connections with a typical resistance per bump in the range \( 0.20 – 0.31 \, \Omega \) on daisy chains with a bond density of 2125 bumps/cm\(^2\). The daisy chains underwent thermal cycling to test their mechanical and electrical robustness. After 500 120 s cycles of \(- 50^\circ\) C to \(+ 50^\circ\) C no defects were introduced over more than 10,000 bumps. Mechanical tests have shown

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shear strengths of 9 mN/bump have been achieved, corresponding to
\( \sim 250 \text{ N across the FE-I4.} \)

4. Quad module characterisation in testbeam

A full thickness quad module, bump bonded at VTT was taken
to the ACONITE testbeam at DESY [8] as part of the ATLAS PPS
programme [9]. Three of the four FE-I4 readout chips were
operational and were readout using the USBPix system. The data
from the three FE-I4s have been reconstructed separately as single
chip devices using the testbeam reconstruction software package.
Software to reconstruct 4 FE-I4s in a quad as a single object
together with the tracks reconstructed in the telescope is under
development. The reconstructed hit maps in the reference frame
of each readout chip are shown in Fig. 6. The hits are reconstructed
over an area of approximately 20 mm \( \times \) 10 mm corresponding to
the full area of the trigger scintillator, indicating that there are no
issues with disconnected bumps that have been observed in the
quad modules with thinned sensors and readout chips.

5. Summary

Quad sensors compatible with 4 FE-I4 readout chips with designs
including slim edges and structures to bridge the gaps between the
FE-I4 chips have been manufactured with high yield. Characterisation
of a single FE-I4 in a quad module has shown that it behaves in a
similar way to a single chip module in terms of noise and threshold.
Thinned modules show low bump yield and this is being addressed
by investigating other assembly methods: the use of a compensating
layer to reduce the bow of the FE-I4 chip during solder based bump
bonding and investigating room temperature bump bonding using
indium.

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