# Co-fabrication of Planar Gunn Diode and HEMT on InP Substrate

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***Abstract* - We present the co-fabrication of planar Gunn diodes and high electron mobility transistors (HEMTs) on an Indium Phosphide (InP) substrate for the first time. Electron beam lithography (EBL) has been used extensively for the complete fabrication procedure and a 70 nm T-gate technology was incorporated for the enhancement of the small-signal characteristics of the HEMT. Diodes with anode-to-cathode separation ($L_{ac}$) down to 1 $\mu$m and 120 $\mu$m width where shown to oscillate up to 204 GHz. The transistor presents a cut-off frequency ($f_T$) of 220 GHz, with power gain up to 330 GHz ($f_{max}$). The integration of the two devices creates the potential for the realisation of high-power, high-frequency MMIC Gunn oscillators, circuits and systems.**

***Index Terms* - Gunn diode, HEMT, integration, mm-wave**

## I. Introduction

THE Gunn diode oscillator was discovered in 1963 [1] while J. B. Gunn was examining the current-voltage characteristics of GaAs and InP. In recent years research has led to the implementation of increasingly high frequency Gunn diode oscillators for a range of applications [2]. Typically, Gunn diodes are implemented as a vertical layer stack of materials grown using methods such as molecular beam epitaxy (MBE). Vertically grown devices have presented a maximum frequency of oscillation of 77 GHz for GaAs based systems integrated into a rectangular waveguide [3]. Coplanar waveguide (CPW) based devices that are simpler and cheaper to implement have also been demonstrated, operating at the same frequency [4]. However, the oscillation frequency of the vertical structures is limited by the fixed anode-to-cathode separation that is determined by the epitaxial thickness of the channel layer.

The first theoretical [5] and experimental results [6] indicated that Gunn oscillations can occur on HEMT layer structures. Therefore, the electrodes of the diode can be implemented on the top of the wafer in a planar configuration similarly to the drain and the source of field effect transistors (FETs). The first planar Gunn diodes operating above 100 GHz were presented recently, where $L_{ac}$ was selected accurately through the lithographic design [7]. Using this method, signals at different frequencies can be generated from diodes with different geometries, implemented on the same chip. Recent development of planar Gunn diodes has focused on the modification of the layer structure to increase the output power. The addition of extra doping layers [8] and the introduction of strained $In_{0.23}Ga_{0.77}As$ for the formation of the channel layer [9] led to the significant improvement of the power characteristics. The maximum generated power was boosted to -4 dBm in an alternating $In_{0.23}Ga_{0.77}As$/GaAs layer structure with 7 channel layers [10]. However, the current density of the multi-channel devices was increased by approximately 5 times in comparison with the single-channel devices, indicating that not all the channels contribute to the oscillation.

The implementation of planar Gunn diodes and pHEMTs on GaAs substrates side-by-side has been recently studied [11], demonstrating the potential for amplification of the diode signal using a transistor-based amplifier on the same IC. However, the low power level of -40 dBm suggested that we either improved the layer structure or moved to an InP-based system. Most recently, planar devices with a single channel layer of $In_{0.53}Ga_{0.47}As$ grown on InP have demonstrated exceptional characteristics with 164 GHz maximum frequency of oscillation and -10 dBm generated power [12]. In this paper we demonstrate the co-fabrication of planar Gunn diodes and HEMTs on the same InP substrate for the first time. The InAlAs/InGaAs hetero-structure using a single delta-doping layer was designed for the implementation of HEMTs, where $In_{0.53}Ga_{0.47}As$ was used for the formation of the channel and the cap layer. The use of a relatively simple InP-based HEMT structure [12] enabled us to demonstrate co-integration of two

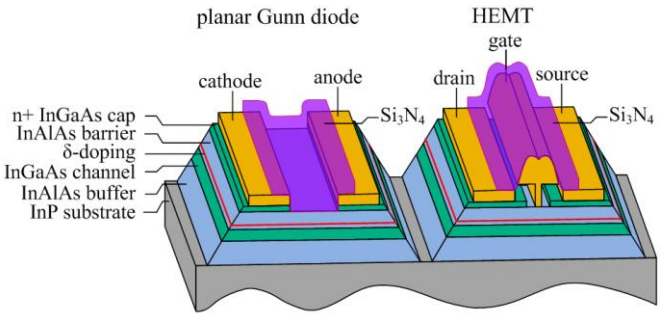


Fig. 1. Cross-section illustration of the co-fabricated planar Gunn diode and the HEMT (not to scale).

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types of devices on the same layers. A new 70 nm T-gate technology has been used for the enhancement of the high frequency response of the transistor. The detailed layer structure and the fabrication procedure of the HEMT are described extensively in the next section. In addition, the fabrication process of the Gunn diode is also described in detail, presenting the required compatibility with the HEMT material system.

## II. Fabrication of the Devices

The layer structure used in this work was grown on a 355 $\mu$m thick substrate of InP, using molecular beam epitaxy (MBE). We chose to have our designs on a proven layer structure with a Hall mobility (μH) of $2.1\times10^{12}$ cm$^{-2}$ and sheet carrier concentration ($n_{sh}$) of 7500 cm$^2$/Vs [13]. A 200 nm thick un-doped $In_{0.52}Al_{0.48}As$ buffer layer was grown on the top of the InP substrate, followed by an un-doped 15 nm thick $In_{0.53}Ga_{0.47}As$ channel layer. A 3 nm thick layer of $In_{0.52}Al_{0.48}As$ was grown afterwards to form the spacer layer. A Si delta-doping layer with $6\times10^{12}$ cm$^{-2}$ density was deposited on the top of the spacer, followed a 14 nm thick $In_{0.52}Al_{0.48}As$ barrier layer. The growing process was complete after the deposition of a $In_{0.53}Ga_{0.47}As$ cap layer with 14 nm thickness and doping level of $6\times10^{18}$ cm$^{-3}$.

The first lithographic step incorporates the pattern definition of the Ohmic contacts following the same procedure as presented in [11]. A metal alloy consisting of 14 nm Au / 14 nm Ge / 14 nm Au / 11 nm Ni / 70 nm Au was evaporated for the simultaneous formation of the Ohmic contacts for both devices. The contact resistance resulting from the metal stack on the highly doped $In_{0.53}Ga_{0.47}As$ cap layer is equal to 0.12 Ω.mm.

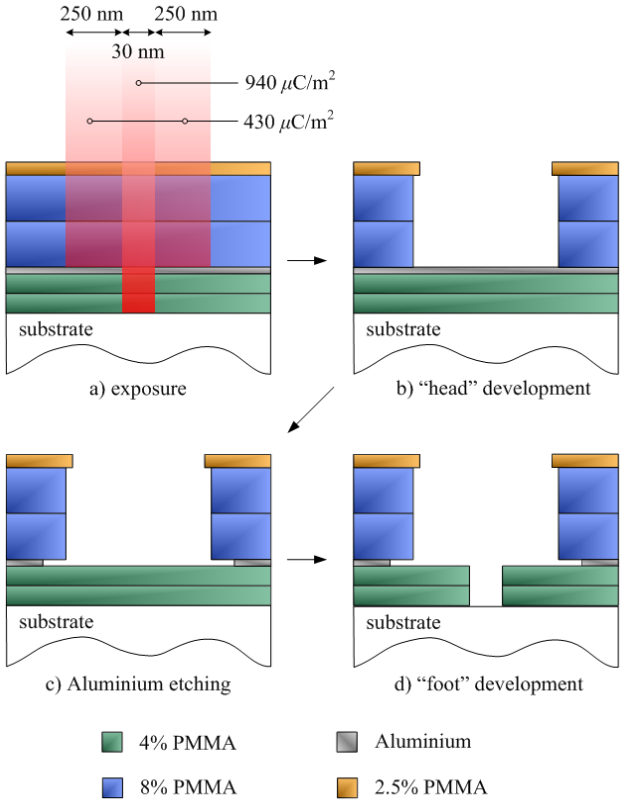


Fig. 2. Schematic diagram of the PMMA/Al/PMMA T-gate technology

After the fabrication of the Ohmic contacts, the mesa areas of the two devices were isolated from the surrounding areas. A 12 % PMMA layer was hard baked in a conventional oven at 180ºC. The samples remained in the oven for two hours to ensure a high resistivity of the mask to the etching solution. After the development of the resist, the samples were processed by a 1 : 1 : 100 - orthophosphoric acid : $H_2O_2$ : $H_2O$ solution for 120 s. The isolation of the two devices was tested during the etching procedure via electrical measurements.

The stepped profiles for the implementation of T-gates have traditionally been created by 3D EBL techniques where different doses are assigned on resist layers with different sensitivities as in UVIII/LOR/PMMA systems [14, 15]. Thus, a sharp profile is created between the "head" and the "foot" areas due to the high contrast of the sensitivities between the two layers. In this work, a new technique is presented using exclusively PMMA resist as presented in Fig. 2. The PMMA layers were spun at 5 krpm for 60 s and baked at 155ºC on a hot plate for 90 s, individually.

Following the conventional exposure technique, a low dose is assigned at the side patterns for the formation of the "head" area. A high dose is assigned afterwards in the middle section to create the T-gate "foot". However, the different PMMA layers do not have a high contrast between them and the resulting depth of the "head" area varied due to temperature and timing variations in the development process [16]. The sharp profile between the top and the bottom PMMA layers was created after the introduction of an intermediate aluminium layer with 10 nm thickness. The Al layer creates a threshold since the electron beam with a relatively low dose of 430 $\mu$C/m$^2$ is sufficiently back-scattered so that the layers underneath are under-exposed. Therefore, the low dose exposure is used for the formation of the "head" pattern on the top 8 % PMMA layers. On the other hand, the high dose equal to 940 $\mu$C/m$^2$ assigned in the middle of the design adequately penetrates the Al layer, exposing the resist stack down to the substrate. Therefore, the "foot" pattern is created at the bottom 4 % PMMA layers. The top 2.5 % PMMA layer has a higher molecular weight compared to the 8 % PMMA layer underneath, creating the required undercut profile for the lift-off process. A 70 nm "foot" window resulted from the 30 nm line design due to the increased forward scattering caused by the multiple PMMA/Al layers. However, the current technique is simple to implement since only one registration job is required.

The opening of the T-gate window is performed in 3 steps. Initially, a 2.5 : 1 IPA : MIBK developer solution kept at 23 ºC is applied for 40 s, removing the top three PMMA layers. The MF-CD-26 (Microposit$^{TM}$) solution is applied for 100 s afterwards, etching the Al layer sufficiently for the exposure of the bottom layers. Finally, a second treatment with the MIBK solution is applied for 40 s for the development of the "foot" pattern.

Following the creation of the T-shaped resist profile, the recess etching procedure was performed for the removal of the highly doped cap layer using a succinic acid solution. The pH of the solution was adjusted to 5.9 and the samples were processed for 16 s. Afterwards, a de-oxidising process was applied using a 10 : 1 $H_2O$ : Ammonia solution for 20 s and the gate area was metallised using a conventional 15 nm / 15 nm Pt / 400 nm Au metal alloy.

Finally, the areas between the drain and the source were passivated using a $Si_3N_4$ film. Prior to the dielectric deposition, a bi-layer of PMMA was spun and the windows were opened around the gates. An ICP-CVD process was used in the next, for the deposition of the $Si_3N_4$ film. This process was executed at room temperature preventing the diffusion of the gate metal in the semiconductor and any melting of the PMMA. In the end, the unwanted dielectric was removed following a lift-off process.

The coplanar waveguide pads of both devices were deposited afterwards using a metal stack of 20 nm Ti / 500 nm Au, presenting 50 Ω of characteristic impedance. The fabrication process continued with the removal of the cap layer between the anode and the cathode of the diode. Similarly to the recess etching process of the HEMT, the same succinic acid solution was applied for the selective removal of $In_{0.53}Ga_{0.47}As$ between the diode electrodes. A target current level of 60 mA was set for 120 $\mu$m wide Gunn diodes, according to [12], indicating the end point of the process. The corresponding current density, which is equal to 500 mA/mm, is in agreement with the current density of the HEMT as presented in the next section. Finally the areas between the anode and the cathode of the diode were de-oxidised using a 4 : 1 $H_2O$ : HCl solution and passivated with $Si_3N_4$ following the same process described for the transistor.

The most significant advantage of the procedure described above is the common execution of the majority of the fabrication steps for both the Gunn diode and the HEMT. Only the passivation procedure is executed individually due to the different de-oxidising solutions required for the exposed InAlAs barrier layer of the HEMT and the InGaAs cap layer of the Gunn diode. The complete Gunn diode and HEMT are shown in Fig. 3 and a more detailed image of the HEMT before the deposition of the passivation layer is presented in Fig. 4.

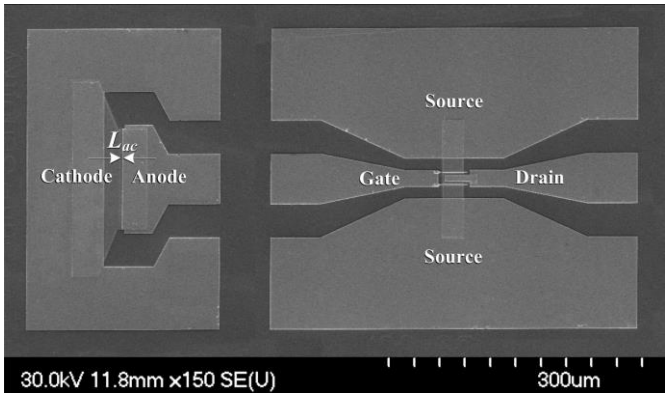


Fig. 3. Scanning electron microscope picture of the fabricated 120 $\mu$m wide Gunn diode with 1 $\mu$m $L_{ac}$ (left) and the 25 $\mu$m wide HEMT with 2x70 nm T-gates (right).

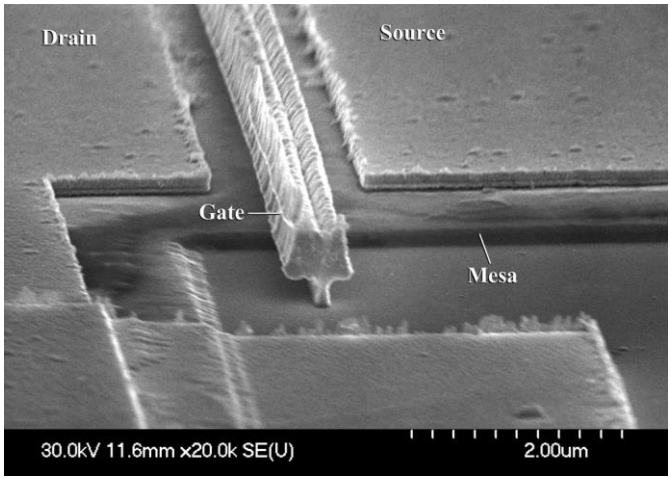


Fig. 4. Detailed scanning electron microscope picture of the fabricated HEMT structure. The drain-to-source separation is equal to 1.5 $\mu$m.

## III. Results and Discussion

An Agilent Technologies B1500A semiconductor analyser was used for the DC characterization of the devices. Fig. 5 illustrates the drain current of the fabricated transistors versus the drain voltage for different biasing voltages applied at the gate. The measurements correspond to HEMTs with two-finger 70 nm T-gates and 25 $\mu$m width. The devices present a maximum current density of 560 mA/mm for 1 V $V_{DS}$ and 0.8 V $V_{DS}$ where a $V_{GS}$ of -0.6 V is required for the pinch-off of the transistor. The transconductance performance is depicted in Fig. 6 showing a maximum value of 520 mS/mm for 0.6 V $V_{DS}$ and -0.15 V $V_{GS}$ biasing conditions.

Two Agilent vector analysers were used for the small-signal characterisation of the HEMTs for the frequency range between 10 MHz - 110 GHz and 140 - 220 GHz. Following the characterisation of the HEMTs, the tapers performing the CPW transition from 40 $\mu$m-60 $\mu$m-40 $\mu$m to 15 $\mu$m-20 $\mu$m-15 $\mu$m ground-signal-ground configuration (Fig. 3), were de-embedded. The Ansoft HFSS electromagnetic modeling tool

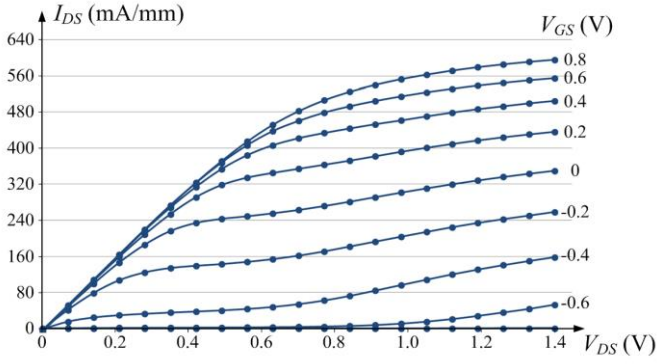


Fig. 5. Current-voltage ($I_{DS}$ - $V_{DS}$) characteristics of the 2x70 nm T-gate HEMT with 25 $\mu$m width for variable $V_{GS}$.

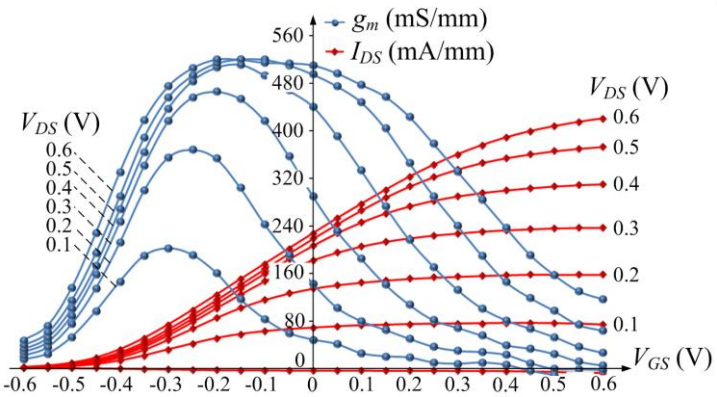


Fig. 6. Transconductance-voltage ($g_m$ - $V_{GS}$) characteristics (blue curves) and current-voltage ($I_{DS}$ - $V_{GS}$) characteristics (red curves) for variable $V_{DS}$.

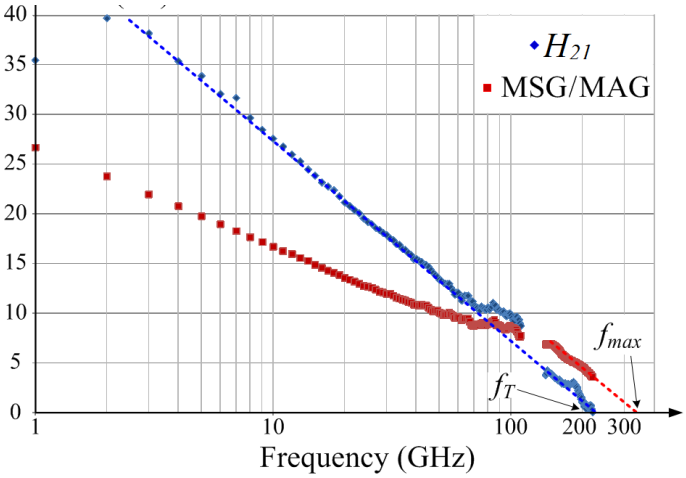


Fig. 7. Current gain $H_{21}$ and maximum stable/available gain (MSG/MAG) as a function of the operation frequency for the 2x25 $\mu$m wide HEMT. The $f_{max}$ and the $f_T$ after de-embedding the transition pads are 330 GHz and 220 GHz, respectively.

was used for the simulation of the small signal characteristics up to 110 GHz. For the frequency range between 140 - 220 GHz, the transition pads were characterised using two Picoprobe GSG probes with 100 $\mu$m and 50 $\mu$m pitch. The maximum stable/available gain (MSG/MAG) and the current gain $H_{21}$ of the 2x25 $\mu$m devices are presented in Fig. 7 after de-embedding the transition pads. The devices biased at -0.15 V $V_{GS}$ and 1.0 V $V_{DS}$ demonstrate an $f_T$ of 220 GHz and $f_{max}$ equal to 330 GHz.

An E4448A Agilent technologies spectrum analyser was used for the investigation of the Gunn diode oscillations. An ACP 110-100 GSG CascadeMicrotech probe and a WHMP-10 Faran Technology mixer were used for the detection of oscillations in the W-band. A Picoprobe GSG probe with 100 $\mu$m pitch and a WR-05 Faran Technology mixer were used for the investigation of the frequency range between 140 - 220 GHz. After the identification of the oscillation frequencies, the mixers were replaced by a PM4 Ericson power meter for the accurate measurement of the generated power. The losses introduced by the probes were also subtracted from the power measurements.

Devices with 60 $\mu$m and 120 $\mu$m width and various $L_{ac}$ designs were fabricated, where the 120 µm wide diodes presented superior power performance over the 60 µm devices. Fig. 9 illustrates the measured spectrum of a Gunn

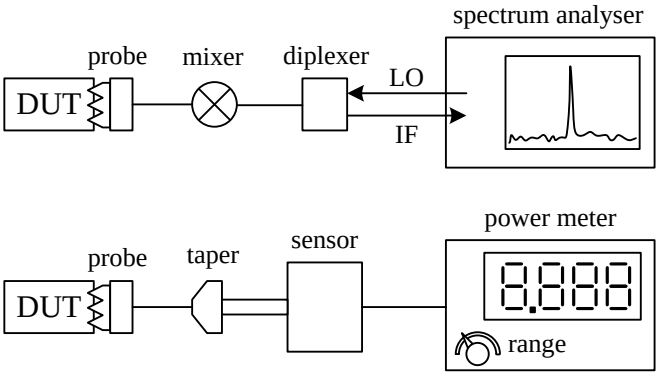


Fig. 8. Experimental set-up for frequency and power characterisation.

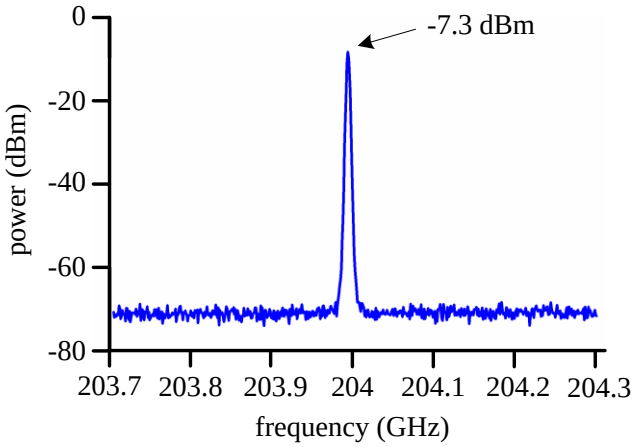


Fig. 9. Measured spectrum of the 120 $\mu$m wide Gunn diode with 1 $\mu$m $L_{ac}$ biased at 3.2 V.

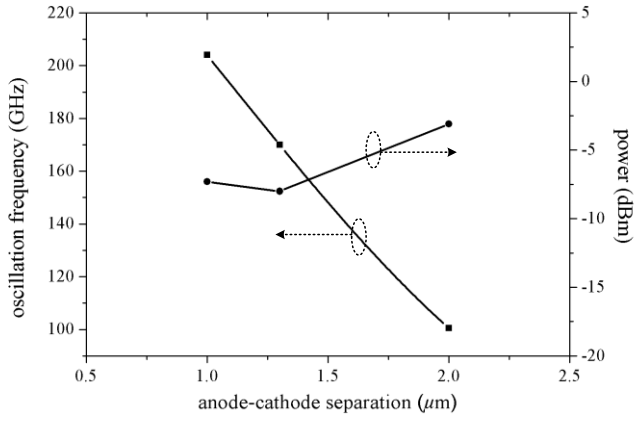


Fig. 10. Dependence of the oscillation frequency and the generated power for 120 $\mu$m wide devices with various $L_{ac}$.

diode with 1 $\mu$m $L_{ac}$ and 120 $\mu$m width biased at 3.2 V. The device generates oscillations at 204 GHz with -7.3 dBm maximum output power. The oscillation frequency and the generated power for devices with various $L_{ac}$ are depicted in Fig. 10. The frequency dependence follows the same rule as reported in [12] for devices with $In_{0.53}Ga_{0.47}As$ channel. The generated power was found to be unrelated to the $L_{ac}$, remaining as approximatly -6 dBm for all the devices. These new devices therefore produce similar power levels to those devices presented in [12] (-10 dBm), where the layer structure was exclusively designed for the fabrication of planar Gunn diodes. The maximum measured power in this work was equal to -3.1 dBm for devices with 2 $\mu$m $L_{ac}$ at 130GHz.

The presented results show a great potential for the implementation of high-power high-frequency oscillators consisting of planar Gunn diodes and HEMTs. The diode itself demonstrates excellent characteristics and the future integration with a transistor amplifier is expected to enhance significantly the output power. Additionally, a possible implementation of a HEMT-based mixer circuit could boost the generated frequencies in the terahertz regime.

The new 70 nm T-gate technology was used for the demonstration of HEMT devices with very good high frequency performance, compared to similar geometries [13, 17]. However, the reduction of the T-gate length in the range of 30 nm-50 nm is required for the enhancement of the gain performance in the D-band (110-140 GHz) and above. In a future development of the T-gate technology, the foot area could be exposed after the removal of the head area. Thus a shorter gate length would result from the reduced forward scattering of the e-beam. Since no rapid thermal annealing (RTA) process is required in this process, a self-aligned technique can also be applied, providing significant advantages as demonstrated in [18]. The current and transconductance of the HEMTs could be increased by the addition of a second δ-doping layer in future impelementaions [17]. The addition of an extra dopping layer is also expected to introduce additional offers for the power performance of the Gunn diode [8].

## IV. Conclusion

The integration of planar Gunn diodes and HEMTs on an InP substrate has been presented for the first time in this work. The maximum frequency of oscillation equal to 204 GHz for planar Gunn diodes has been demonstrated from devices with 1 $\mu$m $L_{ac}$ and 120 $\mu$m width. The power levels of the diodes are also very promising where -3.1 dBm maximum generated power has been measured for 2 $\mu$m devices. The HEMTs present $f_T$ of 220 GHz and $f_{max}$ of 330 GHz and the performance of the devices is expected to improve significantly after the reduction of the gate length and the use of a self-aligned technique. The technology presented demonstrates excellent characteristics for the implementation of high-power, high-frequency MMIC oscillators.

## V. Acknowledgements

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