Integration Techniques of pHEMTs and Planar Gunn Diodes on GaAs Substrates

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Abstract

This work presents two different approaches for the implementation of pseudomorphic high electron mobility transistors (pHEMTs) and planar Gunn diodes on the same gallium arsenide substrate. In the first approach, a combined wafer is used where a buffer layer separates the active layers of the two devices. A second approach was also examined using a single wafer where the AlGaAs/InGaAs/GaAs heterostructures were designed for the realisation of pHEMTs. The comparison between the two techniques showed that the devices fabricated on the single pHEMT wafer presented superior performance over the combined wafer technique. The DC and small-signal characteristics of the pHEMTs on the single wafer were enhanced after the use of T-gates with 70 nm length. The maximum transconductance of the transistors was equal to 780 mS/mm with 200 GHz maximum frequency of oscillation (f_{max}). Planar Gunn diodes fabricated in the pHEMT wafer, with 1.3 μm anode-to-cathode separation (L_{AC}) presented oscillations at 87.6 GHz with maximum power of oscillation equal to -40 dBm.

I. INTRODUCTION

The first planar Gunn diodes presenting oscillations above 100 GHz [1] demonstrated the capability of integrating millimeter-wave sources with monolithic microwave integrated circuits (MMICs). The development of the device in subsequent years was focused on the modification of the layer structure for the reinforcement of the power performance since the initial diodes presented relatively low generated power equal to -43 dBm. The generated power was doubled and the phase noise significantly decreased after the introduction of extra delta-doping layers [2]. The introduction of $In_{0.23}Ga_{0.77}As$ channel layers led to an increase of the maximum oscillation frequency to 116 GHz [3]. Lately, planar Gunn diodes based on an $In_{0.53}Ga_{0.47}As$ channel layer presented significantly improved performance where the maximum frequency of oscillation was equal to 164 GHz with -10 dBm maximum power generated [4].

Alternatively, enhancement of the oscillator performance can be achieved by the monolithic implementation of the planar Gunn diode with transistor-based MMICs. Transmitters and receivers operating at 60 GHz [5] and Q-band high power amplifiers [6] are examples of MMICs based on GaAs pHEMTs that would benefit from a low phase noise oscillator. By integrating the Gunn diode on the same chip as the pHEMTs we can retain the advantages of a Gunn diode, such as superior

phase noise, whilst using transistor gain to increase the oscillation power. Clearly, opportunities to develop more sophisticated hybrid device MMICs could be possible.

This work investigates the implementation of planar Gunn diodes and the pHEMTs on the same substrate for the future fabrication of high-power, high-frequency MMIC oscillators. Several examples of transistors integrated with other active devices have been demonstrated in the past like the implementation of HEMTs with resonant tunneling diodes (RTDs) [8] and p-i-n photodiodes [9].

Two different approaches are presented for the implementation of the planar Gunn diode and the pHEMT on the same substrate. Initially, the first technique is described in detail where the combined wafer consists of two groups of active layers that were independently optimized for the individual implementation of the two devices. A buffer layer is used for the isolation of the two devices. In another approach, a single wafer designed for the realization of GaAs - based pHEMTs was used for the implementation of both devices. In this technique a compromise has been conducted since the layer structure was not designed for the implementation of Gunn diodes. The latter approach demonstrated the first successful implementation of both devices on the same substrate for the first time, as presented in [10]. A 70 nm T-gate technology was incorporated for the optimization of the DC and the small-signal characteristics of the transistor. In the next sections, the fabrication procedures and the characterization techniques performed for both approaches are described in detail.

II. The combined wafer approach

A. *Wafer structure*

The design of the combined wafer consists of two groups of active layers separated by a thick buffer of GaAs. Initially, the active layers of the Gunn diode were grown on a 620 μm thick GaAs substrate, using molecular beam epitaxy (MBE). The layer structure selected in this design for the realisation of the diode includes two GaAs channel layers that contribute mutually to the current conduction, sandwiched by 2 delta-doping layers each, as presented in [11]. Only the cap layer of the current design has

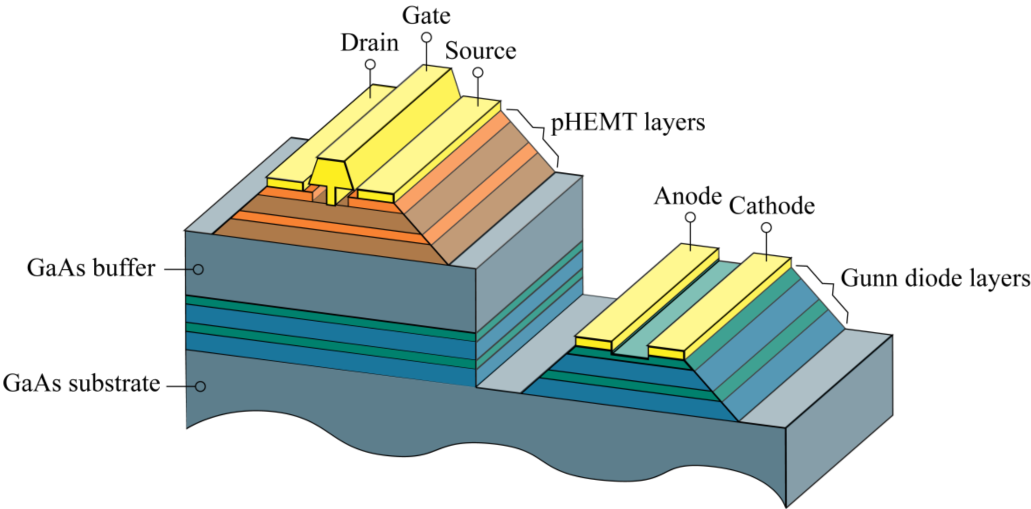

Figure 1. The general layer structure of the combined wafer approach (not to scale).

been amended, where the graded GaAs/InGaAs structure has been replaced by highly-doped GaAs. This modification is required in order to avoid a lattice mismatch appearing between the top InGaAs surface with high Indium content and the GaAs buffer grown on top. In addition, the thickness of the cap layer is increased to 150 nm, providing an error margin while etching the top layers.

A thin layer of 5 nm lattice matched AlGaAs is deposited between the Gunn cap layer and the GaAs buffer layer. This performs as an etch-stop layer providing high accuracy while reaching the top of the Gunn structure, removing the pHEMT layers and the buffer. As described above, a GaAs buffer is grown after the Gunn layers where the thickness of the layer is equal to 1.1 μm ensuring electrical isolation between the two devices. The pHEMT layer structure, similar to the one presented in [12], is grown on the top of the buffer completing the growing procedure. The detailed layer structure of the combined wafer is presented in Table 1. The procedure of reaching the Gunn layers and the fabrication of the diode, are described in detail in the next section.

Material	Doping Level	Thickness (nm)	Description	
GaAs	4×10^{18} cm^{-3}	30	cap	**pHEMT layers**
$Al_{0.3}Ga_{0.7}As$		5	etch stop	
GaAs		2.5	oxidisation stop	
$Al_{0.3}Ga_{0.7}As$		7	barrier	
GaAs		2 ML		
Si delta doping	7×10^{12} cm^{-2}			
GaAs		3ML		
$Al_{0.3}Ga_{0.7}As$		5	spacer	
$In_{0.2}Ga_{0.8}As$		10	channel	
GaAs		50	buffer	
Super lattice		5 periods		
GaAs		400		
Super lattice		50 periods		
GaAs		1100	pHEMT-Gunn isolation	
$Al_{0.8}Ga_{0.2}As$		5	etch stop reaching Gunn	
GaAs	3.5×10^{18} cm^{-3}	150	cap	**Gunn layers**
$Al_{0.8}Ga_{0.2}As$		5	etch stop	
GaAs	3.5×10^{18} cm^{-3}	15	Gunn surface	
$Al_{0.22}Ga_{0.78}As$		10		
Si delta doping	8×10^{11} cm^{-2}			
$Al_{0.22}Ga_{0.78}As$		10		
GaAs		50	channel	
$Al_{0.22}Ga_{0.78}As$		10		
Si delta doping	8×10^{11} cm^{-2}			
$Al_{0.22}Ga_{0.78}As$		10		
$Al_{0.22}Ga_{0.78}As$		10		
Si delta doping	8×10^{11} cm^{-2}			
$Al_{0.22}Ga_{0.78}As$		10		
GaAs		50	channel	
$Al_{0.22}Ga_{0.78}As$		10		
Si delta doping	8×10^{11} cm^{-2}			
$Al_{0.22}Ga_{0.78}As$		10		
GaAs		620 um		

Table 1. The detailed layer structure of the combined wafer.

B. Reaching the Gunn diode surface

A dry-etching procedure was followed for removing the pHEMT and buffer layers to access the Gunn layers. Dry etch was chosen instead of wet etch because of higher uniformity [13]. A Hydrogen Silsesquioxane (HSQ) negative electron beam resist was chosen for this step. The HSQ layer was initially spun at 6 k rpm and then baked at 90 ^{o}C for 15 minutes. The areas that are to remain for the protection of the transistor layers are exposed to the electron beam and the complementary windows are opened after the development of the HSQ. Electron beam lithography (EBL) has been used exclusively in this work using a Vistec Microsystems VB6 vector beam exposure tool.

The transistor and the buffer layers were then etched, using a reactive ion etching (RIE) technique with a silicon-tetrachloride ($SiCl_4$) gas environment. A test run was conducted prior to the actual fabrication, where an interferometer was used for the complete monitoring of the layer structure. In this step, the whole layer stack was removed reaching the semi-insulating GaAs substrate. The interferometer response that resulted from the test run is depicted in Figure 2 with the pHEMT, buffer, Gunn and substrate areas highlighted. The same test procedure was performed three more times. The total etching time was different between the tests due to the varying condition of the RIE chamber. However, the same sequence of maximums and minimums was observed demonstrating the repeatability of the process

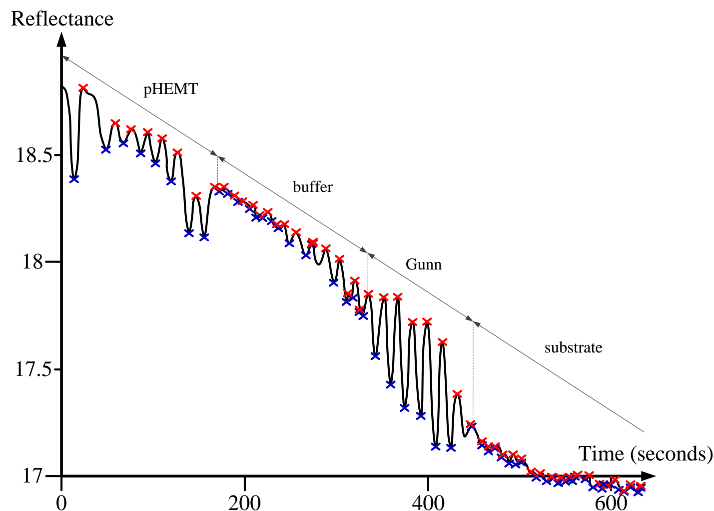

Figure 2. The interferometer response after the complete etching test run. The red and the blue marks indicate the local maximums and minimums of the reflectance, respectively.

For the fabrication of the actual Gunn diodes, the monitored dry-etching process was stopped before reaching the Gunn layers, leaving an error margin after the interruption of the etching. A wet-etching treatment was applied afterwards in steps of 30 s for reaching the AlGaAs etch stop layer. A 3:1 - $C_6H_8O_7$:H_2O_2 citric acid solution was used in this procedure, where the successful end of the etch stop layer was examined using a Dektak profilometer. Finally, a 10:1 buffered hydrofluoric acid (HF) solution was applied for 30 s for the removal of the AlGaAs layer.

C. Fabrication of planar Gunn diode.

After removal of the top layers it was possible to fabricate the Gunn diode. The first lithographic step was the definition of the mask windows before the evaporation of the metal for the Ohmic contacts using a bi-layer of 12 % and 2.5 % dissolved polymethyl methacrylate (PMMA). Each individual layer was spun at 5 krpm for 60 s and baked at 155 ^{o}C on a hot plate for 90 s. An adjusted electron dose was applied for the correction of the proximity effect, maintaining a constant distance between the electrodes. After the development of the resist, the metal alloy for the formation of the Ohmic contacts was deposited, consisting of 14 nm Au / 14 nm Ge / 14 nm Au / 11 nm Ni / 70 nm Au. The samples where annealed at 300 ^{o}C for 20 s followed by 30 s at 360 ^{o}C, resulting a contact resistivity of the electrodes equal to 0.25 Ω.mm.

The mesa areas of the devices were isolated in the next step. A 12 % PMMA layer was hard baked in a convention oven at 180 ^{o}C for two hours in order to get the required resistance to the wet-etch. After the development of the resist, the surrounding areas were etched away using a 10:1 - $C_6H_8O_7$:H_2O_2 citric acid solution for 180 s. In the following step, a metal stack of 20 nm Ti/500 nm Au was deposited to form the coplanar waveguide (CPW) pads with characteristic impedance of 50 Ohms for the characterisation of the devices. At the end of the fabrication procedure, the cap layer between the electrodes of the Gunn diode was partially etched. The current level was reduced by using small etch steps to avoid device burning, caused by the high electric field appearing close to the ohmic contacts [14]. A succinic acid solution with adjusted pH at 5.9 was incrementally applied in short steps until the reduction of the current to the same level as presented in [11]. Devices with various geometric characteristics were fabricated, with widths from 30 μm to 120 μm and L_{ac} from 1 μm to 4 μm.

D. Characterisation and results

The DC characterization of the diodes was performed using an Agilent Technologies B1500A semiconductor analyser. The current versus the applied voltage (*I-V*) of a fabricated planar Gunn diode with 60 μm width and 2 μm L_{AC} is shown in Figure 3. The diode presents a promising negative differential resistance (NDR) after the biasing voltage of 2.1 V. An Agilent Technologies E8361A vector network analyser (VNA) with frequency extenders for measurements up to 110 GHz was used for an initial signal identification [11]. Figure 4 illustrates the $|s_{11}|$ response from the same 2 μm device biased at 2.5 V. A maximum value of 1 dB is observed around the frequency of 60 GHz which is the highest s_{11} response between all the tested devices.

The oscillation of the diodes was further investigated using an E4448A Agilent Technologies spectrum analyser. An ACP 110-100 GSG CascadeMicrotech W-band probe was used in combination with a WHMP-10 Faran Technology W-band mixer. The latter was used for the extension of the measured frequency range of the spectrum analyser. However, no oscillations were detected in any device regardless of the design geometry and the biasing conditions.

Further tests were performed for the identification of the reasons causing the poor device performance. Test contacts for the transmission line method (TLM) were fabricated on the top cap layer of the pHEMT as well as on the cap layer of the Gunn structure. Approximately equal resistivity values resulted for the TLM structures in both levels with 0.25 Ω.mm and 0.29 Ω.mm for the Gunn and the pHEMT level, respectively. Additional measurements using the profilometer showed that the thickness value of the Gunn cap layer remained above 120 nm after removing the top layers. As a result, the measured sheet resistance of the Gunn level was approximately 3 times smaller than for the pHEMT level (65 Ω/□ over 215 Ω/□). The test samples were

further processed and the highly-doped sections between the TLM pads were removed. The Gunn TLM pads showed extremely high resistivity without Ohmic behaviour.

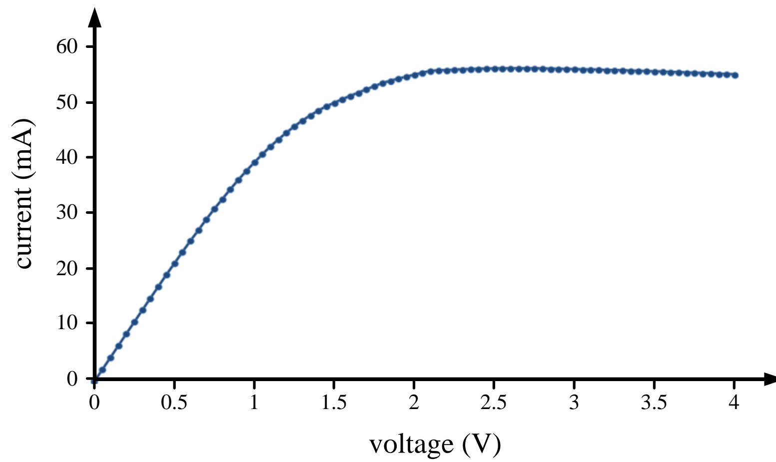

Figure 3. The current-voltage (*I-V*) characteristics of the 60 μm - wide Gunn diode with 2 μm L_{AC}, fabricated after the removal of the HEMT and the buffer layers.

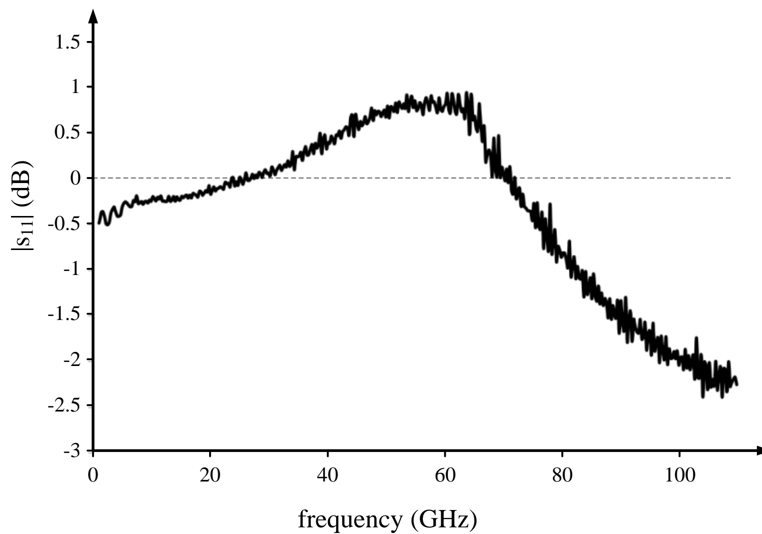

Figure 4. The $|s_{11}|$ response of a 60 μm - wide Gunn diode with 2 μm L_{AC} as a function of frequency.

The above tests indicate that the thickness of the Gunn cap layer remains unchanged after removing the top layers. Thus, after the annealing procedure the ohmic contacts have not been diffused down to the channel layer. The very high resistance accessing the channel significantly degrades the performance of the devices, suppressing any growing oscillations. A future design of the layer structure could include a Gunn cap layer with a thickness of the order of 40 nm.

III. THE SIDE-BY-SIDE APPROACH

The implementation of the first planar Gunn diodes operating above 100 GHz [1] has been inspired by the first simulation [15] and experimental results [16] that presented Gunn oscillations on HEMT layer structures. Thus, the operation of planar Gunn diodes using a pHEMT layer structure was also examined, in parallel with the process of the combined wafer. The layer structure of the pHMET wafer is identical to the transistor layers presented previously for the combined wafer. The side-by-side implementation of the two devices using the same epitaxial layers is illustrated in Figure 5. The current technique presents comparable simplicity since both devices are implemented on the same level, sharing most of the fabrication steps.

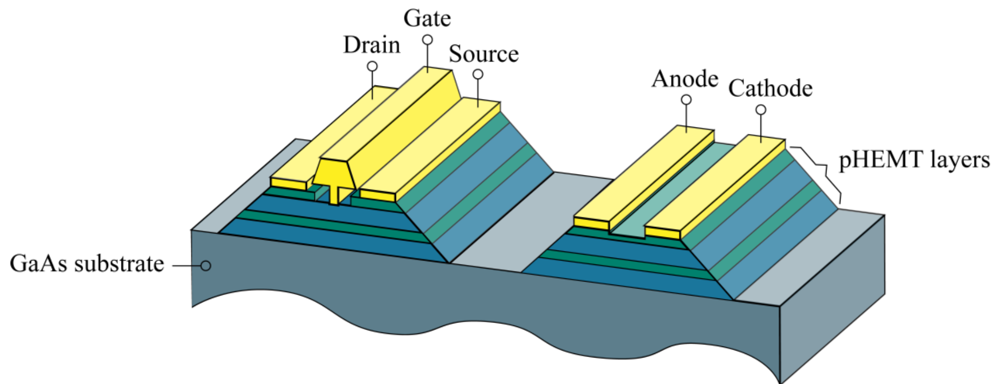

Figure 5. The side-by-side approach using the pHEMT wafer (not to scale).

A. Fabrication procedure

In the first fabrication step, the drain and source electrodes of the transistor were deposited at the same time with the anode and cathode electrodes of the diode. The same metallurgy and annealing strategy, as described above for the Gunn diode, were followed in this process. The contact resistivity of the electrodes in this wafer was equal to 0.29 Ω.mm. The mesa areas of both devices were isolated simultaneously following the same technique described in the previous paragraph.

The next fabrication steps incorporate the recess etching of the cap layer and the implementation of the T-shaped gate of the transistors. A 3D EBL technique was applied on a stack of multiple PMMA layers for the formation of the T-gates. Two layers of 4 % PMMA were deposited initially for the definition of the T-gate foot and the next two layers of 12 % PMMA were deposited for the formation of the T-gate head. A final layer of 2.5 % was used for the creation of the undercut needed for the lift-off process. Each layer was spun at 5 k rpm for 60 s and baked at 155 ^{o}C on a hot plate for 90 s individually. A high dose of electrons was applied in the middle of the patterns, penetrating the total resist stack for the creation of the foot areas. A lower dose, which does not expose the bottom 2.5 % PMMA layers, was applied at the sides of the patterns for the formation of the head areas. The recess etching was performed after developing the resist, using the same succinic acid solution used in the previous technique for 20 s. The T-gate fabrication was completed after the evaporation of a 15 nm Ti/15 nm Pt/400 nm Au metal stack for the formation of the Schottky gate contact.

Similarly to the combined wafer approach, the CPW pads were evaporated afterwards and the cap layer between the Gunn electrodes was partially removed. A PMMA layer was spun to protect the transistors and the succinic acid solution was applied

in short steps to the diodes. The process was stopped after 7 s when the diode current was reduced to the same level as the current of the transistor presenting maximum transconductance. Figure 6 illustrates the scanning electron microscope (SEM) image of a complete 2-finger transistor. The T-gate profile is presented in the inset of Figure 6, where the foot length is approximately equal to 70 nm. Figure 7 illustrates an optical image of a 60 μm - wide planar Gunn diode with 1.3 μm L_{AC}.

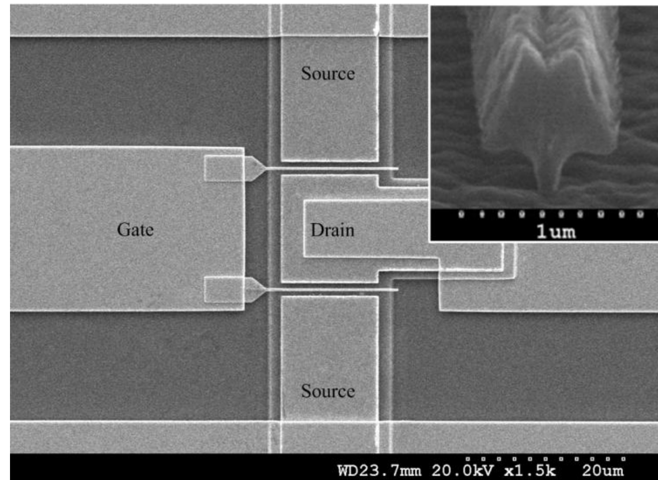

Figure 6. SEM image of the fabricated 2x12 μm - wide device with 1.5 μm drain-to-source separation and the cross section of the 70 nm - long T-gate (inset) [10].

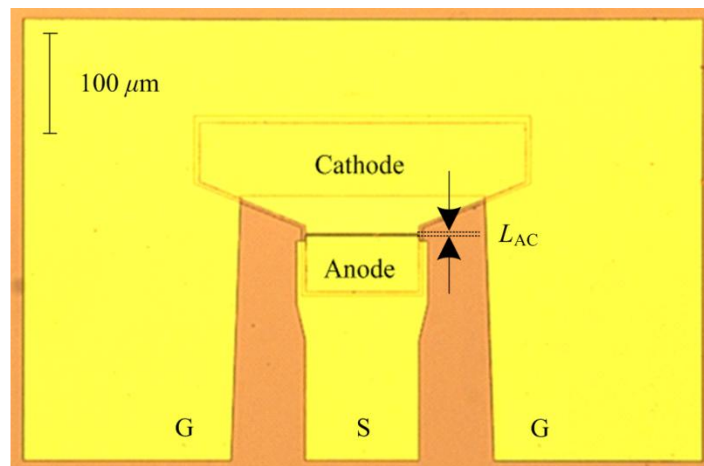

Figure 7. Optical image of the 60 μm - wide Gunn diode with 1.3 μm L_{AC}. The signal pad is 60 μm wide and the signal-ground gap of the CPW is 40 μm [10].

B. Results and Discussion

Figure 8 illustrates the drain current versus the applied drain voltage for the HEMT with 70 nm gate length, under various gate bias. The device shows excellent current density with a maximum drain current of approximately 780 mA/mm with 1 V gate bias. The device is pinched-off after applying a gate bias below to -600 mV. The transconductance of the transistor under

various bias conditions is depicted in Figure 9. The device shows a maximum transconductance equal to 780 mS/mm with gate and drain bias equal to 250 mV and 1.0 V, respectively, indicating that the device operates in enhancement mode. The performance of the device can be improved by applying the recess etching treatment for a shorter period.

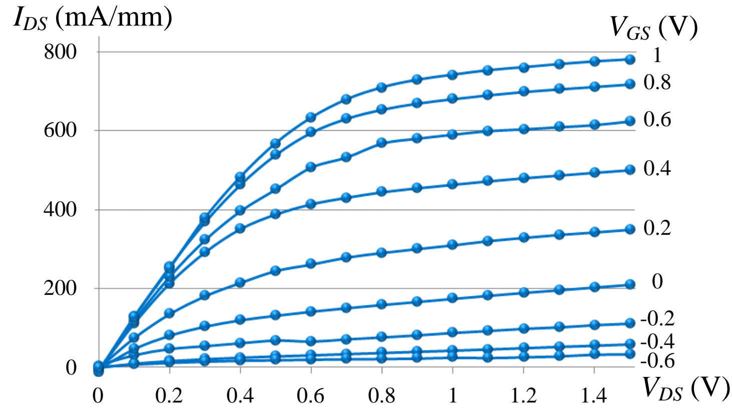

Figure 8. Current-voltage (I_{DS} - V_{DS}) characteristics of the pHEMT under various gate bias [10].

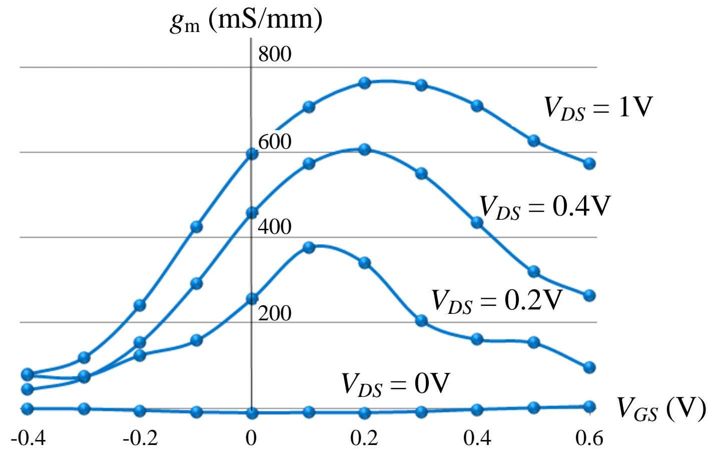

Figure 9. The transistor transconductance as a function of the gate voltage (g_m - V_{GS}) under various drain bias V_{DS} [10].

The small-signal characteristics for a 12 μm - wide device are illustrated in Figure 10 where the current gain $H(2,1)$ and the maximum available/stable gain (MAG/MSG) are shown as a function of frequency. After applying 200 mV and 1 V biasing at the gate and the drain, respectively, the transistor presents 90 GHz cut-off frequency (f_T) and 200 GHz maximum frequency of oscillation (f_{max}). The DC and small-signal performance of the current device is comparable with the state-of-the-art pHEMTs fabricated on GaAs [17, 18].

The I-V characteristic of a 60 μm - wide planar Gunn diode with 1.3 μm L_{AC} is presented in Figure 11. The device presents an NDR between the bias voltage of 2.3 V and 2.6 V, which is difficult to observe due to the impact ionisation effect. A more detailed picture of the NDR region is presented in the inset of Figure 11.

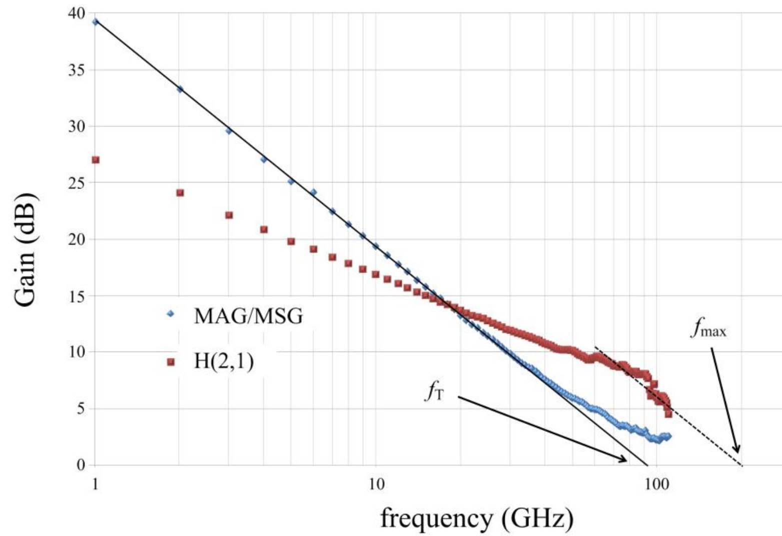

Figure 10. The current gain H(2,1) and the maximum available/stable gain (MAG/MSG) as a function of frequency, for a 2x12 μm - wide transistor. The cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) are 90 GHz and 200 GHz, respectively [10].

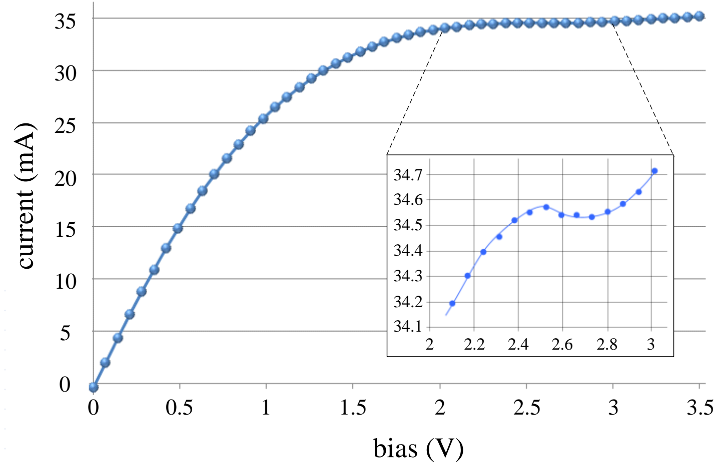

Figure 11. The current-voltage (I-V) characteristics of the 60 μm - wide Gunn diode with 1.3 μm L_{AC} and the negative differential resistance (inset) hardly observed, due to the impact ionisation effect [10].

The spectrum analyser setup was used for the detection of the Gunn diode oscillations. Figure 12 illustrates the measured spectrum of the device presented above, one of the first oscillating devices implemented side-by-side with a pHEMT [10]. The power level generated by the diode was defined using a PM4 Erickson power meter, considering the loss introduced by the

probe (-2.5 dB). The device oscillates in the fundamental mode at 87.6 GHz and the maximum output power is equal to -40 dBm after applying a bias of 3.42 V.

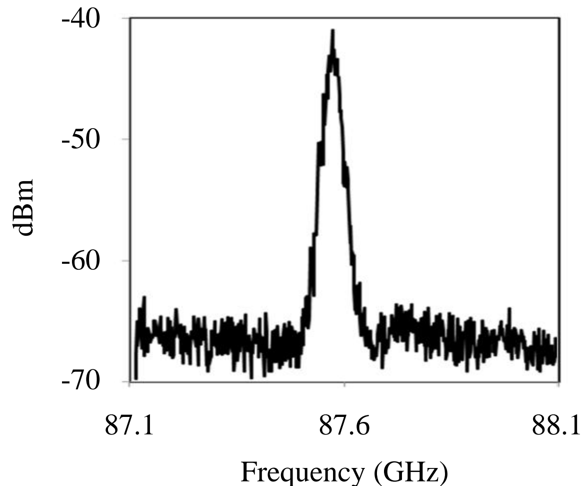

Figure 12. The measured spectrum of a 60 μm – wide planar Gunn diode with 1.3 μm L_{AC} [10].

The above results are encouraging for the future implementation of high-power, high-frequency, low phase noise MMIC oscillators. The generated power is relatively low, being however in the same order as the power of the first high-frequency planar Gunn diode [1]. Future development of the layer structure is expected to enhance significantly the performance of both devices. The introduction of a graded InGaAs cap layer could decrease the access resistance [19] and the current levels of the devices may be increased by adding extra delta-doping layers [2]. These modifications have the potential to reinforce the generated power of the Gunn diode and the amplifying characteristics of the pHEMT. In addition, the same side-by-side approach could be applied on an Indium Phosphide material system, since planar Gunn diodes with an $In_{0.53}Ga_{0.47}As$ channel layer have recently demonstrated exceptional characteristics [4].

IV. Conclusion

Two different techniques for the implementation of planar Gunn diodes and pHEMTs on the same wafer have been presented in this paper. The combined wafer approach requires a more complicated fabrication procedure, since the exposure of the Gunn layers needs to be conducted in a very uniform way across the wafer. No oscillations were detected due to the increased access resistance of the diode electrodes, which can be decreased after a subsequent thinning of the cap layer. In addition, an air-bridge technology would be needed for the connection of the two devices lying on different levels, introducing more complexity to the fabrication procedure.

By contrast, a simplified process is adequate for the side-by-side implementation, where the majority of the fabrication steps is executed for both devices at the same time. Oscillations at 87.6 GHz were detected from a 1.3 μm Gunn diode with a relatively low generated power, equal to -40 dBm. The pHEMTs using a 70 nm T-gate technology presented 780 mS/mm

maximum transconductance and 200 GHz maximum frequency of oscillation. The diode performance can be improved by the introduction of a graded InGaAs cap layer and extra delta-doping layers. The development of the layer structure is expected to also enhance the transistor characteristics.

V. ACKNOWLEDGEMENTS

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