The impact of strain engineering on hole mobility of $In_xGa_{1-x}As$ channels for III-V pMOSFETs

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Abstract

Whilst the high electron mobility of compound semiconductors makes them attractive for beyond 22 nm CMOS, a key challenge in implementing III-V materials is their modest hole mobility. Addressing this issue motivates an investigation of the impact of strain to optimize the hole transport properties of III-V MOSFET channel materials. In this work, we describe the dependence of hole mobility on the bi-axial compressive strain of $In_xGa_{1-x}As$ layers with indium concentrations in the range 53%-85%. The vertical architecture of the material structure of this study resembles a III-V high mobility transistor where the dopant is spatially separated from the device channel. Mobility and channel carrier concentration were determined using Hall effect measurements. While the 53% In-content (0% strain) structures demonstrated modest mobilities of 60-70 cm^2/Vs, the strained structures exhibited superior transport with the 85% In-content (2.1% strain) channel demonstrating mobilities of 427-433 cm^2/Vs with sheet hole densities of 1.33 x 10^{12}-1.6 x 10^{12} cm^{-2} depending on the doping level used. To our knowledge, the room temperature mobility of the 2.1% strained structures are the highest ever reported for an $In_xGa_{1-x}As$ channel.

I. Introduction

A III-V based compound semiconductor solution appears to be one of the main contenders to improve device performance beyond the 22nm technology node. The motivation to switch to compound semiconductors can be appreciated from the paradigm shift that has occurred in Intel's 45nm technology node. Silicon dioxide, perhaps the foundation to silicon's dominance in the microelectronic industry, has been replaced by a high-k dielectric, gate electrodes have switched back to using metals and epitaxy has been introduced to induce strain to the channel [1]. This technology appears to be analogous to a compound semiconductor based solution with the exception of high mobilities and high saturation velocities that can be gained from compound semiconductors. Although the superior electron mobility of III-V materials makes them attractive for CMOS, there are still a number of challenges to overcome before III-V materials can be considered as potential successors to Silicon technology. One of the key challenges is the realization of a viable pMOSFET [2].

High-speed logic applications necessitate high drive currents at both high, and low drain biases. This in turn requires high mobility and conductivity. While linear drive current is proportional to the conductivity, the saturation drive current in short channel devices, on the other hand, is proportional to both the carrier density and carrier injection velocity. Generally, III-Vs have a lower density of states as compared to Silicon accounting for the lower carrier density. However, III-Vs have superior electron mobility due to their smaller effective mass. As such, the injection velocity is sufficiently high to compensate for the reduced carrier density in the case of electrons. This translates to lower gate delay as compared to Si MOSFETs [2]. On the contrary, the hole mobility of III-V materials presently is comparable to or only slightly better than Silicon. Consequently, the gate delay does not improve appreciably for III-V based p-channel devices.

At present, two alternatives exist to improve the hole mobility for a viable pMOSFET solution. One solution is to use Germanium as a p-channel material due to its superior hole mobility. However, Ge is a narrow bandgap (0.66 eV) semiconductor making it susceptible to band-to-band tunneling. Moreover, the n-channel MOSFET is likely to be based around an $In_xGa_{1-x}As$ channel with $x \geq 0.53$. From a CMOS integration perspective, a pMOSFET based around an $In_xGa_{1-x}As$ material would be ideal. In line with this, the other option is to utilize strain engineering to improve the hole mobility of III-V materials in the device channel. However, the exploration of $In_xGa_{1-x}As$ channel material and device design towards the realization of a viable III-V p-MOSFET have been limited [see Ref. 3-5].

In this paper, we present the design and optimization of a III-V p-channel heterostructure based around an $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ material system. The hole transport properties, primarily carrier concentration and mobility, is investigated by employing bi-axial compressive strain in the $In_xGa_{1-x}As$ channel. The indium concentrations explored ranged from 53% to 85%. To elucidate the underlying physical mechanisms governing hole transport in the device channel, temperature dependent magneto-transport characterization was undertaken. We report the highest hole mobility ever reported for a high indium content channel with a peak mobility of 433 cm^2/Vs for a 85% indium-content (2.1% strain) 7.5nm thick channel.

II. Material Structure Concept

a. 'Implant-free' III-V MOSFET

The architecture of the III-V MOSFET is based on the 'implant-free' device concept [6] shown schematically in Fig. 1. In some respects the vertical architecture looks similar to a

High Mobility Transistor; a smaller bandgap channel is sandwiched between larger bandgap barrier layers within the buried channel heterostructure. Modulation doping is adopted out with the channel, usually a small distance from the top and/or bottom of the channel. This provides for good carrier confinement in the channel and high mobility due to the spatial separation of carriers from the dopant atoms. In other respects, the "implant-free" architecture mimics a conventional MOSFET; surface potential modulation stems from depositing a high-k dielectric that 'unpins' the Fermi level at the dielectric-semiconductor interface. A key feature of the device that sets it apart is the "implant-free' nature of the architecture. Traditional MOSFETs use ion-implanted source-drain extensions. In the "implant-free" architecture, however, the ohmic contacts and the doping plane furnish the access regions and channel with charge carriers. As such, there are no thermal budget constraints involved in activation of implanted regions. Very high drive currents can be generated as a result of the high velocity and low back-scattering of the carriers injected into the channel. Furthermore, the adoption of an appropriate doping arrangement ensures low access resistance as well as depletion of the channel in the gate region by the high workfunction of the metal gate. Therefore, enhancement-mode operation at the right threshold voltages can be achieved. An additional benefit of the architecture is its ability to withstand relatively thick gate dielectric as the gate lengths are scaled. This is only possible because of the good electrostatic integrity and high-mobility channel of the device. This allows for the circumvention of the low density of states in III-V materials and high drive currents at low voltage bias [7].

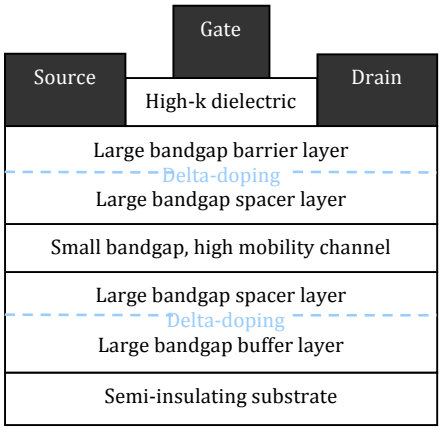

Fig. 1. Schematic of an 'implant-free' III-V MOSFET

b. 'Pre-MOSFET' architecture

Given the current status of high-k dielectric development for non-GaAs based devices, the 'pre-MOSFET' architecture was chosen for materials screening. The pre-MOSFET structure very much resembles the architecture of the implant-free MOSFET except that in place of a gate dielectric, a doped cap is utilized to mimic the electrostatics of the III-V MOSFET. The thickness and doping concentration of the cap layer is designed in such a way that the cap layer is just fully depleted. This facilitates ohmic contact formation and accommodates depletion from the pinned semiconductor surface.

III. GROWTH AND FABRICATION

Material growth was undertaken on 2-inch semi-insulating InP substrates using a Veeco Gen III dual chamber molecular beam epitaxy (MBE) system. An overview of the layer compositions of the pre-MOSFET structure is shown Fig. 2. The Beryllium (Be) δ-doped layer, embedded in 2 monolayers of $In_{0.53}Ga_{0.47}As$, was grown with a growth interrupt after the $In_{0.52}Al_{0.48}As$ spacer layer. A thickness of 4nm and a Be doping density of 2.5 x 10^{18} cm^{-3} ensured that the cap was just depleted in line with the pre-MOSFET design requirements. The following growth and structural parameter spacing were investigated as part of the strain engineering study: barrier layer thickness, δ-doping concentration, spacer layer thickness, channel thickness and strain. The channel-to-cap distance was maintained at 30nm for different permutations of the spacer and barrier thicknesses for all as-grown wafers.

Cap layer	4nm $In_{0.53}Ga_{0.47}As$ (Be doped)
Barrier layer	?nm $In_{0.52}Al_{0.48}As$
Doping layer	Be delta-doped
Spacer layer	?nm $In_{0.52}Al_{0.48}As$
Channel	?nm $In_xGa_{1-x}As$
Buffer layer	340nm $In_{0.52}Al_{0.48}As$
Substrate	S.I. InP

Fig. 2. Cross-section of III-V p-channel pre-MOSFET

Van der Pauw (VdP) structures were fabricated on the wafers to elucidate the room temperature hole mobility and carrier concentration parameters. For temperature dependent magneto-transport characterization, wafers were fabricated into Hall-bars using a two level photolithographic process flow. Initially, the ohmic level was defined by Au/Zn/Au contact deposition using a thermal evaporator and rapid thermal annealing at 360°C for 3s. This was followed by the isolation of the active area by wet chemcial etching in 1 H_3PO_4: 1 H_2O_2: 10 H_20 solution for 80s.

IV. EXPERIMENTAL TECHNIQUES

The most widely used technique for material characterization and optimization of transport in heterostructures is the Hall effect measurement due to its ease of use. However, in the presence of mixed (parallel) conduction, this technique fails to selectively determine the carrier densities and mobilities but rather gives misleading results in the form of an effective single carrier density and mobility. Shubnikov-de Haas is another technique that is often employed to selectively deconstruct all conducting layers together with their corresponding transport properties. In order to observe the Shubnikov-de Haas effect, two requirements must be met; $\mu B > 1$ and $kT < \hbar\omega$. This translates to high magnetic induction and liquid helium temperatures. In the case of III-V p-type structures, extremely high fields would be needed due to the expected low mobilities. An alternative is the novel variable-field Hall technique, which would allow for the selective determination of the transport properties of all conducting paths within a

Wafer	Cap doping (cm^{-2})	Barrier thickness (nm)	δ-doping (cm^{-2})	Spacer thickness (nm)	Channel thickness (nm)	Channel strain (%)	300 K Mobility (cm^2/Vs)	300 K Carrier Concentration (cm^{-2})	300K Sheet Resistance (ohms/sq)
C545	2.5×10^{18}	25	4×10^{12}	5	10	0	62	2.4×10^{12}	38796
C550	2.5×10^{18}	25	2.85×10^{12}	5	10	0	67	1.8×10^{12}	47791
C567	2.5×10^{18}	23	2.85×10^{12}	7	10	0	65	1.6×10^{12}	57938
C646	2.5×10^{18}	25	2.85×10^{12}	5	10	1.4	336	1.19×10^{12}	15600
C665	2.5×10^{18}	25	2.85×10^{12}	5	7.5	2.1	433	1.33×10^{12}	10900
C674	2.5×10^{18}	25	4×10^{12}	5	7.5	2.1	427	1.6×10^{12}	9181

Table 1. Summary of growth/material parameters of all wafers grown together with the room temperature hole transport data

structure in the classical low-field limit [8]. In a single conducting channel structure, the sheet density is not expected to be a function of the magnetic induction provided that $\mu B << 1$ and $B < 0.6T$. In contrast, for structures with parallel conducting channels, the sheet density varies with magnetic induction [9]. Therefore, temperature dependent single field and variable field Hall measurements in the magnetic field range 0.0135-0.62T and in the temperature range 10-300K were utilized in this work.

V. Results and Discussion

An overview of the wafers grown as part of the strain engineering study and their corresponding transport properties is illustrated in Table 1. The lattice-matched wafers demonstrated modest, comparable room temperature hole mobilities of 60-70 cm^2/Vs with sheet carrier concentrations in the range 1.6×10^{12}-2.4×10^{12} cm^{-2} depending on the doping level used. The mobility data from these wafers were rather low compared to simulated data of quantum-well like InGaAs channel exhibiting a mobility in the order of 150 cm^2/Vs [10]. A plausible explanation for the low mobilities was the diffusion of Be dopants from the δ-plane into the channel as Be tends to diffuse more readily in aluminum containing alloys. The diffusion length in C545 and C550 was estimated to be 10.5nm based on their substrate growth temperature of 450°C [11]. As such, it is likely that the dopants have diffused past the 5nm spacer into the channel. Dominance of ionized impurity scattering in the channel would account for the low mobilities observed in both wafers. To circumvent this, C567 was grown with a much lower substrate temperature of 400°C and a thicker spacer of 7nm. The Be diffusion length for this wafer was estimated to be 6nm. However, the hole mobility of C567 was comparable to those of C545 and C550.

A few observations relating mobility, carrier density, δ-doping concentration and spacer thickness are expected from single channel conduction [12]: (a) The carrier density and mobility increase with increased δ-doping concentration; (b) The carrier density increases but the mobility decreases with reduced spacer thickness. A comparison of the transport data between C545 and C550, and C550 and C567 shows that the conditions a) and b) are violated, respectively. The transport analysis of these pre-MOSFET wafers is indicative of the presence of two or more parallel conducting channels. Such additional parallel paths can arise from a few scenarios [13]: (1) Multiple subband occupancy of the single 2DHG; (2) Presence of several spatially separated 2DHGs in the InGaAs channel; (3) Un-depleted regions of the delta-doped plane in the pre-MOSFET; (4) Increased scattering in the 2DHG as a result of dopant diffusion.

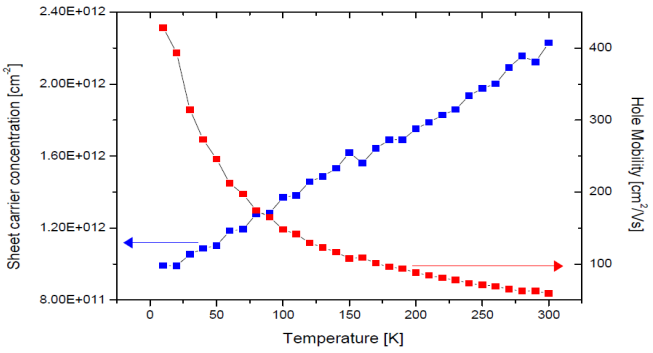

Fig. 3. Single field Hall data of C545 in the range 10-300K

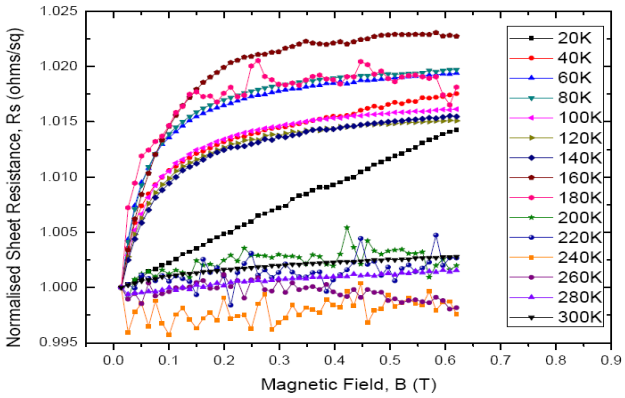

Fig. 4. Normalized sheet resistance as a function of magnetic field and temperature for wafer C545

Temperature dependent single-field Hall measurement data of C545 (see Fig. 3) is indicative of parallel conduction owing to large increase in the carrier concentration in the temperature range 10-300K. In the absence of parallel conduction, the carrier concentration should essentially be unchanged or only change by a slight margin throughout this temperature range [14]. The variable-field Hall data of C545 (see Fig. 4) further illustrates the presence of parallel conduction due to the variation of the sheet resistance with magnetic induction. With decreasing temperature the

presence of parallel conduction becomes more prominent. It is not easy to distinguish which of the previously mentioned effects is the cause. However, a few of the possible effects can be ruled out due to the layer design. Due to single-sided doping, the quantum well will be asymmetric in shape. As such, the presence of more than one spatially separated 2DHG in the channel is unlikely [15]. Additionally, the cap will not contribute to parallel conduction as it has been designed such that it is depleted of carriers. However, in asymmetric quantum wells, the lack of inversion symmetry lifts the spin degeneracy for finite k even at zero magnetic fields, which result in spin-split subbands. This could easily result in parallel conduction as even for sheet densities less than 1 x 10^{12} cm^{-2}, the two lowest spin-split subbands can be occupied [16]. Un-depleted regions of the delta plane as well as dopant diffusion into the channel could just as easily account for the presence of parallel conduction.

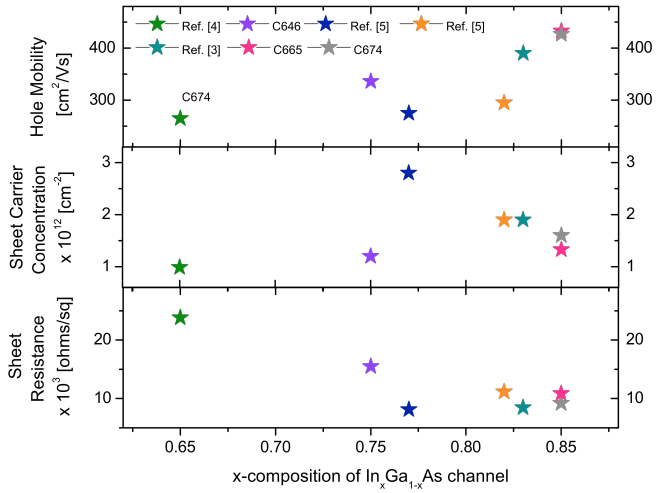

Fig. 5. Benchmarking the hole mobility, carrier concentration and sheet resistance of heterostructures based around an InGaAs channel material

The role of strain was explored with a 75% In-content (1.4% strain) 10nm thick channel, and a 85% In-content (2.1% strain) 7.5nm thick channel (see Table 1.). Of significance, the hole mobility of strained structures show ~5-7X improvement over the lattice-matched structures. Interestingly, the carrier concentrations of the strained structures are considerably lower as compared to the lattice-matched structure; With the exception of 1.4% strain, C646 was identical to C550. The increased valence band offset of C646 compared with C550 should result in more carriers in the channel. On the contrary, the experimental data shows fewer carriers. The most likely explanation for this is parallel conduction in C550 due to un-depleted regions of the delta plane owing to the small valence band offset of 0.2 eV [4], which would account for the poor confinement of holes in the channel. Dopant diffusion can be ruled out as a cause since the hole mobility has drastically increased to 336 cm2/Vs in C646. By increasing the strain to 2.1% and reducing the channel thickness to 7.5nm, to prevent the channel from relaxing, further improvements in mobility and carrier concentrations is realized. The highest ever reported hole mobility of 433 cm2/Vs for an $In_xGa_{1-x}As$ channel has been demonstrated in 2.1% strained structure (see Fig. 5.).

IV. CONCLUSION

The dependence of hole mobility on the bi-axial compressive strain of $In_xGa_{1-x}As$ layers with indium concentrations in the range 53%-85% has been investigated. The lattice-matched structures, regardless of doping level or spacer width, exhibited modest room temperature mobilites in the range 60-70 cm^2/Vs. Temperature-dependent magneto-transport measurement data of C545 was indicative of parallel conduction. The cause of low mobility in the lattice-matched structures was deduced to be arising from un-depleted regions of the delta-plane as opposed to dopant diffusion. Strained structures demonstrated excellent transport properties with a ~5-7X hole mobility improvement over the lattice-matched structures. The hole mobility, 433 cm^2/Vs, of the 2.1% strained structure is the highest room temperature mobility for an $In_xGa_{1-x}As$ material system reported to date. These transport data are highly encouraging for a future pMOS solution based on III-V materials.

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