
http://eprints.gla.ac.uk/4052/

Deposited on: 2 April 2008
LOW NOISE HIGH PERFORMANCE 50nm T-GATE METAMORPHIC HEMT WITH CUT-OFF FREQUENCY $f_T$ of 440GHz for MILLIMETERWAVE IMAGING RECEIVERS APPLICATIONS

K. Elgaid, D. Moran, H. McLelland, M.Holland, I.G. Thayne
Nanoelectronics Research Centre, Department of Electronics and Electrical Engineering
University of Glasgow, Glasgow, G12 8LT, Scotland, United Kingdom
Phone: + 44 141 330 6678, Fax: + 44 141 330 4907 e-mail: kelgaid@elec.gla.ac.uk

Abstract
The 50nm m-HEMT exhibits extremely high $f_T$ of 440GHz, low $F_{min}$ of 0.7dB, associated gain of 13dB at 26GHz with an exceptionally high ld of 200mA/mm and gm of 950ms/mm at low noise biased point.

I. INTRODUCTION
High Electron Mobility transistors for millimeterwave applications using InAlAs/InGaAs on InP substrates have proven their capability in all aspects such as speed, gain, noise, and efficiency [1-3] over GaAs based lattice matched and pseudomorphic HEMTs (LMHEMT and PHEMT) [4-7]. However InP suffers from poor mechanical yield due to the fragility of the substrate, which resulted in the limit of the wafer size available and therefore increasing cost. To utilise the superb performance of the InP devices without compromising wafer fragility, metamorphic high electron mobility transistors (m-HEMTs) on GaAs substrates have become the focus of III-V industry for the applications of millimetre-wave monolithic integrated circuits (MMMICS). The high frequency performance of III-V field effect transistors can be improved in two ways; by reducing the device gate length, or by increasing the velocity of carriers in the device channel.

In III-V GaAs-based field effect devices, the electron velocity can be enhanced by increasing the indium concentration in the device channel. For a GaAs substrate however, a maximum indium concentration of around 25-30% exists using traditional molecular beam epitaxy (MBE) growth approaches due to strain in the device channel arising from the lattice constant mismatch of GaAs and In$_x$Ga$_{1-x}$As for such indium percentages. At higher indium concentrations, the channel relaxes with the introduction of dislocations which dramatically reduce the electron transport properties of the layer, completely at odds with the aim of increasing the channel indium concentration. Moving to higher indium concentrations requires either the use of an InP substrate or developing more complex MBE growth techniques on a GaAs substrate.

In this work we present results based on a 50 nm T-gate of 53% indium concentration in the channel metamorphic high electron mobility transistors (mHEMTs) on GaAs substrate. All the technology required for this device was developed by Glasgow University. These devices showed a superb RF, DC, and High Frequency Noise performance.

II. DEVICE LAYER STRUCTURE AND FABRICATION
Figure 1 shows the double delta doped In$_{0.48}$Al$_{0.52}$As/In$_{0.75}$Ga$_{0.25}$As metamorphic MBE layer structure on a semi insulating GaAs substrate used to realise the high performance 50 nm T-gate length device. Electrical characterisation of the MBE layer showed an electron sheet charge density of $2.31 \times 10^{12}$ cm$^{-2}$ and a mobility of 6470 cm$^2$/V-s at room temperature. The device process flow begins with mesa isolation, using non selective orthophosphoric acid based wet chemical etching. An isolation current of less than 200 pA/mm at 2V was routinely obtained for an etch depth of 65±5 nm (determined by AFM), indicating high quality MBE growth of the mHEMT virtual substrate. Ohmic contact resistances as low as 0.06 $\Omega$-mm were obtained using an annealed Au:Ge:Ni based metallization. Devices were realised using a 1.5 μm source drain separation between which 50 nm gate length T-gates were aligned using a Leica EBPG5-HIR 100 electron beam lithography tool operating at 100 keV and a UVIII/LOR/PMMMA resist stack [8]. A selective succinic acid-based wet chemical etch was used to form the gate recess, prior to the deposition of Ti:Pt: Au gate metallization. Fig. 2 shows a SEM image of the 50 nm T-gate profile after metallisation and lift-off. Finally, 50 $\Omega$ Coplanar waveguide bondpads were defined to enable on-wafer characterisation of the completed devices.

III. RESULTS
DC characterisations were performed by probing the 50nm T-gate device using Cascade MicroTech on wafer RF probes and measuring the electrical traces using Agilent 4155A Semiconductor Parameter Analyser. Figure 3 shows a typical...
DC output characteristic of a 2x50 μm wide device. The DC performance metrics include Ids of more than 800 mA/mm achieved at a drain bias (Vd) of 1.0 V, pinch-off voltage (Vp) of -1.0 V. Figure 4 shows the transfer characteristics of a 2x50 μm wide device, peak extrinsic DC transconductance (gmn) of greater than 1.0 S/mm and higher than 800 ms/mm for gate biases in the range -0.2 V to -0.8 V.

On-wafer S-parameter measurements were performed from 0.04 to 60 GHz, using an Anritsu 360B Vector Network Analyser and on-wafer RF probes from Cascade MicroTech. Calibration was performed using a Cascade Microtech Impedance Standard Substrate (ISS) and the LRRM technique. Fitting of the measured S-parameters to a standard lumped element equivalent circuit model was used to de-embed the coplanar waveguide feed lines. Figure 5 shows the results of this analysis, yielding an fT of 440 GHz and fmax of 400 GHz. To our knowledge, this transistor shows the highest m-HEMT fT and fmax reported to date.

Excellent high frequency noise performance was shown by the device, figure 6 shows the noise parameters as function of frequency up to 26GHz biased at Vds of 0.8 V and Vgs of -0.6 V, Fmm and the associated gain of 0.7 dB and 13 dB respectively were obtained. At these obtained noise performance the device exhibits Ids of 200 mA/mm and gmn of 950 mA/mm.

IV. CONCLUSIONS

In this work we report on low noise high performance 50 nm T-gate In0.53Ga0.47As/In0.53Ga0.47As Metamorphic GaAs HEMTs (m-HEMT) for millimeterwave imaging receivers’ applications. The realised device shows an excellent DC, RF and high frequency noise performance. From the DC characterisation, the device achieved an Ids of 815 mA/mm and (gmn) of 1028 mS/mm. We believe this device exhibits the highest fT and fmax reported up to date for 50 nm m-HEMT of 440 GHz and 400 GHz respectively. Another figure of merit achieved by this device is the extremely low noise parameter and the high associated gain of 0.7 dB and 13 dB respectively at 26 GHz with high Ids of 200 mA/mm.

Fig. 1. Vertical structure of the double delta doped In0.48Al0.52As/In0.53Ga0.47As metamorphic MBE layer on a semi insulating GaAs substrate used in this work.

Fig. 2. 50nm T-gate profile after metallisation and lift-off.

Fig. 3. Output characteristics of a 2 finger 50 μm gate width 50 nm gate length T-gate m-HEMT, showing Ids of 815 mA/mm. Device was measured at Vds up 1.0 V and Vgs from 0V to -1.0 V in -0.1 V steps.

Fig. 4. Transfer characteristics of a 2 finger 50μm gate width with a 50nm gate length T-gate m-HEMT, a transconductance (gmn) of 1000mS/mm was achieved at a bias point of Vds of 1.0 V and Vgs of -0.4 V.
Fig. 5. RF performance of a 2-finger 50 μm gate width with a 50nm gate length T-gate m-HEMT, the device showed a superior $f_T$ of 440 GHz and $f_{max}$ of 400 GHz.

Fig. 6. Noise parameters and the associated gain as function of frequency (GHz) of a 2 finger 50μm gate width with a 50nm gate length T-gate m-HEMT biased at $V_d=0.8V$ and $V_g=-0.6V$.

ACKNOWLEDGEMENTS

This work was supported by the UK Engineering and Physical Sciences Research Council.

REFERENCES


[7] Hyung Sup Yoon; Jin Hee Lee; Jae Yeob Shim; Ju Yeon Hong; Dong Min Kang; Woo Jin Chang; Hae Cheon Kim; Kyoung Ik Cho, “0.15μm gate length InAlAs/InNWAs power metamorphic HEMT on GaAs substrate with extremely low noise characteristics,” International Conference on Indium Phosphide and Related Materials, PP. 114 – 117, May 2003.