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Enhancement-Mode GaAs MOSFETs With an $In_{0.3}Ga_{0.7}As$ Channel, a Mobility of Over 5000 $cm^2/V \cdot s$, and Transconductance of Over 475 $\mu S/\mu m$

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***Abstract*—We present metal-gate high-κ-dielectric enhancement-mode (e-mode) III–V MOSFETs with the highest reported effective mobility and transconductance to date. The devices employ a GaGdO high-κ ($\kappa = 20$) gate stack, a Pt gate, and a δ-doped InGaAs/AlGaAs/GaAs heterostructure. Typical 1-μm gate length device figures of merit are given as follows: saturation drive current, $I_{d,\mathrm{sat}} = 407\ \mu A/\mu m$; threshold voltage, $V_t = +0.26$ V; maximum extrinsic transconductance, $g_m = 477\ \mu S/\mu m$ (the highest reported to date for a III–V MOSFET); gate leakage current, $I_g = 30$ pA; subthreshold swing, $S = 102$ mV/dec; on resistance, $R_{\mathrm{on}} = 1920\ \Omega \cdot \mu m$; $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio $= 6.3 \times 10^4$; and output conductance, $g_d = 11$ mS/mm. A peak electron mobility of 5230 $cm^2/V \cdot s$ was extracted from low-drain-bias measurements of 20 μm long-channel devices, which, to the authors' best knowledge, is the highest mobility extracted from any e-mode MOSFET. These transport and device data are highly encouraging for future high-performance n-channel complementary metal–oxide–semiconductor solutions based on III–V MOSFETs.**

***Index Terms*—Enhancement mode (e-mode), GaGdO, high κ, III–V MOSFET.**

I. INTRODUCTION

FUTURE SCALING of CMOS in accordance with Moore's law and to meet the demands of the International Technology Roadmap for Semiconductors will require various nontraditional solutions such as high-κ dielectrics, metal gates, and high-mobility channels [1]. Interest has recently focused on germanium and III–V-based material systems as likely p- and n-channel ultimate scaling solutions because of their superior transport properties. It is expected that the corresponding high intrinsic hole and electron mobilities and low effective masses should translate to higher drive current and lower access resistance [2]–[4]. III–V MOSFET technology may also find future use in radio frequency applications at low voltage and for high efficiency, i.e., in wireless and mobile products. In this letter, we report record performance and mobility from implant-free GaAs MOSFETs [5] that feature a high-κ dielectric/metal gate stack and an $In_{0.3}Ga_{0.7}As$ channel. In contrast with previously reported GaAs MOSFET electron mobility measurements made by noncontact methods of ungated structures [3], the data reported here represent the highest mobility extracted from GaAs MOSFET I_d–V_{ds} characteristics. Previously, enhancement-mode (e-mode) GaAs MOSFETs with performance that was significantly constrained by relatively high source and drain resistance were reported [6], [7]. In this letter, we have utilized a wet etch process to remove the gate oxide prior to ohmic contact metallization rather than an ion mill technique, which delivers a reduction in contact resistance by a factor of five to ten. This is due to both the selective nature of the wet etch removal of the oxide layer, which stops on the underlying semiconductor surface and the lack of any damage introduced by the physical ion milling process.

II. EXPERIMENT

The epitaxial layer structure used to fabricate the transistors comprised the following layers that were sequentially grown on a semi-insulating (100) GaAs substrate: a 200-nm GaAs buffer; a 65-nm $Al_{0.2}Ga_{0.8}As$ buffer; a 5-nm $Al_{0.2}Ga_{0.8}As$/GaAs spacer; a 10-nm $In_{0.3}Ga_{0.7}As$ channel; a 3-nm GaAs spacer; a 2-nm $Al_{0.45}Ga_{0.55}As$ barrier layer; a 0.5-nm GaAs layer; and a 10-nm Ga_2O_3/GaGdO (GGO) dielectric stack. Silicon δ-doping layers were placed above and below the channel, with doping densities of 1×10^{12} and 3×10^{12} cm^{-2}, respectively. A two-level wrap-around gate design (where the gate encircles the drain) was used to simplify the device process flow, removing the need for isolation. First, the Pt/Au gate was patterned by direct-write electron beam lithography (EBL) and liftoff. Subsequently, ohmic contacts, with a source–drain separation of 2.7 μm, were defined, again, by EBL. The GGO dielectric stack was removed by selective HCl wet etching (1:100 HCl:H_2O, 30 s) prior to deposition of Ni/Ge/Au ohmic

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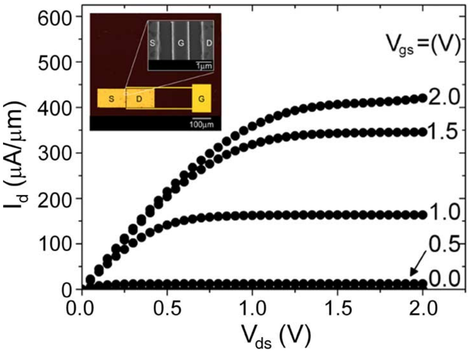

Fig. 1. I_d–V_{ds} characteristics of a typical 1-μm gate length GaAs MOSFET with an $\mathrm{In}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ channel. Inset: optical and SEM micrographs of a completed device.

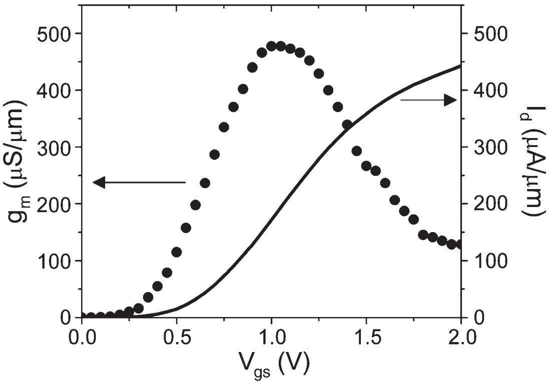

Fig. 2. I_d–V_{gs} and g_m–V_{gs} characteristics of a typical 1-μm gate length GaAs MOSFET with an $\mathrm{In}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ channel ($V_{\mathrm{ds}} = 2$ V).

contacts, which underwent rapid thermal annealing at 430 °C for 60 s. Optical and scanning electron microscope micrographs of a completed device are shown in the inset of Fig. 1. Transmission line measurements of process control structures, alongside the MOSFET devices, gave a contact resistance of 410 $\Omega\cdot\mu$m and a sheet resistance of 449 Ω/sq.

III. Results and Discussion

Fig. 1 shows the I_d–V_{ds} characteristics of a typical 1-μm device, where the gate voltage was varied from 0 to 2.0 V in steps of 0.5 V. Fig. 2 plots the I_d–V_{gs} and g_m–V_{gs} curves at a drain bias of 2 V. The device figures of merit were given as follows (measurement conditions in parentheses): $V_t = 0.26$ V ($V_{\mathrm{ds}} = 2$ V and $I_d = 1$ μA/μm); $I_{d,\mathrm{sat}} = 407$ μA/μm ($V_{\mathrm{gs}} = 2$ V and $V_{\mathrm{ds}} = 1.75$ V); maximum extrinsic $g_m = 477$ μS/μm ($V_g = 1.1$ V and $V_d = 2$ V); $g_d = 11$ μS/μm ($V_{\mathrm{gs}} = 1.5$ V and $V_{\mathrm{ds}} = 1.5$ V); $R_{\mathrm{on}} = 1920$ $\Omega\cdot\mu$m ($V_{\mathrm{gs}} = 2$ V and $V_{\mathrm{ds}} = 0.05$ V); and maximum $I_g = 30$ pA (maximum across full operating voltage range). Fig. 3 shows the semilogarithmic plot of the I_d–V_{gs} characteristics ($V_{\mathrm{ds}} =$ 0.1 and 2 V), with I_g ($V_{\mathrm{ds}} = 0.1$ and 2 V) in the insert. Drain-induced barrier lowering is effectively 0 mV/V, indicating a well-scaled layer structure for this gate length. The average S is 102 mV/dec ($V_{\mathrm{gs}} = -0.2$ to 0.2 V and $V_d = 2$ V), and the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio is 6.3×10^4 ($I_{\mathrm{off}}, V_{\mathrm{gs}} = 0$ V and $V_d =$ 2 V; $I_{\mathrm{on}}, V_{\mathrm{gs}} = 2$ V and $V_{\mathrm{ds}} = 2$ V). The five to ten times reduction in contact resistance from previously published devices [6], [7] has resulted in a factor of two to six times increase in the maximum extrinsic g_m. The excellent subthreshold performance and high g_m indicate a minimal interface trap density over the complete gate voltage operation range. Details about the device operation of implant-free flatband MOSFETs can be found in [5].

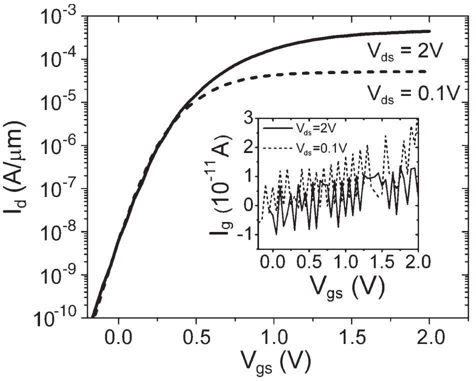

Fig. 3. Logarithm of I_d–V_{gs}, with I_g–V_{gs} in the inset, of a typical 1-μm gate length GaAs MOSFET with an $\mathrm{In}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ channel. Dashed lines: $V_{\mathrm{ds}} = 0.1$ V. Solid lines: $V_{\mathrm{ds}} = 2$ V.

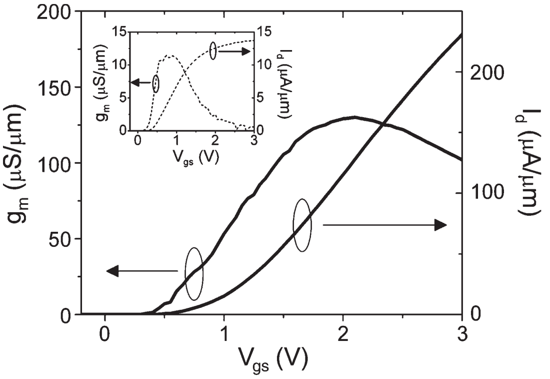

Fig. 4. I_d–V_{gs} and g_m–V_{gs} characteristics of a typical 20-μm gate length GaAs MOSFET with an $\mathrm{In}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ channel. Dashed lines (inset): $V_{\mathrm{ds}} = 0.1$ V. Solid lines: $V_{\mathrm{ds}} = 3$ V.

A method that is analogous to the split *CV* method [8] was used to extract the effective carrier mobility as a function of carrier concentration from the I_d–V_{gs} characteristics of a 20-μm gate length device at $V_{\mathrm{ds}} = 0.1$ V. Typical I_d–V_{gs} and g_m–V_{gs} ($V_{\mathrm{ds}} = 0.1$ and 3 V) plots of an $L_g = 20$ μm device are given in Fig. 4. Figures of merit are $V_t = 0.45$ V ($V_{\mathrm{ds}} = 0.1$ V and $I_d =$ 1 μA/μm), $I_{d,\mathrm{sat}} = 230$ μA/μm ($V_{\mathrm{gs}} = 3$ V and $V_{\mathrm{ds}} = 3$ V), maximum extrinsic $g_m = 130$ μS/μm ($V_{\mathrm{gs}} = 2.1$ V and $V_d =$ 3 V), $R_{\mathrm{on}} = 7120$ $\Omega\cdot\mu$m ($V_{\mathrm{gs}} = 3$ V and $V_{\mathrm{ds}} = 0.1$ V), and $I_g = 200$ pA (maximum across full operating voltage range).

The wrap-around gate design precludes the split *CV* measurement of transistors, due to the parasitic contribution from the large probe pads. Instead, $C(V_g)$ at 1 MHz was measured on annular *CV* structures, fabricated adjacent to the 20-μm gate length transistors. The channel carrier concentration n_s was obtained by integration over $C(V_{\mathrm{gs}})$. The resulting mobility/carrier concentration plot (Fig. 5) can be split into two

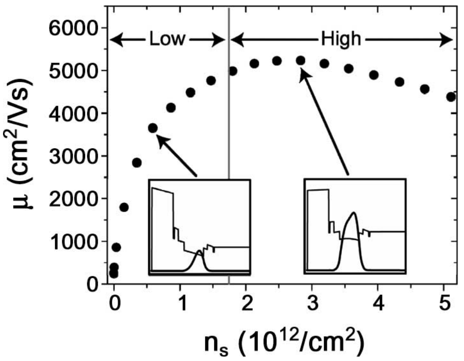

Fig. 5. Mobility, with band diagrams in the inset, of a typical 20-μm gate length GaAs MOSFET with an $\mathrm{In}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ channel.

regions – low and high carrier concentrations. The insets of Fig. 5 are the conduction band energy, E_c, and the electron distribution, n, diagrams that are indicative of the free carrier positions within the layer structure for each region. In the low-carrier-concentration region, the channel charge is well confined at the back of the $\mathrm{In}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ layer. In this situation, the electron mobility is dominated by remote Coulomb scattering from the underlying δ-doping layer. The mobility in this region increases with charge density due to enhanced screening. At higher concentrations, the charge distribution moves from the rear of the channel toward the upper interface, with an increasing applied gate voltage (and, thus, carrier concentration). The mobility peaks $(5230\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s};\ n_s = 2.8\times 10^{12}\ \mathrm{cm}^{-2})$ at approximately flatband (defined as zero field in the barrier layer), which corresponds to the charge centroid being located near the center of the channel and, hence, having the minimum contribution from interface roughness scattering from either the front or back interfaces. These data show good correlation to contactless Hall effect data on similar layer structures [3]. At a higher gate voltage, channel confinement is lost, and carriers spill into the low-mobility GaAs spacer and $\mathrm{Al}_{0.45}\mathrm{Ga}_{0.55}\mathrm{As}$ barrier layers above the channel. This mobility extraction method neglects interface traps, which will become populated when upper confinement is lost. Hence, Hall bar measurements are required to determine the mobility/carrier concentration relationship at higher charge density.

IV. SUMMARY

Recent developments in improving contact resistance have enabled the demonstration of e-mode GaAs MOSFETs with an $\mathrm{In}_{0.3}\mathrm{Ga}_{0.7}\mathrm{As}$ channel and extrinsic transconductance of over 475 $\mu\mathrm{S}/\mu\mathrm{m}$—the highest value reported to date. These 1-μm gate length devices have excellent subthreshold performance (102 mV/dec), positive threshold voltage (0.26 V), and large $I_{d,\mathrm{sat}}$ (407 $\mu\mathrm{A}/\mu\mathrm{m}$). A peak effective mobility of 5230 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ $(n_s = 2.8\times 10^{12}\ \mathrm{cm}^{-2})$ was extracted from long-channel devices. This is the highest value reported for any MOSFET device and indicates the potential of this technology for future n-channel CMOS solutions.

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