Design of a Single-Chip pH Sensor Using a Conventional 0.6-μm CMOS Process

Paul A. Hammond, Danish Ali, and David R. S. Cumming

***Abstract*—A pH sensor fabricated on a single chip by an unmodified, commercial 0.6-μm CMOS process is presented. The sensor comprises a circuit for making differential measurements between an ion-sensitive field-effect transistor (ISFET) and a reference FET (REFET). The ISFET has a floating-gate structure and uses the silicon nitride passivation layer as a pH-sensitive insulator. As fabricated, it has a large threshold voltage that is postulated to be caused by a trapped charge on the floating gate. Ultraviolet radiation and bulk-substrate biasing is used to permanently modify the threshold voltage so that the ISFET can be used in a battery-operated circuit. A novel post-processing method using a single layer of photoresist is used to define the sensing areas and to provide robust encapsulation for the chip. The complete circuit, operating from a single 3-V supply, provides an output voltage proportional to pH and can be powered down when not required.**

***Index Terms*—CMOS analog circuit, encapsulation, ion-sensitive field-effect transistor (ISFET), pH, system-on-chip (SoC).**

I. Introduction

THE pH sensor is of great importance in a wide range of industries. A miniature pH sensor is of particular interest in the field of medical diagnostics for use on catheter tips or in implantable devices. Traditional pH sensors use a glass bulb electrode that is both fragile and bulky. Solid-state pH sensors based on ion-sensitive field-effect transistors (ISFETs) have been developed since the 1970s as a miniature, robust alternative. However, they invariably require the use of bulky, external circuitry in order to take readings.

In recent years, system-on-chip (SoC) technology has been increasingly used to create complex, integrated systems on a single CMOS chip, for example, mobile phones and set-top boxes. Combining sensors with more conventional SoC components will lead to a fully integrated diagnostic system, which can take readings and provide analysis on a single chip. The pH sensor, and ISFET-based sensors, in general, are good candidates for integration with the CMOS process, as both are based on FETs.

Initial attempts at integration introduced several ISFET-specific steps to a create a custom CMOS process [1]–[3]. However, it is highly desirable to use a commercial CMOS process, to take advantage of the well-established design environment and resources. ISFETs have been fabricated by an unmodified commercial process but were found to have large and varied threshold voltages [4].

In this paper, we show how the threshold voltage of the CMOS ISFET can be controlled by using ultraviolet radiation. A differential circuit, which uses the ISFET, a reference FET (REFET), and a quasireference electrode, is presented. The complete circuit is implemented on a single chip using standard library components and operates from a 3-V supply. A novel post-processing method using a single layer of photoresist to define the sensing area and encapsulate the device is also demonstrated. The pH sensor circuit forms an intellectual property (IP) block that can be used as part of a more sophisticated sensor system-on-chip.

II. CMOS Compatible ISFET

A standard metal-oxide-semiconductor FET (MOSFET) can be converted into an ISFET by removing the gate metal and placing the gate oxide in direct contact with the test solution. Hydrogen ions in the solution are specifically adsorbed onto the oxide surface, causing a build up of charge that varies with the pH of the solution. The charged surface creates an electrical double-layer capacitance at the surface-solution interface across which the surface potential appears. This potential affects the electric field in the gate oxide and so changes the threshold voltage (V_T) of the ISFET. Since its introduction in 1970 [5], the ISFET has received a lot of attention, mostly focussed on improving the performance by using other insulators in place of the gate oxide. Studies have shown that Si_3N_4, Al_2O_3 and Ta_2O_5 all have good linearity, sensitivity, and stability.

In a CMOS process, a polysilicon gate electrode is used to define the self-aligned source and drain regions. Multiple metal layers—usually aluminum—are used to connect devices and circuits together. A top passivation layer—usually silicon nitride or silicon oxynitride—is used to protect the chip from the environment. Recently, an ISFET has been designed that uses a floating gate electrode formed from the CMOS metal layers to connect the nitride passivation layer to the gate oxide layer [4]. This is an important advantage, as it allows ISFETs to be created by a commercial CMOS foundry with no additional process steps. An equivalent circuit for the CMOS ISFET comprises the underlying MOSFET in series with capacitors to model the impedance of the passivation layer (C_{PASS}) and the electrical double layer (C_{DL}). There is also a voltage source that represents the electrochemical potential difference U_{REF} between reference electrode and solution (Fig. 1).

We have fabricated ISFETs in a three-metal, 0.6-μm process from Austria Micro Systems. In this process, the passivation layer consists of 0.4 μm of silicon nitride on top of 0.6 μm of silicon oxynitride. The source and drain regions were interleaved

Manuscript received October 31, 2002; revised September 8, 2003. This work was supported by grants from the Engineering and Physical Sciences Research Council, the Scottish Higher Education Funding Council, and Philips Research Laboratories, U.K. The associate editor coordinating the review of this paper was Prof. P. M. Sarro.

P. A. Hammond and D. R. S. Cumming are with the Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow, G12 8LT, U.K. (e-mail: p.hammond@elec.gla.ac.uk).

D. Ali is with Philips Research Laboratories, Redhill, RH1 5HA, U.K.

Digital Object Identifier 10.1109/JSEN.2004.836849

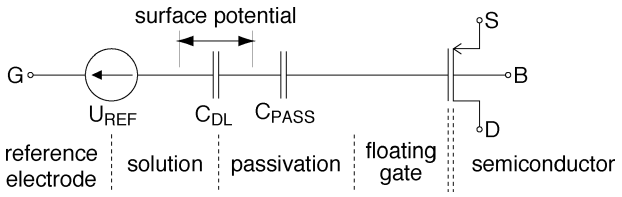

Fig. 1. CMOS ISFET equivalent circuit.

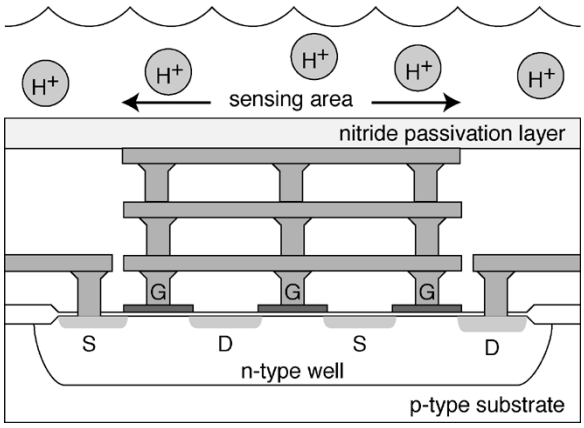

Fig. 2. Schematic cross section through a CMOS ISFET.

(Fig. 2) to reduce the area occupied by the ISFET, which has width/length dimensions of 1000/4 μm. A p-type ISFET was chosen since, with a p-type substrate, it can be contained in a separate n-type well to provide isolation from the rest of the chip. At low frequencies, p-type ISFETs have also been shown to have better noise performance than their n-type counterparts [6].

III. Differential Sensing

An ideal reference electrode for use as the ISFET gate terminal should provide

1) an electrical contact to the solution from which to define the solution potential;
2) an electrode/solution potential difference (U_{REF}) that does not vary with solution composition.

The conventional silver chloride or calomel electrode provides both of these functions by maintaining an electrochemical equilibrium with the solution. Such an electrode requires compartments filled with a reference solution and separated by a permeable membrane. Although these can been fabricated with IC-compatible techniques, using a porous silicon plug, they have only short lifetimes [7].

A. Reference FET

An alternative technique is to make differential measurements between an ISFET and an *ion-insensitive* FET or reference FET (REFET). A metal electrode provides the electrical contact to the solution and defines its potential. However, the electrode/solution potential difference will vary with solution composition, hence the metal electrode is called a *quasi*-reference electrode (qRE). Provided that the qRE is used to bias both ISFET and REFET in a differential measurement circuit, variations in U_{REF} are rejected as a common-mode signal.

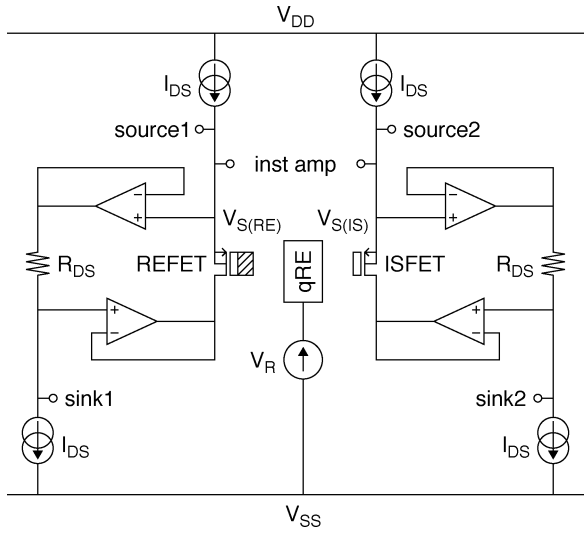

Fig. 3. Differential circuit diagram.

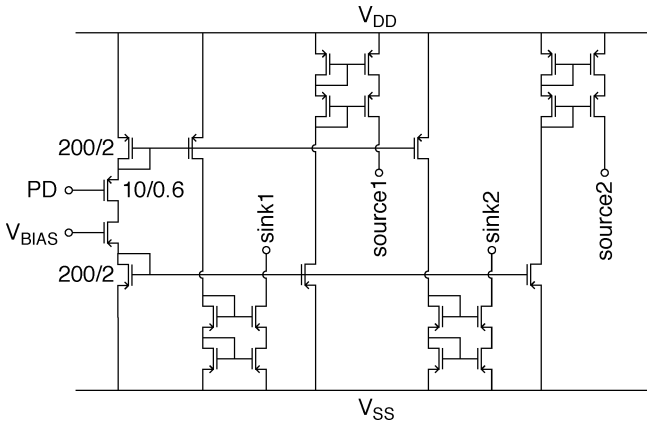

Fig. 4. Cascode current source and sink.

The ideal REFET for a pH sensor would be completely insensitive to hydrogen ions but identical to the ISFET in terms of transconductance, thermal response, etc. This can be achieved by coating an ISFET with a polymer membrane to prevent the hydrogen ions from reaching the insulator surface. The polymer used must be ion unblocking to preserve the electrical characteristics of the underlying ISFET [8]. That is, the polymer must allow conduction by another ion species to prevent a potential drop forming across the membrane. It has been demonstrated that for a particular PVC membrane composition, the REFET sensitivity to H^+, Na^+, and K^+ ions in the solution is very low [9].

B. Differential Circuit Design

For an ISFET in the saturation region, the drain current is given by

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{\mathrm{RS}} - V_T)^2(1 + \lambda V_{\mathrm{DS}})$$

where k' is a process-dependant constant, λ is the channel length modulation factor, and W and L are the width and length of the device. In order to be able to measure the threshold voltage of the ISFET—and hence the solution pH—it is necessary to bias it at constant drain current and constant drain-source voltage (V_{DS}). This uniquely specifies the value of ($V_{\mathrm{RS}} - V_T$) and so,

as V_T varies, the reference-source voltage $(V_{\rm RS})$ must adjust by an equal amount to compensate.

A circuit to maintain both constant I_D and constant $V_{\rm DS}$ has been proposed in [10]. We have devised a double version of this circuit, similar to that used in [11], that biases both ISFET and REFET with respect to a common qRE (Fig. 3). Considering just the right-hand half of the circuit, the ISFET source and drain terminals can adopt any voltage between the dropout voltages of the current source and sink. The top current source forces a constant current through the ISFET, while the bottom current sink forces an identical current through the fixed resistor $R_{\rm DS}$. Current source and sink are mirrored to ensure that the two currents are the same. The constant voltage dropped across $R_{\rm DS}$ is replicated across the ISFET by the pair of unity-gain operational amplifiers. Since V_R is fixed by the voltage source, as V_T varies, so too will $V_{S({\rm IS})}$ to maintain a constant $(V_{\rm RS}-V_T)_{({\rm IS})}$. $V_{D({\rm IS})}$ will also track $V_{S({\rm IS})}$, maintaining constant $V_{DS({\rm IS})}$.

The REFET is biased using an identical circuit so that both FET operating points are identical, eliminating a source of differential signal error. For an ideal REFET, V_T does not vary and so $V_{S({\rm RE})}$ is constant; the difference $(V_{S({\rm IS})}-V_{S({\rm RE})})$ forms the pH-dependant signal. This is input to an instrumentation amplifier to produce a full-scale signal swing and provide buffering for driving off-chip circuits.

The current sources and sinks were implemented using a cascode current mirror circuit [10]—rather than single-transistor mirrors—to provide a constant current over a wide range of voltages (Fig. 4). Both the NMOS and PMOS transistors (with the exception of the transistor connected to terminal PD) have identical dimensions of 200/2 μm to simplify the layout and improve device matching. The circuit can source and sink currents with less than 1% error at voltages greater than 0.7 V from the supply rails. For a 3-V supply, this leaves the ISFET and REFET with a 1.6-V range to operate in, which is more than sufficient. The current is set by an external voltage $V_{\rm BIAS}$ and the circuit can be powered down using the terminal PD. The qRE was implemented as an exposed aluminum bondpad, designed to be coated with gold or another stable metal by plating or evaporation. The other components required for the differential circuit and instrumentation amplifier were standard library components, provided as part of a design kit by the foundry.

IV. Fabrication

The pH sensor circuit and the ISFET characterization devices were fabricated on the same chip. The chips were supplied as unpackaged die, approximately 4 $\times$ 4 mm in size. Fig. 5 shows a scanning electron microscope (SEM) image of the cross section on an ISFET obtained by cleaving the chip. The passivation layer and the three metal layers are clearly visible. Less obvious is the polysilicon layer, which forms the gates of the underlying MOSFET. The vias that connect MET1 to the source and drain regions and the voids left by the vias between MET3 and MET2 can also be seen. Only the connections between MET2 and the POLY gates are invisible as they do not lie in the cleavage plane.

Before the chips could be tested, some post processing was required to create the REFET and to provide a waterproof connection to a PCB. The membrane used to create the REFET is formed by solvent casting and so a well is required to constrain the membrane. These two requirements can be satisfied by a single process that uses a thick layer of SU-8[1] photoresist. Previous studies using photocurable epoxies have either applied them to the whole wafer by spin coating [12] or to wire-bonded chips by hand [13]. By recessing the chip into the PCB, we are able to use spin coating to apply a uniform layer of encapsulating material after bonding.

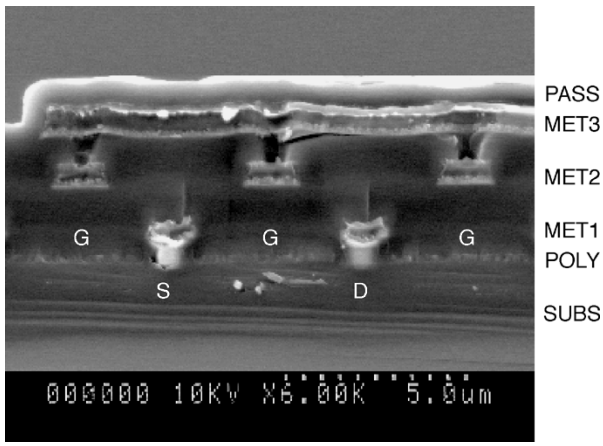

Fig. 5. SEM image of ISFET cross section.

First, a square recess was milled into the PCB so that when inserted, the chip lies flush with the surface of the PCB. The bondpads on the chip were then connected to the PCB tracks using 20-μm wire in a wedge bonder (Fig. 6, step 1). A thick layer of SU-8 (approximately 150 μm) was spun over the chip and PCB. The SU-8 was exposed to ultraviolet light on a mask aligner using an acetate mask printed with a high-resolution laser printer (Fig. 6, step 2). The mask was designed to prevent exposure above the ISFET, REFET, qRE, and PCB connector terminals. After development, the PCB was cleaned in an oxygen plasma to ensure all traces of resist and solvent were removed from the chip surface. Finally, a surface-mount connector was soldered to the PCB and the membrane was deposited in the well above the REFET using a glass capillary (Fig. 6, step 3). The PVC membrane composition and solvent-casting process used was the same as in [9].

V. Results and Discussion

The ISFET characteristics were measured using a Keithley 4200 Semiconductor Characterization System to apply bias voltages and currents. The chip, mounted on the PCB, was placed in a beaker of solution inside a Faraday cage to minimize the effects of interference and varying light levels. The solutions used were 0.15 M NaCl with 0.05-M phosphate or acetate buffer and the reference electrode was a conventional Ag/AgCl electrode.

A. Threshold Modification

The threshold voltage of n-type CMOS ISFETs has been found to vary from -7 to $+6$ V, depending on the device geometry [4]. The p-type ISFET fabricated in this study has a threshold voltage of approximately -5 V, making it incompatible with operation from a 3-V supply. Hence, it is necessary to be able to modify V_T after fabrication.

[1]Epoxy based negative photoresist from MicroChem Corp.

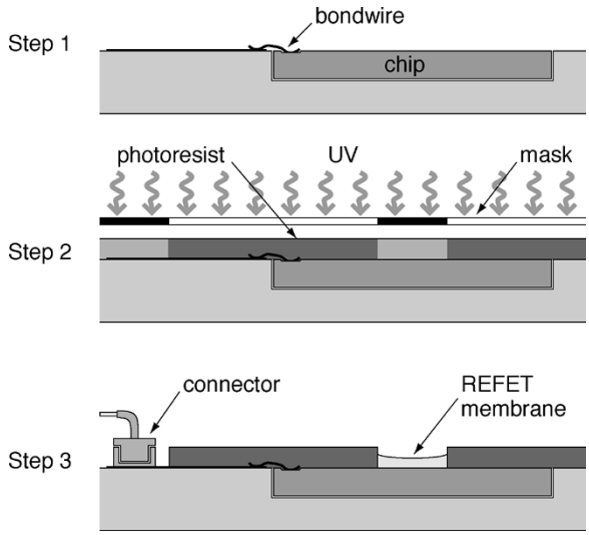

Fig. 6. Chip post processing using a single layer of photoresist.

A CMOS ISFET has a similar structure to an electrically programmable read-only memory (EPROM) device, which uses charge trapped on the floating gate of a transistor to store a 1 or a 0 in memory. These chips have a quartz window that allows them to be erased by exposure to ultraviolet (UV) radiation. The UV light excites the electrons on the gate to such an extent that they can overcome the oxide energy barrier and discharge the gate. UV programming of floating-gate transistors has been demonstrated using polysilicon-polysilicon capacitors in another CMOS process from the same foundry, with a dielectric oxide that is 1.6 times as thick as the gate oxide being used here [14]. Accordingly, the ISFET was exposed to UV light using an EPROM eraser to investigate the effect that this had on the threshold voltage.

Such long exposure times were required to produce a sufficient change in V_T that the photoresist used to encapsulate the chip was damaged. In order to measure the ISFET characteristics before the chip is packaged, a liquid probe was devised to act as a miniature quasireference electrode. A customized probe arm was used to position a glass capillary just above the ISFET on the chip using a micropositioner on a probe station. Silicone rubber tubing connected the capillary to a syringe allowing 0.1-M NaCl solution to be forced into contact with the chip surface without it touching the bondwires. A silver wire inside the capillary provided the electrical connection to the reference electrode. The other connections to the ISFET were made using bondwires.

The ISFET was placed in the EPROM eraser for a period of time after which its characteristics were measured—in darkness—using the liquid probe (Fig. 7). The effect of UV exposure on the threshold voltage is clearly seen in the I_D versus V_R curves of Fig. 8. After 1 h, V_T had increased to approximately -2 V and continued to increase toward -1 V over the next 2 h. However, the rate of change of V_T is much reduced as it approaches its equilibrium value. If a further increase in V_T is required, this can be achieved by applying a positive voltage to the ISFET bulk with respect to the substrate—and hence with respect to the floating gate—during exposure. The final curve in Fig. 8 shows the effect of an additional one hour exposure during which a bulk-substrate bias of $+5$ V was applied.

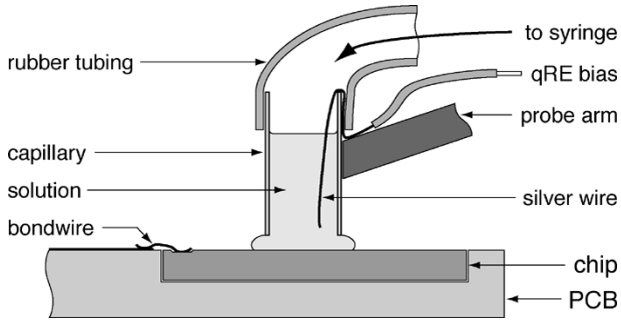

Fig. 7. Liquid probe used as ISFET gate terminal.

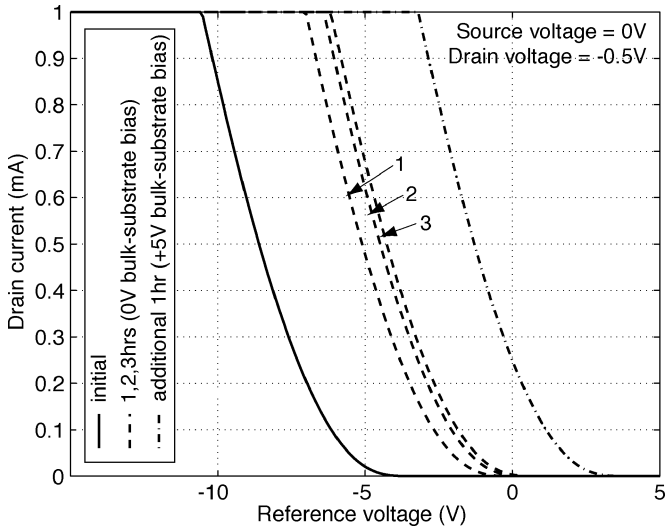

Fig. 8. Effect of UV exposure on threshold voltage.

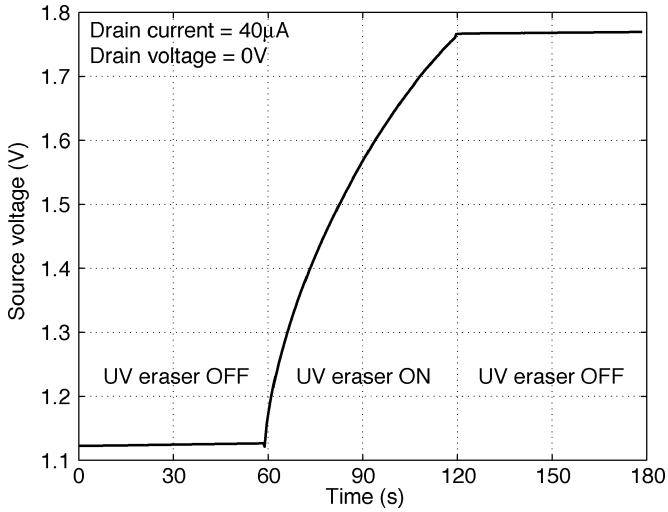

Fig. 9. Modification of threshold voltage measured inside UV eraser.

The UV exposure has a permanent effect on the threshold voltage, which can be seen by taking readings inside the EPROM eraser. In this experiment the voltage required to maintain a constant drain current was applied to the source of the ISFET. While the UV eraser is on, V_T increases and the source voltage rises to maintain I_D (Fig. 9). When the UV eraser is switched off, the source voltage remains constant at

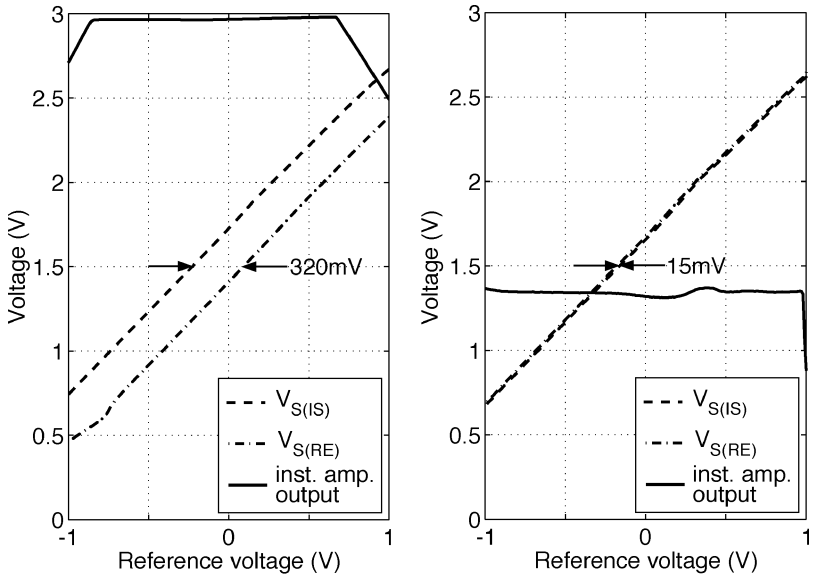

Fig. 10. Effect of UV exposure on ISFET/REFET threshold voltage mismatch, measured prior to the application of the REFET membrane; (a) 3-h exposure and (b) 17-h exposure.

the new higher level indicating that V_T has been permanently altered. More long-term evidence for this comes from the drift curve of Fig. 11, which shows no sign of the threshold voltage relaxing back toward its original value.

The UV radiation modifies the threshold voltage either by removing fixed charge from the passivation layer or by removing trapped charge from the floating electrode. Fixed charge was concluded to be the cause of the wide range of threshold voltages observed in [4]. UV radiation is known to annihilate fixed charge in silicon nitride films by affecting the dangling-bond centers [15]. However, the effect that the bulk-substrate bias has during exposure suggests that charge removal from the floating electrode is the more likely explanation. Applying a bias changes the conduction band level in the ISFET bulk. The UV radiation excites the electrons to overcome the energy barrier of the gate oxide so that the population on the floating electrode can achieve an equilibrium with those in the bulk. When the bias and the UV illumination are removed the band levels in the bulk are restored, but the electrons can no longer cross the gate oxide, and so the floating electrode remains in the new state, modifying the threshold voltage. A different design of ISFET with a continuous top metal layer was not affected by the UV radiation. This suggests that the metal acts as a shield, preventing the UV from reaching the polysilicon and causing the electrons to tunnel through the gate oxide. In contrast, the intermediate-gate ISFETs fabricated in [16] have leaky sensing insulators and can quickly discharge the gate electrode to the solution.

The fact that V_T reaches an equilibrium value after a long UV exposure is particularly important for the differential circuit, which relies on ISFET and REFET having well-matched threshold voltages. To investigate any mismatch, the differential circuit (Fig. 3) was measured prior to the application of the polymer layer to the REFET. Fig. 10 shows the values of $V_{S(\mathrm{IS})}$ and $V_{S(\mathrm{RE})}$ as the voltage on the liquid probe quasireference electrode is varied. After 3 h of UV exposure, there is still a mismatch of 320 mV between ISFET and REFET V_T. The differential gain of the circuit causes the instrumentation amplifier output to saturate at the supply voltage (+3 V). However, after 17 h of exposure, the V_T mismatch is reduced to 15 mV, causing only a small offset to the desired mid-rail circuit output of 1.5 V.

B. ISFET Sensitivity and Drift

By extracting the threshold voltage from I_D versus V_R curves while changing the solution pH, the ISFET sensitivity was measured to be approximately 43 mV/pH. This compares well with the value of 47 mV/pH for the commercial CMOS ISFETs in [4], but is significantly lower than the near-Nernstian value of 58 mV/pH for the ISFETs in a specialized CMOS process [2]. Silicon nitride as an ISFET-sensing layer is usually obtained by low-pressure chemical vapor deposition (CVD), whereas plasma-enhanced CVD is used to create the CMOS passivation layer. The different deposition conditions are a likely cause of the observed difference in sensitivity.

The CMOS ISFET also exhibits considerable threshold voltage drift, as shown in Fig. 11. Since I_D and V_R are held constant and the ISFET is in saturation, the measured change in V_S is virtually identical to the change in V_T. The initial drift rate was 120 mV/h, and, after 10 h, it had fallen to 3.5 mV/h, which is equivalent to a change in reading of 0.08 pH units/h. The drift is thought to be caused by the slow conversion of the Si_3N_4 surface to a hydrated SiO_2 or oxynitride layer during contact with the solution. A physical model for this process—based on a mechanism known as dispersive transport—has been developed and used to compensate for the drift [17], [18]. A system-on-chip approach is well suited to the implementation of a real-time compensation algorithm such as this.

During the drift experiments, the leakage current from the reference electrode remained less than 1 nA, demonstrating that the photoresist encapsulation remained intact. A more robust

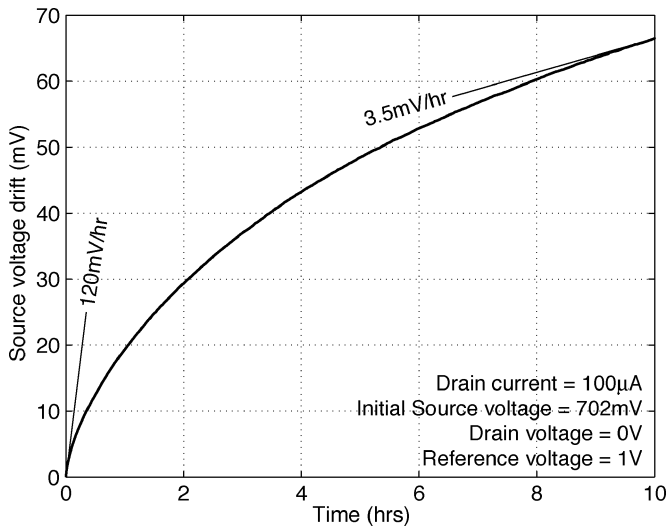

Fig. 11. Long-term ISFET threshold voltage drift.

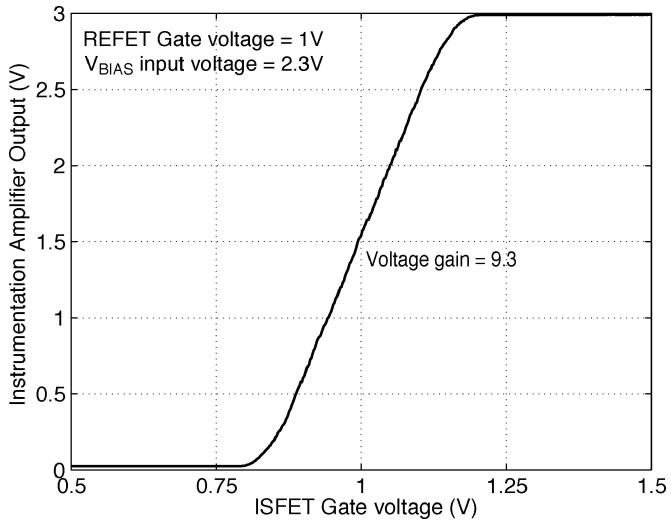

Fig. 12. Emulated differential circuit response.

encapsulation could be achieved by using a polyimide layer in place of the SU-8 photoresist, but only if the chip can withstand the high curing temperature.

C. Circuit Performance

When covered with the PVC-based membrane, the REFET showed a much-reduced pH sensitivity. However, the addition of the membrane produced a V_T mismatch between ISFET and REFET that would have caused the circuit output to saturate. Further work is required to find a suitable REFET membrane.

In order to emulate the effect of a differential pH response on the circuit as a whole, direct probe connections were made to the floating gates of ISFET and REFET by laser ablation of the passivation layer. The REFET gate was held fixed at $+1$ V while the ISFET gate voltage was varied; the circuit output response is shown in Fig. 12. The voltage gain in the working region is 9.3, which gives a sensitivity of 400 mV/pH and an input range of 6 pH units, assuming maximum differential sensitivity. The complete circuit consumes 2.1 mW while operating, but consumes less than 0.1 μW when it is powered down.

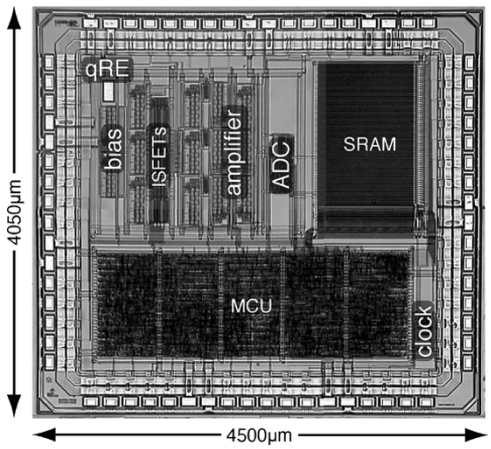

Fig. 13. Integrated system-on-chip pH sensor.

VI. Conclusion

The design of a single-chip CMOS pH sensor based on a floating-gate ISFET has been presented. As fabricated, the ISFETs were found to have a large threshold voltage of approximately -5 V. Exposure to ultraviolet radiation and the application of a bulk-substrate bias has been shown to allow arbitrary and permanent control over V_T. It is concluded that the modification of V_T is due to the removal of trapped charge from the floating gate electrode. UV exposure is also shown to reduce ISFET-REFET V_T mismatch, which is important for differential measurements.

A circuit for making differential measurements between ISFET and REFET has been designed and fabricated. It produces and output with a maximum overall sensitivity of 400 mV/pH and consumes 2.1 mW from a single 3-V supply. A novel method of post processing that uses a single layer of photoresist to encapsulate the chip and define the sensing areas has also been developed.

The pH sensor circuit can be powered down when not in use, making it ideal for use in a low-power, battery-operated device. It can also be made available as an intellectual property block for use in a more sophisticated sensor system-on-chip (Fig. 13).

Acknowledgment

The authors would like to thank Dr. A. Glidle and Dr. B. Casey, University of Glasgow, and the design engineers at Austria Micro Systems for technical assistance.

References

[1] H.-S. Wong and M. White, "A self-contained CMOS integrated pH sensor," in *Proc. IEEE Int. Electon Devices Meeting*, Dec. 1988, pp. 658–661.

[2] L. Bousse, J. Shott, and J. Meindl, "A process for the combined fabrication of ion sensors and CMOS circuits," *IEEE Electron Device Lett.*, vol. 9, pp. 44–46, Jan. 1988.

[3] Y.-L. Chin, J.-C. Chou, T.-P. Sun, W.-Y. Chun, and S.-K. Hsiung, "A novel pH sensitive ISFET wth on chip temperature sensing using CMOS standard process," *Sens. Actuators B*, no. 76, pp. 582–593, 2001.

[4] J. Bausells, J. Carrabina, A. Errachid, and A. Merlos, "Ion-sensitive field-effect transistors fabricated in a commercial CMOS technology," *Sens. Actuators B*, vol. 57, pp. 56–61, 1999.

[5] P. Bergveld, "Development of an ion-sensitive solid-state device for neurophysiological measurements," *IEEE Trans. Biomed. Eng.*, pp. 70–71, Jan. 1970.
[6] C. Jakobson and Y. Nemirovsky, "$1/f$ noise in ion sensitive field effect transistors from subthreshold to saturation," *IEEE Trans. Electron Devices*, vol. 49, pp. 259–261, Feb. 1999.
[7] R. Smith and D. Scott, "An integrated sensor for electrochemical measurements," *IEEE Trans. Biomed. Eng.*, vol. 33, pp. 83–90, Jan. 1986.
[8] P. Bergveld, A. van den Berg, P. van der Wal, M. Skowronska-Ptasinska, E. Sudhölter, and D. Reinhoudt, "How electrical and chemical requirements for REFETs may coincide," *Sens. Actuators B*, vol. 18, pp. 309–327, 1989.
[9] A. Errachid, J. Bausells, and N. Jaffrezic-Renault, "A simple REFET for pH detection in differential mode," *Sens. Actuators B*, vol. 60, no. 43–48, 1999.
[10] L. Ravezzi and P. Conci, "ISFET sensor coupled with CMOS read-out circuit microsystem," *IEE Electron. Lett.*, 1998.
[11] B. Palán, F. Santos, J. Karam, B. Courtois, and M. Husák, "New ISFET sensor interface circuit for biomedical applications," *Sens. Actuators B*, vol. 57, pp. 63–68, 1999.
[12] J. Muñoz, A. Bratov, R. Mas, N. Abramova, C. Domínguez, and J. Bartrolí, "Planar compatible polymer technology for packaging of chemical microsensors," *J. Electrochem. Soc.*, vol. 143, no. 6, pp. 2020–2025, 1996.
[13] A. Bratov, J. Muñoz, C. Dominguez, and J. Bartrolí, "Photocurable polymers applied as encapsulating materials for ISFET production," *Sens. Actuators B*, vol. 24, pp. 823–825, 1995.
[14] Y. Berg, T. Lande, and Ø. Næss, "Programming floating-gate circuits with UV-activated conductances," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 12–19, Jan. 2001.
[15] D. Krick, P. Lenahan, and J. Kanicki, "Electrically active point defects in amorphous silicon nitride: an illumination and charge injection study," *J. Appl. Phys.*, vol. 64, no. 7, pp. 3558–3563, 1988.
[16] C. Jakobson, U. Dinnar, M. Feinsod, and Y. Nemirovsky, "Ion-sensitive field-effect transistors in standard CMOS fabricated by post processing," *IEEE Sensors J.*, vol. 2, pp. 279–287, Aug. 2002.
[17] S. Jamasb, S. Collins, and R. Smith, "A physical model for drift in pH ISFETs," *Sens. Actuators B*, vol. 49, pp. 146–155, 1998.
[18] S. Jamasb, J. Churchill, S. Collins, and R. Smith, "Accurate continuous monitoring using ISFET-based biosensors based on characterization and modeling of drift and low frequency noise," in *Proc. IEEE 20th Annu. Int. Conf. Engineering in Medicine and Biology Society*, vol. 20, Oct. 29–Nov. 1 1998, pp. 2864–2867.

Paul A. Hammond received the M.Eng. degree in electrical and information sciences from the University of Cambridge, Cambridge, U.K., in 1999, and the Ph.D. degree from the University of Glasgow, Glasgow, U.K., in 2004.

He was with STMicroelectronics as a CMOS Analogue Circuit Designer. His interests include the use of system-on-chip techniques for sensing applications.

Danish Ali received the B.A. degree in natural sciences and the M.A. degree from the University of Cambridge, Cambridge, U.K., in 1988 and 1992, resepctively, and the Ph.D. degree in microelectronics from the Cavendish Laboratory, University of Cambridge, in 1994.

In 1995, he joined Philips Research Laboratories, Redhill, U.K., initially in the Cordless Communications Group, but more recently in the Wireless Group, where he has been doing research on circuit design and system optimization for wireless communication devices. His interests include baseband signal processing and analog-to-digital conversion.

David R. S. Cumming received the B.Eng. degree from the University of Glasgow, Glasgow, U.K. in 1989 and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1993.

He has worked variously on mesoscopic device physics, RF characterization of novel devices, fabrication of diffractive optics for optical and submillimeter wave applications, diagnostic systems, and microelectronic design. He is presently a Professor and EPSRC Advanced Research Fellow in electronics and electrical engineering at the University of Glasgow, where he leads the Microsystem Technology Research Group.