Impact of Random Dopant Induced Fluctuations on Sub-15nm UTB SOI 6T SRAM Cells

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Abstract: The CMOS scaling increases the impact of intrinsic parameter fluctuation on the yield and functionality of SRAM. A statistical circuit simulation framework which can fully capture intrinsic parameter fluctuation information into the compact model has been developed. The impact of discrete random dopants in the source and drain regions on 6T SRAM cells has been investigated for well scaled Ultra Thin Body (UTB) SOI MOSFETs with physical channel length in the range of 10nm to 5nm.

Introduction: Around the 90nm technology node, intrinsic parameter fluctuations will drasticaly reduce the noise margin and overall speed in SRAM based on conventional MOSFETs [1]. SRAMs based on UTB SOI MOSFETs will outperform the conventional MOSFETs one due to superior electrostatic integrity, significant reduction of collective junction capacitance on the bitline and improved intrinsic parameter fluctuations. Although UTB device can operate without dopant within the channel region there are necessarily discrete random dopants in the source/drain regions that will introduce fluctuations in the effective channel length and access resistance at nanoscale dimensions.

Simulation Methodology: The physical parameters of carefully scaled UTB SOI MOSFETs are summarised in Table 1. In order to capture statistical variation associated with the discrete random dopants in the source and drain regions as illustrated in Fig. 1, an ensemble of 200 macroscopically identical, but microscopically different devices is created and simulated using the Glasgow 3D 'atomistic' drift diffusion simulator [2].

An improved two-stage statistical parameter extraction methodology [3] is employed to capture all device fluctuation information obtained from the 3D 'atomistic' simulator into a representative set of BSIMSOI-FD compact models library. Fig. 2(a) illustrates the quality of BSIMSOI extraction from 3 extreme cases of the physically simulated I_D-V_G characteristics. The static transfer characteristics of the 6T SRAM cells is depicted in Fig. 2(b). Transistors in the SRAM circuit are randomly selected from the compact models library during SPICE simulation of 1, 2 and 3 cell ratio.

Results and Discussions: Figure 3 illustrates the distribution of the static noise margin (SNM) due to discrete random doping for SRAM cells with different cell ratios, corresponding to each channel length being investigated here. It clearly follows the expected trend that increasing cell ratio improves cell stability although it delivers less improvement of the SNM with smaller channel length. The SRAMs based on 5nm transistors could not achieve the required yield even at cell ratio 3, while 10nm and 7.5nm requires at least a cell ratio of 2 and 3 respectively. Typical write operation stability considering quasi-static operation is shown in Table 3. The relative read operation speed of the different cells is obtained by measuring the discharge time for the bitline as shown in Fig. 4 and Table 4. As a measure of the write times, the worst-case flip time of the bitlines was recorded as shown in Table 5. Roughly the discrete random dopants will cause 40% performance difference for read operation and less then 5% difference for write operation.

Conclusions: UTB SOI MOSFETs could extend the benefits of SRAM scaling beyond the 65nm technology node [5]. However, novel device architectures such as Double Gate MOSFETs are required after the 10nm channel length mark. It is important that each potential sources of intrinsic parameter fluctuation is carefully studied to fully map their impact on the corresponding SRAM cell generations.

References

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Channel Length (nm)	10	7.5	5
Gate Oxide Thickness, T_{ox} (nm)	0.67	0.5	0.33
Body Thickness, T_{si}(nm)	2.5	2.25	2.0
Buried Oxide Thickness, T_{box}(nm)	50		
Channel Doping, N_a (cm^{-3})	1e14		
source-drain Doping, $N_{s/d}$ (cm^{-3})	2e20		

Table 1: Generic device parameters considered.

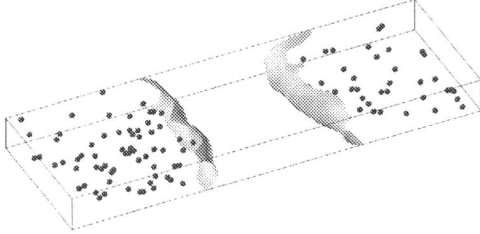

Fig. 1: Location of discrete random dopants in the source/drain regions and corresponding variation of effective channel length in the silicon body of a 10nm UTB SOI MOSFET.

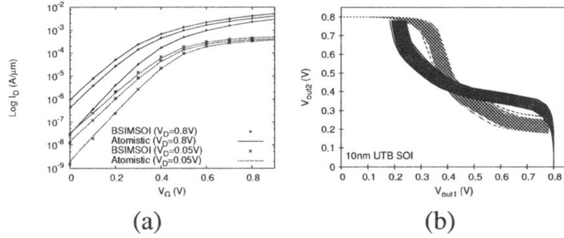

Fig. 2: (a) Compact model calibration of gate characteristics for 3 extreme fluctuation cases of 10nm channel length. All characteristics are from nMOSFET UTB SOI. (b) Static transfer characteristics of 200 statistical 6T SRAM cells utilising 10nm UTB MOSFET with a cell ratio of 1.

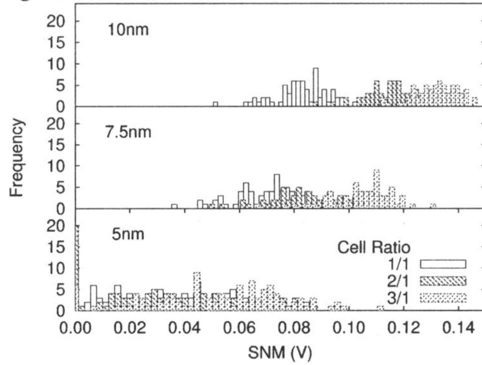

Fig. 3: Static Noise Margin Distributions.

	Cell Ratio	Mean, μ(mV)	SD, σ(mV)	σ/μ(%)
10nm	1	81.9	10.1	12.3
	2	115.4	7.8	6.7
	3	132.9	7.1	5.3
7.5nm	1	70.2	11.5	16.5
	2	89.8	12.3	13.7
	3	106.2	10.7	10.1
5nm	1	34.0	22.1	65.0
	2	37.5	23.9	63.7
	3	53.8	23.5	43.6

Table 2: Static Noise Margin distributions during read operation. The Static Noise Margin (SNM) is the minimum DC noise voltage needed to flip the cell state. As a guideline, μ-6σ is required to exceed 4% of the supply voltage to achieve 90% yield on 1Mbit SRAM [4].

	Cell Ratio	Mean, μ(mV)	SD, σ(mV)	σ/μ(%)
10nm	1	542	17	3.2
	2	586	18	3.1
	3	612	19	3.1
7.5nm	1	473	27	5.7
	2	512	26	5.1
	3	534	27	5.0
5nm	1	451	57	12.6
	2	485	58	12.0
	3	505	56	0.11

Table 3: Switch Point Voltage distributions . The write operation stability could be measured by switch point voltage which is defined as the bit line voltage that will cause data to begin to change under a write operation.

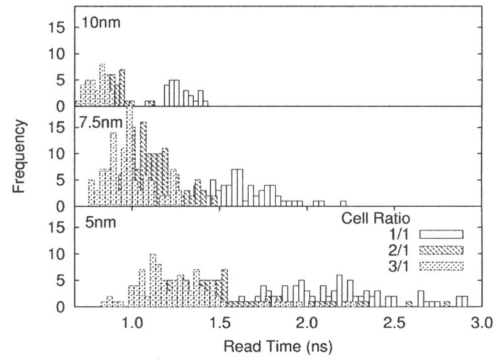

Fig. 4: SRAM read discharge time distribution.

	Cell Ratio	Mean, μ(ns)	SD, σ(ns)	σ/μ(%)
10nm	1	1.28	0.073	5.7
	2	0.91	0.053	5.8
	3	0.79	0.048	6.2
7.5nm	1	1.65	0.196	11.8
	2	1.14	0.129	11.2
	3	0.98	0.114	11.6
5nm	1	2.09	0.366	17.5
	2	1.49	0.299	20.0
	3	1.28	0.257	20.1

Table 4: SRAM read discharge time distribution. The read discharge time is measured when one of the bitlines is reduced to half of the supply voltage after the wordline is raised.

	Cell Ratio	Mean, μ(ps)	SD, σ(ps)	σ/μ(%)
10nm	1	231.4	3.91	1.69
	2	234.0	4.29	1.83
	3	236.1	4.66	1.97
7.5nm	1	241.8	7.77	3.21
	2	244.8	8.46	3.46
	3	247.3	9.30	3.76
5nm	1	255.8	21.82	8.53
	2	260.3	25.30	9.72
	3	265.0	29.91	11.29

Table 5: SRAM Write time distribution. The flip time was measured from the time the wordline was raised after placing an opposite value on the bitlines to when the latter of the two storage nodes reached 90% of its final value.