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SiGe p-channel MOSFETs with tungsten gate


A self-aligned SiGe p-channel MOSFET tungsten gate process with 0.1 μm resolution is demonstrated. Interface charge densities of MOS capacitors realised with the low pressure sputtered tungsten process are comparable with thermally evaporated aluminium gate technologies (5 × 10¹⁰ cm⁻² and 2 × 10¹⁰ cm⁻² for W and Al, respectively). Initial results from 1μm gate length SiGe p-channel MOSFETs using the tungsten-based process show devices with a transconductance of 33 mS/mm and effective channel mobility of 190 cm²/Vs.

Introduction: Recently there has been significant improvement in the performance of SiGe p-channel MOSFETs, strained Si n-channel MODFETs and scaled bulk Si devices [1 - 3]. The motivation for these enhancements is driven by CMOS shrinkage requirements, but also by the goal of realising microwave and millimetre wave Si-based transceiver circuitry compatible with a standard CMOS process flow.

One of the outstanding technological issues limiting the performance of 0.1μm gate length Si-based MOSFETs for both CMOS and RF applications is the high resistance of conventional polysilicon gate processes [4]. This has led to the development of complex silicide and salicide gate stack processes [5] as well as the demonstration of metal gate CMOS devices [6].

In this Letter a self-aligned SiGe p-channel MOSFET tungsten gate technology with 0.1μm resolution is described, together with the first results on 1μm gate length SiGe p-channel MOSFETs realised with the process.

![Layer structure showing percentage of Ge concentration, and SEM of 100nm W gate](image)

**Fabrication:** The layer structure on which devices are fabricated was grown by MBE and is shown in Fig. 1a. Using both step and linear grading, a maximum Ge concentration of 40% in the channel was achieved. The 200nm buffer layer, doped at 5 × 10¹⁶ cm⁻³ n-type with Sb, is grown on an n-type Si substrate doped at 5 × 10¹⁶ cm⁻³. The channel comprises three layers: a 2nm SiGe layer graded from 0 to 10% Ge followed by a 10nm SiGe layer graded from 10 to 40% Ge, then a 5nm SiGe layer graded from 40 to 0% Ge. Approximately 5nm of the 10nm Si cap layer is consumed during the cleaning and oxidation processes. All layers above the buffer are nominally undoped at a background level of 10¹⁵ cm⁻³ n-type.

The device process flow begins with the growth of a 6nm gate oxide using a 200min dry thermal oxidation performed at 750°C to prevent any out-diffusion of Ge during the oxide growth. A further 30min 750°C anneal in an argon atmosphere results in a device quality oxide layer. Next, the 100nm thick tungsten gate is deposited by RF sputtering at a pressure of 2mtorr and power of 100W. To enable an assessment of the damage induced by the sputtered tungsten process to be made, 100nm thick thermally evaporated aluminium gate MOS capacitors were also defined for comparison.

Tungsten gates with minimum feature sizes of 100nm as shown in Fig. 1b, were fabricated using a Leica Microsystems Lithography LTD EBPG5 beamwriter and AZPN114 negative tone resist to define the geometry, followed by tungsten patterning with a 2min, 100W SF₆ reactive ion etch performed at 9mtorr. In situ reflectometry was used during the SF₆ etch to stop the gate metal etch on the thin 6nm SiO₂ layer [7]. The self-aligned source and drain contacts were produced using a shallow (< 100nm) BF₂ implant at an energy of 10keV and a dose of 10¹⁵ atom/cm² activated by a 10s 900°C anneal. Source and drain metallisation of 100nm AlSi was followed by a 5min 400°C anneal. Finally, the devices were shallow trench isolated with a 5min, 100W SF₆ reactive ion etch performed at 9mtorr.

![CV characteristics of W and Al MOS capacitors (20nm thick oxide)](image)

![I-V and gₜ characteristics of 1μm × 100μm p-SiGe W gate MOSFET](image)
**Results:** Fig. 2 shows the CV curve of SiGe-SiO₂ capacitors realised using both the sputtered tungsten and evaporated aluminium gate metallisations. The interface charge densities calculated from the flatband voltage shifts are $5 \times 10^{10}$ cm⁻² and $2 \times 10^{10}$ cm⁻² for W and Al, respectively, showing that the sputtered tungsten gate process causes only a small amount of damage. In addition the larger work function of tungsten results in a lower flatband voltage and thus a reduced threshold voltage when compared with the aluminium gate capacitors.

Using both the van der Pauw and four probe TLM methods, the resistivity of the 100 nm thick sputtered tungsten gate metal film was determined to be 1.2 Ω·cm, a factor of 3 lower than similar geometry polysilicon and silicide gate structures [8]. The measured resistivity was independent of gate length down to 100 nm.

Fig. 3 shows the $I_D(V_D)$ and $g_m(V_D)$ characteristics of a 1 × 100 nm gate length SiGe MOSFET realised using the process described above. The maximum extrinsic transconductance is 33 mS/mm characteristic of the device and accounting for the channel extrinsic transconductance of 33 mS/mm and 2 × 10¹¹ cm⁻² for W and Al, respectively, indicating that this a low damage process. The use of a tungsten gate produces devices with gate resistances of 1.2 Ω/cm independent of gate length down to 100 nm, making this process an attractive candidate for the realisation of low gate resistance devices for RF applications.

Initial results from 1 μm gate length SiGe p-channel MOSFETs using the tungsten-based self-aligned gate process yielded a transconductance of 33 mS/mm and effective channel mobility of 190 cm²/Vs.

**Conclusion:** We have demonstrated a self-aligned SiGe p-channel MOSFET tungsten gate process with 0.1 μm resolution. Interface charge densities of MOS capacitors realised with the low pressure sputtered tungsten process are comparable with thermally evaporated aluminium gate technologies ($5 \times 10^{10}$ cm⁻² and $2 \times 10^{10}$ cm⁻² for W and Al, respectively) indicating that this a low damage process. The use of a tungsten gate produces devices with gate resistances of 1.2 Ω/cm independent of gate length down to 100 nm, making this process an attractive candidate for the realisation of low gate resistance devices for RF applications.

A novel SD junction technology for realise sub-0.1 μm NMOSFETs is proposed. In this technology, SD extensions are formed using arsenic (As) diffusion from an As adsorbed atomic layer on the silicon surface by high temperature RTA. This method provides an extremely shallow extension (below 20 nm) with low sheet-resistance (below 2 kΩ/sq), maintaining a low junction leakage. NMOSFETs fabricated using this technology show better suppression of the short channel effect compared to conventional FETs.

**Introduction:** In sub-0.1 μm NMOSFETs, an extremely shallow junction in a source and drain region is required to suppress a short channel effect (SCE). Recent shallow doping methods instead of low energy As implantation have mainly used phosphorus ion as a dopant [1]. Although As is the preferred N-type dopant in the shallow junction formation, another As doping method apart from ion implantation has not been presented until now.

In this Letter, we investigate the As diffusion from an As adsorbed atomic layer on the silicon surface, and propose process conditions to achieve ultra-shallow junction with low resistance and low junction leakage. Finally, the device characteristics of sub 0.1 μm NMOSFETs fabricated by this method are evaluated.

![Ultra-shallow junction technology by atomic layer doping from arsenic adsorbed layer](image)

**Ultra-shallow junction technology by atomic layer doping from arsenic adsorbed layer**

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A novel SD junction technology for realise sub-0.1 μm NMOSFETs is proposed. In this technology, SD extensions are formed using arsenic (As) diffusion from an As adsorbed atomic layer on the silicon surface by high temperature RTA. This method provides an extremely shallow extension (below 20 nm) with low sheet-resistance (below 2 kΩ/sq), maintaining a low junction leakage. NMOSFETs fabricated using this technology show better suppression of the short channel effect compared to conventional FETs.

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**References**


**Fig. 1 Typical SIMS profiles under different RTA conditions of As atomic layers formed by AsH₃ injection at 550 °C for 30min**

**Shallow junction formation:** The As layer doping consists of three essential steps. First, AsH₃ is supplied to the silicon surface for the As layer formation. Secondly, non-doped silicon glass (NSG) film, used as a capping film, is deposited on the As adsorbed layer by using the APCVD method. Thirdly, rapid thermal annealing (RTA) is carried out. The maximum As coverage (0.95 monolayer) on the silicon surface was obtained at AsH₃ reaction temperature.