Intrinsic Parameter Fluctuations in Decananometer MOSFETs Introduced by Gate Line Edge Roughness

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***Abstract*—In this paper, we use statistical three-dimensional (3-D) simulations to study the impact of the gate line edge roughness (LER) on the intrinsic parameters fluctuations in deep decananometer (sub 50 nm) gate MOSFETs. The line edge roughness is introduced using a Fourier synthesis technique based on the power spectrum of a Gaussian autocorrelation function. In carefully designed simulation experiments, we investigate the impact of the rms amplitude Δ and the correlation length Λ on the intrinsic parameter fluctuations in well scaled, but simple devices with fixed geometry as well as the channel length and width dependence of the fluctuations at fixed LER parameters. For the first time, we superimpose in the simulations LER and random discrete dopants and investigate their relative contribution to the intrinsic parameter fluctuations in the investigated devices. For particular MOSFET geometries, we were able to identify the regions where each of these two sources of intrinsic parameter fluctuations dominates.**

***Index Terms*—Intrinsic parameter fluctuation, line edge roughness (LER), MOSFETs, numerical simulation, random discrete dopants.**

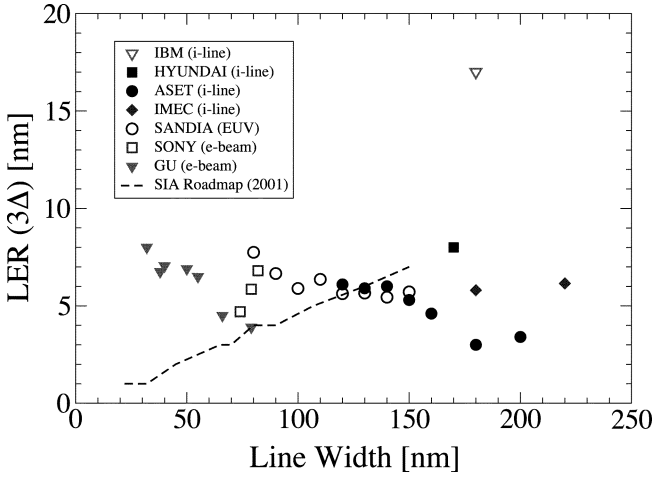

Fig. 1. Actual data from various advanced lithography processes reported by different labs showing that LER does not scale with linewidth according with the Roadmap requirements.

I. Introduction

In THE past couple of years, MOSFETs have reached deep decananometer (sub 50-nm) dimensions with 40–50-nm physical gate length devices developed now for the 90-nm technology node [1], [2], 35-nm transistors ready for mass production in 2–3 years time [3] and 10-nm MOSFETs with conventional architecture demonstrated in a research environment [4]. Intrinsic parameter fluctuations play an increasingly important role in such devices at a time when the fluctuation margins shrink due to reduction in supply voltage and increased transistors count per chip. Various sources of intrinsic parameter fluctuations have been studied using numerical simulations with a preference given in the past to random discrete dopants in the active region of the transistor [5]–[7], random dopants and grain boundaries in the polysilicon gate [8] and oxide thickness fluctuations [9]. The line edge roughness (LER) caused by tolerances inherent to materials and tools used in the lithography processes is yet another source of intrinsic parameter fluctuations [10], [11] which needs close attention.

LER has caused little worry in the past since the critical dimensions of MOSFETs were orders of magnitude larger than the roughness. However, as the aggressive scaling continues into the decananometer regime, LER does not scale accordingly, becoming an increasingly larger fraction of the gate length. As shown in Fig. 1 the edge roughness remains typically on the order of 5 nm almost independently of the type of lithography used in production or research [10], [12]–[17]. Although attempts have been made to simulate analytically the impact of the gate edge roughness on leakage [18] they rely on fitting parameters and lack predictive power due to the complex three-dimensional (3-D) nature of the problem. Previous efforts to numerically model edge roughness effects were limited in terms of realism and sophistication due to the massive computational resources needed to perform statistical simulations on realistic 3-D geometries. Pioneering 3-D simulation studies treat the problem deterministically using a "square wave" approximation for the gate edge [19], [20]. The simplified statistical approach adopted in [10], [21], [22] is based on 2-D simulations of samples of MOSFETs with statistical variations in the channel length but fixed channel width. The attempt to validate this approach using 3-D simulations reveals more than 30% discrepancy in the 3σ estimates of the off-current [10] which is most sensitive to multidimensional short channel effects.

Here, we present a full-scale 3-D statistical simulation approach to investigate mainly the impact of gate edge roughness

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on the intrinsic parameter fluctuations in decananometer MOSFETs. The gate edge is generated using Fourier synthesis, which preserves the statistical properties of the LER in the simulations. For fixed device geometry, we study the impact of the rms amplitude Δ and the correlation length Λ on the variation in the off-current $I_{\rm off}$, on-current $I_{\rm on}$, and threshold voltage V_T. We also study the dependence of the variations on the device geometry. Finally, for the first time we study the simultaneous effect of LER and random discrete dopants on the intrinsic parameter fluctuations in decananometer MOSFETs.

II. Simulation Approach

In this paper, we employ the Glasgow 3-D "atomistic" device simulator described in greater detail elsewhere [7], [23]. The LER modeling approach used to generate random junction patterns is based on a 1-D Fourier synthesis technique and generates gate edges from the power spectrum corresponding to Gaussian or exponential autocorrelation functions. The parameters used are the rms amplitude Δ and correlation length Λ. Experimentally, Δ can be thought of as the standard deviation of the x-coordinate of the gate edge, if the gate is parallel to the y-direction. The correlation length, Λ, is obtained by fitting of a particular type of autocorrelation function to the gate edge line. It should be noted that the value quoted as "LER" is traditionally defined to be 3Δ. In the random line generation algorithm, first a complex array with N elements is constructed, whose amplitude is determined by the power spectrum obtained from the adopted autocorrelation function as follows:

$$S_G(k) = \sqrt{\pi}\,\Delta^2\Lambda e^{-(k^2\Lambda^2/4)} \tag{1}$$

$$S_E(k) = \frac{2\Delta^2\Lambda}{1+k^2\Lambda^2}. \tag{2}$$

S_G and S_E are the power spectra for Gaussian and exponential autocorrelation functions, respectively. $k = i\,(2\pi/N\,dx)$ where dx is the discrete spacing used for the line and $0 \le i \le N/2$. The phases of the elements are selected randomly, making each line unique. However, only $(N/2-2)$ elements of the array are independent. The rest are obtained by symmetry operations imposed so that, after inverse Fourier transform, the resulting "height" function $H(x)$ is real. Random line examples generated using this method are given in Fig. 2 for typical values of Δ and Λ. Lines generated from a Gaussian autocorrelation function are smoother due to a lack of high frequency components which are characteristic of the corresponding exponential power spectrum.

In contrast with the numerous values of LER, or Δ, published in the literature for different lithography processes (most of which are currently in the range of 5 nm as depicted in Fig. 1), significantly less is known about the corresponding correlation length, which is reported to vary between 10 and 50 nm [10]. Our own analysis of SEM micrographs of resist lines obtained from EUV [15] and e-beam [17] lithography indicates values of Λ in the range of 20–30 nm. Gaussian and exponential power spectral models are found to perform almost equally well as least square fits to the captured autocorrelation data [11] as shown in Fig. 3. It is reasonable to assume that Λ and also Δ may be reduced at higher resolution, which can utilize special

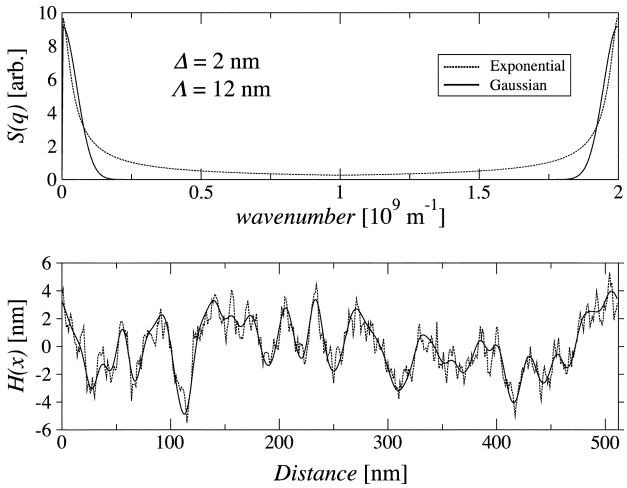

Fig. 2. Example of statistical generation of LER data used in the 3-D device simulator. Both the power spectra (top) and actual random lines (bottom) are shown.

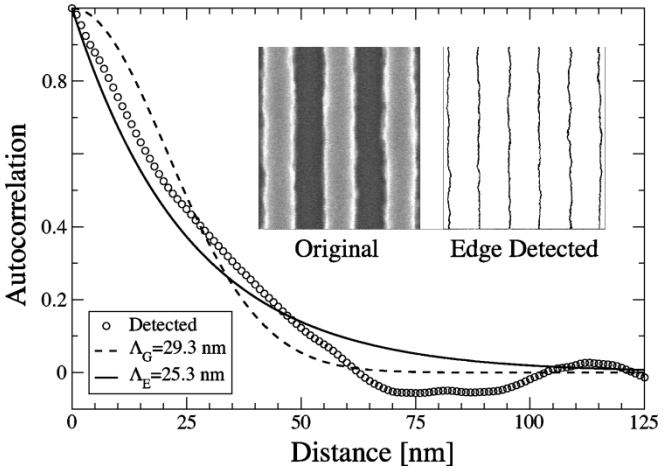

Fig. 3. Autocorrelation of LER captured from 100 nm EUV lines. Correlation lengths obtained from Gaussian (Λ_G) and exponential (Λ_E) fits and detected edges are also given.

resists and/or advanced exposure techniques for better LER performance. Therefore we explore a broader range of values for there parameters in our simulations.

For the sake of simplicity and speed we use the drift-diffusion (DD) approximation, with constant mobility, in the simulations. Although the DD approach, particularly in combination with a constant mobility, cannot describe accurately the correct magnitude of the current in the decananometer MOSFETs it gives a good indication of the expected percentage parameter variations associated with the device electrostatics. Therefore in the forthcoming figures we present only the relative variation in $I_{\rm on}$. In the "atomistic" simulations the effects associated with mobility and carrier velocity variation, due to variation in the coulomb scattering from different ionized impurity configurations in each microscopically different MOSFET, are also excluded.

In the simulated MOSFETs the shape of the surface p-n junction replicates the gate edge profile and follows, in depth, a Gaussian 2-D doping profile. No smearing of the lateral p-n junction edge due to 3-D implantation effects or thermal processing is taken into account. Bearing in mind that with the

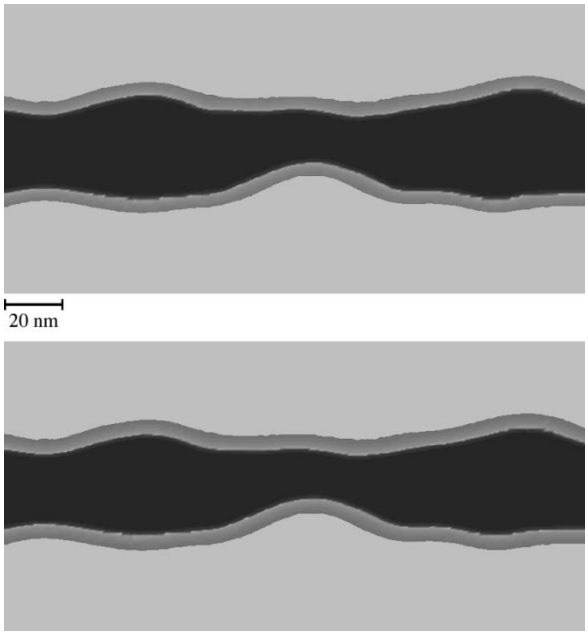

Fig. 4. Gate and p-n junctions profiles from Taurus process simulation of a 35-nm channel length MOSFET including LER after (a) ion implantation; (b) 30 s RTA at 900 °C.

scaling of devices below 50 nm the typical LER correlation length becomes larger than the junction depth, such an approach is not as crude as it might appear at first. To verify this assumption we have carried out, using the 3-D process simulator Taurus–Process [24], detailed process simulations of a real 35 nm transistors reported in [3] including edge roughness with $\Lambda = 20$ nm and $\Delta = 2$ nm. As can be seen from Fig. 4(a) and (b) for correlation length 20 nm the p-n junction closely follows the shape of the gate edge both after the implantation and after 30 s RTA at 900 °C. Although the RTA increases the lateral junction penetration by approximately 1 nm for the chosen correlation length, this is not sufficient to smooth the initial features of the poly-Si gate edge. For shorter correlation lengths and/or large thermal budgets Dt this assumption may not be 100% accurate [10] but could be considered as a worst-case scenario. The expected smearing of the high frequency features in the edge profile due to implantation and subsequent diffusion is also the reason for choosing to use, in the simulations presented here, the smoother edge profile generated from the power spectrum corresponding to a Gaussian autocorrelation function.

In the "atomistic" simulations the random discrete dopants in the case of straight or rough gate edges are generated from the continuous doping distribution using a rejection technique. Ensembles of 200 MOSFETs with identical design parameters but different gate edge patterns and/or discrete dopant distributions are used to extract averages and standard deviations.

III. Simulation Results

In order to simplify the interpretation of the results in our study, we consider MOSFETs with simple architecture and typical effective channel length $L_{\text{eff}} = 30$ nm or 50 nm. The simulated devices have uniform doping concentration in the channel $N_A = 5 \times 10^{18}$ cm^{-3} and gate oxide thickness of $t_{ox} = 1.3$ nm

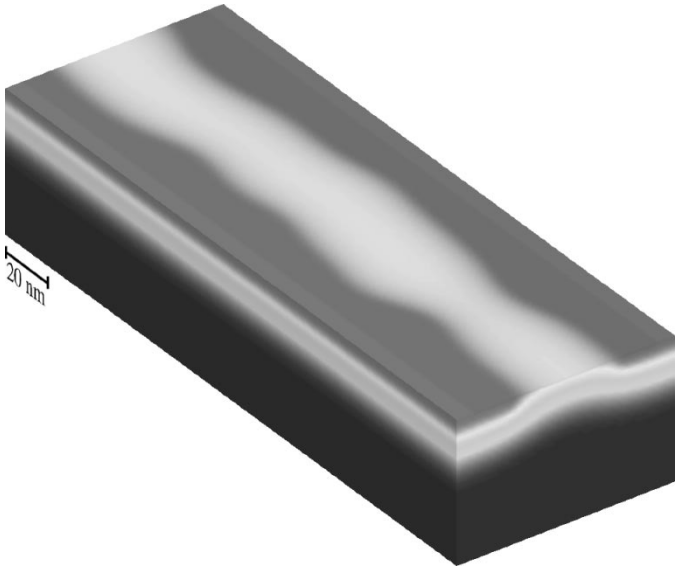

Fig. 5. Potential distribution in a typical 30 × 200 nm MOSFET with LER used in this study. The LER parameters are $\Lambda = 20$ nm and $\Delta = 2$ nm.

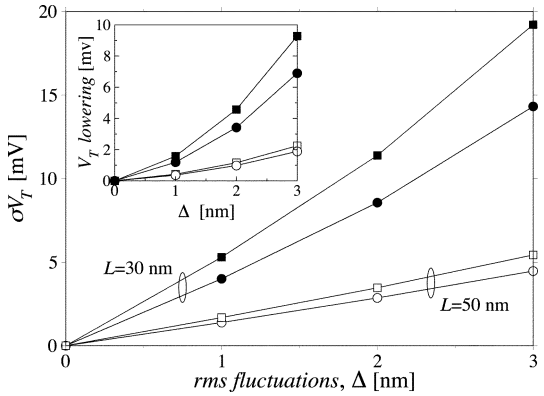

Fig. 6. Standard deviation of threshold voltage σV_T for 30 × 50 and 50 × 50 nm MOSFETs as a function of RMS fluctuations, Δ, at $V_D = 1.0$ V (squares) and $V_D = 0.1$ V (circles).

resulting in a threshold voltage $V_T = 0.2$ V and subthreshold slope $S = 78$ mV/decade. The junction depth is kept small ($x_j = 7$ nm) in order to suppress short channel effects without the use of pockets. The potential distribution in a typical 30 × 200 nm MOSFET with LER used in this study at gate voltage $V_G = V_T$ and drain voltage $V_D = 0.01$ V is illustrated in Fig. 5. The potential follows approximately the shape of the metallurgical p-n junction although some field crowding is visible around indentations in the channel which tends to smooth the variations in the length of the conducting channel.

A. LER With Continuous Doping

In order to establish a link and similarities with previous results on intrinsic parameter fluctuations induced by random discrete dopants we first study the LER induced threshold voltage fluctuations. Similar to random discrete dopants [5], [7], the random LER introduced threshold voltage fluctuations in devices with otherwise identical design parameters even when continuous doping is used in the simulations. For given device dimensions the standard deviation in threshold voltage due to LER increases when Δ or Λ is increased. The former dependence is illustrated in Fig. 6 for 30 × 50 and 50 × 50 nm

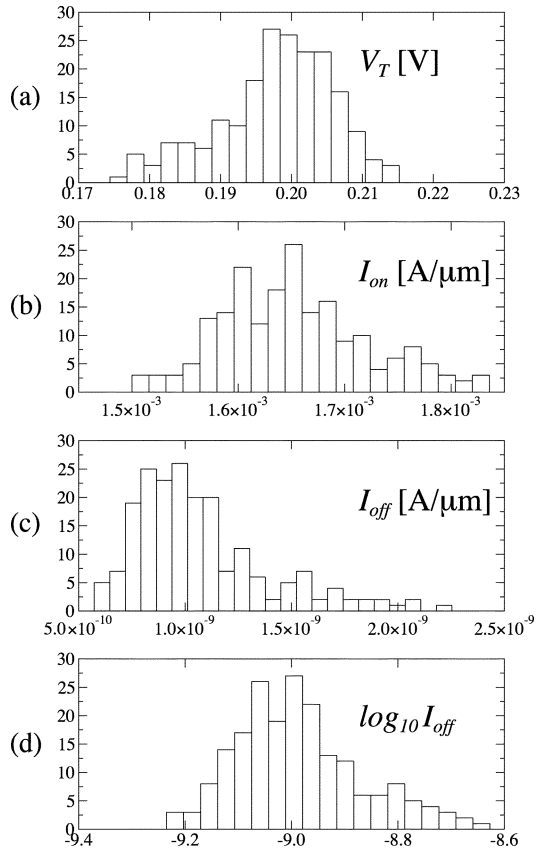

Fig. 7. Distributions of the (a) threshold voltage (b) on-current and (c) and (d) off-current in a 30 × 50 nm MOSFETs corresponding to LER with $\Lambda = 20$ nm and $\Delta = 2$ nm, obtained from simulations at low drain voltage $V_D = 0.1$ V.

MOSFETs assuming LER correlation length $\Lambda = 20$ nm. Also, similar to the "atomistic" simulations [5], [7], the introduction of LER results in threshold voltage lowering compared to the threshold voltage V_{T0} of the generic device with straight gate edges. The inset in Fig. 6 plots the average threshold voltage lowering, $\langle V_T \rangle - V_{T0}$. The threshold voltage fluctuations increase with the increase in the drain voltage. For given LER parameters both the threshold voltage fluctuations and lowering increase as gate dimensions are reduced. Moreover, the fluctuations are comparable in magnitude to those resulting from random dopants in similar 30 nm devices [7].

Typical distributions of threshold voltage, on- and off-currents in 30 × 50 nm MOSFETs corresponding to LER with $\Lambda = 20$ nm and $\Delta = 2$ nm, obtained from simulations at low drain voltage $V_D = 0.1$ V, are illustrated in Fig. 7. As in the case of random discrete dopants [7] the threshold voltage distribution in Fig. 7(a) is close to a normal distribution. The on-current distribution [see Fig. 7(b)] is also close to normal. For the off-current the distribution is normal only on a logarithmic scale [see Fig. 7(c) and (d)]. This follows from straightforward geometrical considerations bearing in mind that the subthreshold current is linear on a semi-logarithmic scale. In the case of well-scaled devices when the subthreshold slope S remains virtually constant the relationship between the standard deviation of the threshold voltage σV_T and the standard deviation of the logarithm of the off-current $\sigma \log(I_{\rm off})$ becomes

$$\sigma \log(I_{\rm off}) = \sigma V_T / S. \tag{3}$$

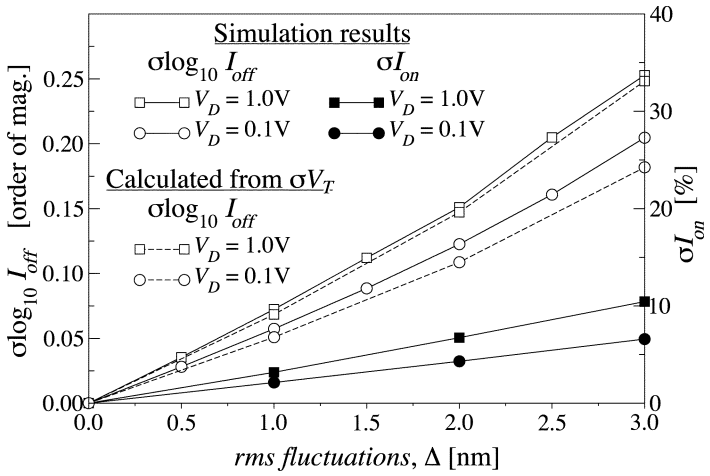

Fig. 8. Dependence of $\sigma I_{\rm on}$ and $\sigma \log(I_{\rm off})$ on the rms amplitude Δ for the 30 × 50 nm MOSFETs from 66 at the same simulation conditions used to generate the σV_T dependence. The dashed lines show $\sigma \log(I_{\rm off})$ calculated from σV_T using (3).

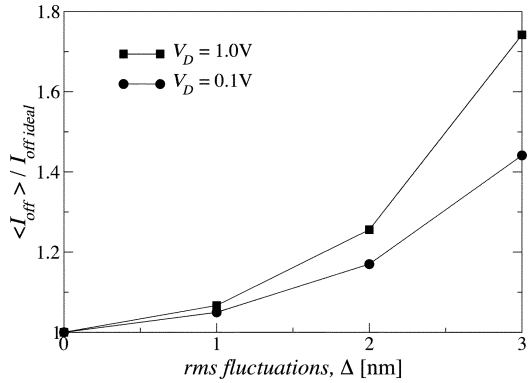

Fig. 9. Off current variation as a function of the rms amplitude Δ for the 30 × 50 nm MOSFETs. $I_{\rm off\,ideal}$ represents the off current of a device with straight gate edges.

Fig. 8 illustrates the dependence of $\sigma I_{\rm on}$ and $\sigma \log(I_{\rm off})$ on the rms amplitude Δ for the 30 × 50 nm MOSFET from Fig. 6 at the same simulation conditions used to generate the corresponding σV_T dependence. The 3-D simulation results for $\sigma \log(I_{off})$ at low and high V_D are compared with estimates based on the corresponding data for σV_T and (3). The agreement for $\sigma \log(I_{\rm off})$ is very good, pointing out that, in properly scaled MOSFETs, σV_T and $\sigma \log(I_{\rm off})$ are correlated according to (3) and the simulation of only one of them is sufficient. This is due to the fact that the subthreshold current, and the corresponding threshold voltage, are mainly determined by the close neighborhood around the shortest channel regions in the device, and dominated by the associated short channel effects. The on-current is an integral quantity and the early turning on of the shortest region of the channel, which determines the threshold voltage, is counterbalanced by the later turning on of the longer channel regions, which smoothest the on-current fluctuations.

Previous work on the simulation of LER effects have been focused mainly on the LER related degradation in the $I_{\rm off}/I_{\rm on}$ ratio [10], [18], [20], [21]. Therefore, in Fig. 9 we plot the corresponding rms amplitude dependence of the ratio between the av-

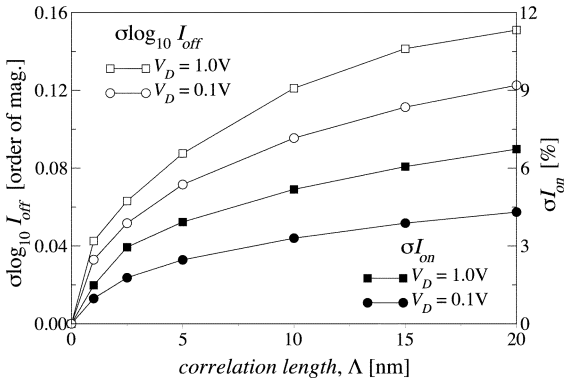

Fig. 10. Dependence of $\sigma I_{\rm on}$ and $\sigma \log(I_{\rm off})$ on the correlation length in 30 $\times$ 50 nm MOSFETs for a fixed rms amplitude $\Delta = 2$ nm.

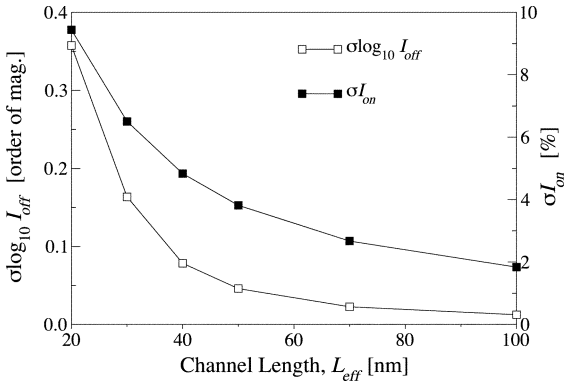

Fig. 11. Dependence of $\sigma I_{\rm on}$ and $\sigma \log(I_{\rm off})$ at fixed LER parameters $\Lambda = 20$ nm and $\Delta = 2$ nm on the channel width for a MOSFET with $L_{\rm eff} = 50$ nm calculated at $V_D = 1.0$ V.

erage off current $I_{\rm off}$ and the off current $I_{\rm off\,ideal}$ of a MOSFET with straight gate edges. An exponential increase in the leakage current is observed with the increase in Δ due to enhanced short channel effects. The magnitude of this increase is in agreement with the experimental results for similar devices reported in [22].

We have investigated the dependence of $\sigma I_{\rm on}$ and $\sigma \log(I_{\rm off})$ on the correlation length for a fixed rms amplitude, $\Delta = 2$ nm, in 30 $\times$ 50 nm MOSFETs which is illustrated in Fig. 10. After an initial increase in the fluctuations with the increase of Δ there is a well-pronounced saturation in the above dependences when the correlation length becomes comparable to the channel width.

For completeness in this section we have also studied the device geometry dependence of $\sigma I_{\rm on}$ and $\sigma \log(I_{\rm off})$ at fixed LER parameters $\Lambda = 20$ nm and $\Delta = 2$ nm. The channel width dependence for a MOSFET with $L_{\rm eff} = 50$ nm calculated at $V_D = 1.0$ V is illustrated in Fig. 11 and closely follows a $1/\sqrt{W}$ relationship. Data for the channel length dependence can be found in the next section.

B. LER With Random Discrete Dopants

In this section we superimpose random discrete dopants on top of the LER in order to understand the simultaneous effect of these two sources of intrinsic parameter fluctuations. The potential distribution in a 30 $\times$ 200 nm MOSFET identical in terms of LER with the device in Fig. 5 but also containing random discrete dopants is illustrated in Fig. 12 at gate voltage

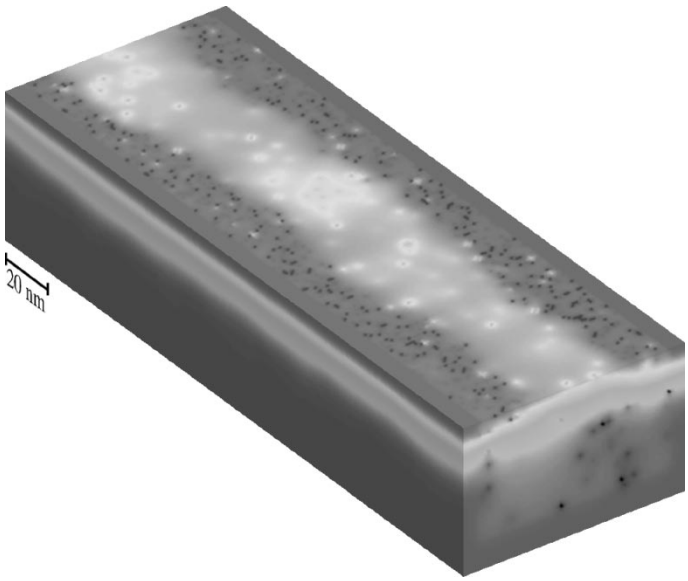

Fig. 12. Potential distribution in a typical 30 $\times$ 200 nm MOSFET with LER ($\Lambda = 20$ nm and $\Delta = 2$ nm) and random discrete dopants.

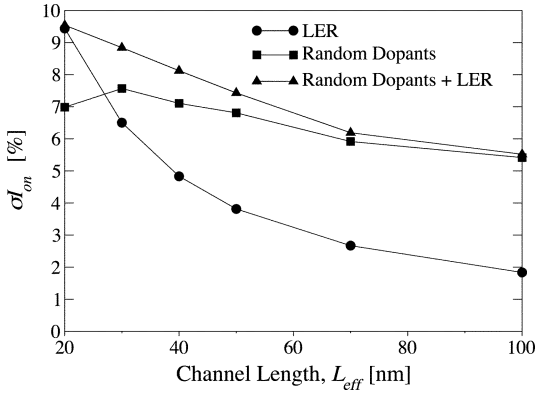

Fig. 13. Dependence of $\sigma I_{\rm on}$ on the channel length for a set of MOSFETs with channel width 50 nm. The LER parameters used to define the gate edges are $\Lambda = 20$ nm and $\Delta = 2$ nm.

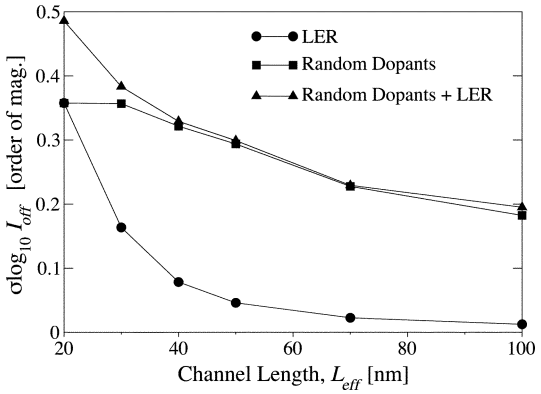

Fig. 14. Dependence of $\sigma \log(I_{\rm off})$ on the channel length for a set of MOSFETs with channel width 50 nm. The LER parameters used to define the gate edges are $\Lambda = 20$ nm and $\Delta = 2$ nm.

$V_G = V_T$ and drain voltage $V_D = 0.01$ V. Figs. 13 and 14 present $\sigma I_{\rm on}$ and $\sigma \log(I_{\rm off})$, respectively, for a set of MOSFETs with channel width 50 nm and channel lengths varying from 20 to 100 nm. Three sets of results representing: i) rough

gate edges with continuous doping; ii) straight gate edges with random discrete dopants; and iii) rough gate edges with random discrete dopants are depicted on each of the two figures. The LER parameters used to define the gate edges, $\Lambda = 20$ nm and $\Delta = 2$ nm, are typical for the advanced lithography techniques today. It is clear that within the margins of the statistical error the two sources of intrinsic parameter fluctuations, LER and random dopants, might be considered statistically independent particularly for channel lengths larger than 30 nm. The standard deviation in the simulations combining the two sources $\sigma_{\rm TOT}$ closely follows the relation $\sigma_{\rm TOT} = \sqrt{\sigma^2_{\rm LER} + \sigma^2_{RD}}$, where $\sigma_{\rm LER}$ and σ_{RD} are the standard deviations when LER and random dopants are considered independently in the simulations. The current fluctuations induced by random dopants and LER have markedly different channel length dependences. The channel length dependence associated with random dopants is weak, showing an increase in fluctuations down to 30 nm gate lengths and then some reduction. This reduction is difficult to explain based on simple analytical assumptions but might be related to screening of the channel potential by mobile charge in the heavily doped source/drain regions. The channel length dependence associated with LER is much stronger (closer to an exponential one) and explodes for channel lengths below 30 nm due to strong short channel effects in regions of reduced channel length due to coincidental combinations of LER intrusions from both sides of the gate. As a result of the different channel length dependences there is a crossover in the dominant current fluctuation source at approximately 20 nm channel length. For channel lengths above 20 nm the dominant source of fluctuations are the random dopants, but below this channel length the LER takes over and becomes the dominant fluctuation source. Due to the virtually statistical independence of the two sources the combined simulations are of particular importance only in the transitional region around 30 nm channel length. It has to be pointed out that, although the channel length at which the transition will happen depends on the MOSFET design and the LER parameters used in the simulations, the general trend of LER overtaking random dopants as a source of fluctuations at shorter channel length will remain, particularly if the scaling of LER continues to be an unresolved problem. The question of how oxide thickness variation might affect this picture and in what conditions it might become a dominant source of fluctuations still remains open and is a subject of future research.

IV. Conclusion

LER is another source of intrinsic parameter fluctuations in decananometer MOSFETs, introducing threshold voltage, on- and off-current variations on a scale similar to those introduced by random discrete dopants. This is complemented with deterioration in the $I_{\rm off}/I_{\rm on}$ ratio due to enhanced short channel effects in regions of the MOSFET channel shortened by LER. The scale of the problem depends on how successfully the future lithography techniques and materials will manage to cope with the requirement for LER scaling.

We have studied for the first time the combined effect of LER and random discrete dopants on the current fluctuations. We have demonstrated that the two sources of fluctuations act in a statistically independent manner when taken into account simultaneously in the simulations. The LER induced current fluctuations have a much stronger channel length dependence and, as devices are scaled to shorter dimensions, are expected to take over as the dominant fluctuation source from the random dopant induced current fluctuations which dominate at longer channel lengths. The transitional channel length will depend on the actual device design and the parameters describing the LER associated with the lithography process used to fabricate the devices.

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