

Research



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Cleanroom strategies for micro- and nano-fabricating flexible implantable neural electronics

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Implantable electronic neural interfaces typically take the form of probes and are made with rigid materials such as silicon and metals. These have advantages such as compatibility with integrated microchips, simple implantation and high-density nanofabrication but tend to be lacking in terms of biointegration, biocompatibility and durability due to their mechanical rigidity. This leads to damage to the device or, more importantly, the brain tissue surrounding the implant. Flexible polymer-based probes offer superior biocompatibility in terms of surface biochemistry and better matched mechanical properties. Research which aims to bring the fabrication of electronics on flexible polymer substrates to the nano-regime is remarkably sparse, despite the push for flexible consumer electronics in the last decade or so. Cleanroom-based nanofabrication techniques such as photolithography have been used as pattern transfer methods by the semiconductor industry to produce single nanometre scale devices and are now also used for making flexible circuit boards. There is still much scope for miniaturizing flexible electronics further using photolithography, bringing the possibility of nanoscale, non-invasive, high-density flexible neural interfacing. This work explores the fabrication challenges of using photolithography and complementary techniques

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in a cleanroom for producing flexible electronic neural probes with nanometre-scale features.

This article is part of the theme issue 'Advanced neurotechnologies: translating innovation for health and well-being'.

1. Introduction

Neurological disorders make up the leading cause of disability-adjusted life-years lost (DALYs) and are the second leading cause of death worldwide (9 million in 2016), second only to heart disease [1]. Two of the four most significant contributors to the DALYS are migraines and dementias – the latter of which includes Alzheimer's disease. These disorders—as well as others such as epilepsy and Parkinson's disease—could benefit enormously from a better understanding of how they manifest themselves in the brain and wider nervous system, in addition to novel treatments and procedures. Electronic neural probes that can record neural signals with high temporal and spatial resolution and stimulate with neuron-level precision have the potential to play a significant role in addressing this challenge now and in the future. This potential is reflected in significant academic research [2–5] and the emergence of countless start-up companies in this field, such as Neuralink [6], Salvia Bioelectronics B. V. and Nyxoah S. A.

Rigid brain implants like Utah and Michigan [7] style arrays, and the long electrodes used in deep brain stimulation [8], have advantages in terms of fabrication quality, resolution and consistency, but do not conform to the brain shape and are typically made of less biocompatible materials, which can lead to immune responses and inflammation (illustrated in figure 2), in the form of the activation of immune cells such as astrocytes and microglia, leading to glial scarring, device failure and neuronal cell death.[9] This is particularly the case if devices are used for long-term implantation which is common in medicine due to the prevalence of chronic conditions like Parkinson's disease and severe tremor. Devices that do not trigger this response could be implanted for longer, meaning less frequent invasive surgeries and a lower likelihood of surgery-related complications such as staph infections [10]. Devices on flexible substrates have been shown to produce much lower immune responses (illustrated in figure 1), including less inflammation, normal cell morphology and less damage to the blood-brain barrier (BBB) during insertion [11]. A comparison between rigid and flexible substrates is presented in table 1.

Modern electronics have only been scalable down to single nanometre scales because of the high purity, defect-free, flat and rigid substrate surfaces. Fabricating miniaturized electronics on flexible substrates is understandably challenging, as the electronic response changes are bound to change with mechanical stresses induced by flexibility. It is nevertheless possible to apply advanced fabrication techniques such as photolithography to flexible devices. For example, Liu *et al.* produced a device made of a spin-coated polyimide and SU-8 substrate with 25 μm Cr-Au wiring using photolithography [23]. Elon Musk's neuroscience start-up Neuralink use photolithography to produce gold on polyamide 'threads' which have diameters between 5 and 50 μm with submicron resolution [6]. Despite the advanced nature of research into polymers and nanofabrication, the niche of nanofabricating on flexible substrates is, in our opinion, underdeveloped. In this work, the focus will be solely on photolithography rather than other pattern transfer methods such as electron-beam lithography and nanoimprint lithography for three reasons: (1) the simplicity of the technique, (2) its wide adoption and (3) the remarkable fact that the Rayleigh criterion (equation (1.1)) has been overcome to produce single nanometre features, leading to Moore's law continuing to apply for half a century [24]. The criterion is the general limit for the minimum resolvable detail in imaging or the minimum distance D at which two light spots of wavelength λ can be resolved

$$D = \frac{1.22\lambda}{2n \sin \theta} = \frac{0.61\lambda}{2NA}, \quad (1.1)$$

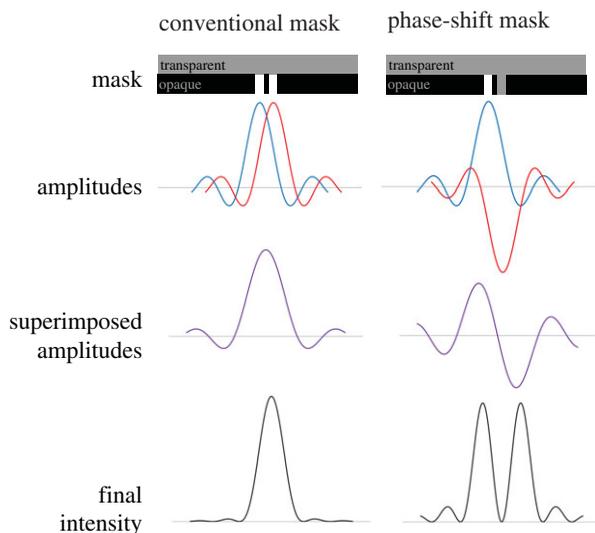


Figure 1. Comparison between how a conventional photolithographic mask and phase-shift mask work with regard to features that are of similar size to the wavelength of light used. Two neighbouring light spots in a conventional mask lead to a single large spot, as diffraction means that the two spots cannot be discriminated. In the phase-shift mask, a transparent element is added to shift the phase of one of the spots, leading to destructive interference in the space between the spots, resulting in two spots which can be smaller than the limit described by the Rayleigh criterion. (Online version in colour.)

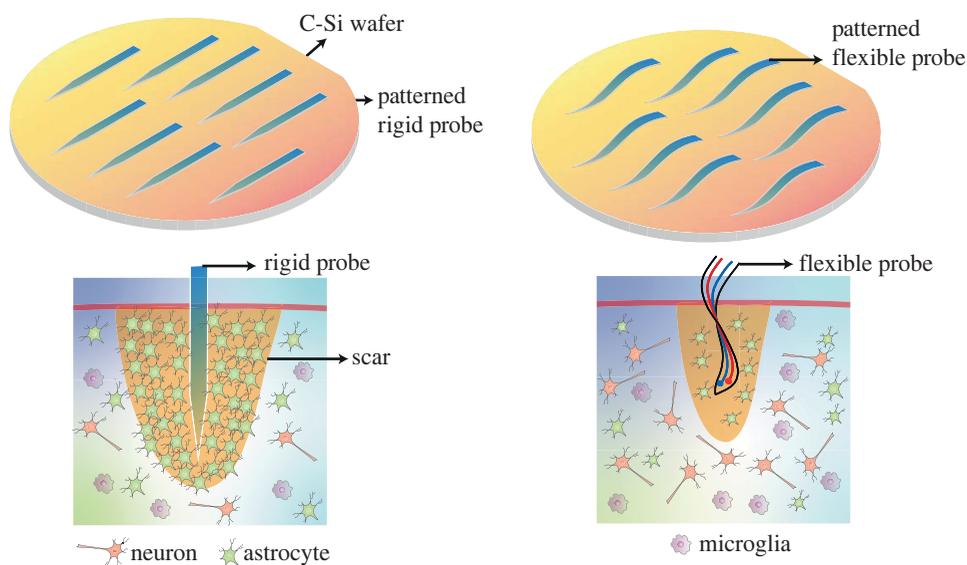


Figure 2. Illustration of the difference in immune responses when traditional rigid probes are used for neural recording/stimulation versus flexible probes. The rigid probes do not conform well with inevitable changes in structure of brain tissue which leads to inflammation and an immune response. (Online version in colour.)

where n is the refractive index of the medium, θ is the extreme angle from the objective lens to the sample. $n \sin \theta$ is often exchanged for numerical aperture (NA), a useful parameter for describing lenses. It is overcome by using *phase-shift masks*, which unlike conventional masks that simply block or transmit light in a given pattern, take advantage of the destructive interference between neighbouring light spots with a phase delay of approximately π . Figure 1 shows how a phase-shift

Table 1. Comparison between the use of traditional rigid materials like crystalline silicon versus flexible polymer-based materials as substrates for electronic neural probes.

	C-Si	flexible substrate
surface roughness	nanometre range [12]	roughness in nm range [13]
electronic properties	dielectric constant 11.7	variable dielectric constant e.g. 2.44–2.81 [14]
foreign body response	astrocyte activation, glial scarring [15]	reduced or negligible FBR with less neuronal death [16]
blood-brain barrier damage	significant acute inflammation [17]	reduced after 8 weeks of insertion [11]
Young's Modulus	169 GPa [18]	3.2 GPa [3,19]
expected buckling force	2.9 mN [19]	0.25–1.25 mN [20]
typical probe thickness	20 μm [21]	15 μm [22]

mask can produce light patterns on the substrate with smaller features than could be produced with a conventional mask.

As such, this paper will detail strategies for overcoming some of the critical issues holding back this field, which has enormous potential for helping produce long-term low-invasiveness. These biocompatible probes could improve the quality of life for people who suffer from neurological disorders.

2. Material choice

Before fabrication can begin, a substrate material must be chosen, keeping several parameters in mind. Firstly, substrate materials that have an existing body of research behind them in micro and nanofabrication and/or are commercially deployed are an excellent place to begin, including materials such as Parylene C, polyimides, SU-8 and PDMS. Certain polyimides and SU-8 are photo-definable, which can simplify the process steps or reduce them in number—we will come back to this later. For implantable neural probes, the mechanical properties such as Young's modulus of the material must be as close to that of brain tissue as possible (the order of kPa), but not so flexible (less than the order of GPa) that they cannot pierce the tissue or buckle during an attempt at insertion [25]. This conundrum is challenging to solve with material choice alone (Young's modulus of typical flexible substrates is in the single GPa range [3]), so water-soluble stiffeners such as dextran [26] and sucrose [19] are often used during insertion so that the most flexible materials may be implanted successfully without probe damage. The stiffener will then dissolve, often with a timescale that can be controlled with coating thickness or the molecular weight of polymers like dextran [26]. Furthermore, it is essential to make sure the chosen material is magnetic resonance imaging (MRI) compatible. This can be done by avoiding any ferromagnetic materials and using materials (e.g. gold) that have a similar magnetic susceptibility to that of the brain [27].

Most substrates that are used in the semiconductor industry like high-quality crystalline silicon or sapphire require energy-intensive and time-consuming production methods like the Czoralski, edge-freeze or Kyropoulos techniques, followed by lengthy and precise cutting and polishing. Flexible substrates on the other hand are solution processible, which means they can be dissolved in a solvent mixture, spin-coated for a precise film thickness, then baked and cured in a matter of minutes or hours. Spin coating is routinely used in the semiconductor industry to rapidly lay down high quality homogenous layers of solvent processable materials like resists that are commonly 0.1–10 μm thick after baking [28]. To produce approximately 100 μm thick layers for stable tissue implantation, more viscous resists can be used, otherwise many cycles of spinning and baking would be necessary to produce the desired thickness. It is worthwhile

considering the baking and curing temperatures of a flexible substrate. SU-8 formulations tend to ‘soft bake’ at less than 100°C and ‘hard bake’ at less than 250°C in under one hour [29,30], but certain polyimides for example require longer bakes with higher temperatures in order to drive out solvent. For example, the widely used HD4100 series of photodefinable (sensitive to UV light, so can be used for photolithography) polyimides require a ramped 375°C cure for up to 3 h to drive out all remaining N-methyl-2-pyrrolidone solvent, as well as a recommended 700°C furnace cleaning cycle [31], bringing optimal fabrication out of reach of most conventional ovens, increasing fabrication time and decreasing throughput. It should also be noted that around 50% of the layer thickness can be lost during baking due to solvent evaporation, which in turn causes stress build-up, which can lead to ruinous wrinkling in the middle of a fabrication process or bending of the final product, particularly for high-aspect ratio structures like neural probes. Four tried and tested strategies to mitigate this issue is including a stress reduction layer [32], slow ramped baking/curing [33], cycled heating and cooling during baking [30] and multiple baking steps, e.g. pre- and post-exposure [34].

It is obviously desirable for the bulk substrate to be biocompatible, but biocompatibility issues can also be addressed by the device being (mostly or entirely) coated with a thin encapsulating layer which can be chosen from a wider range of materials such as dexamethasone [35] or alginate hydrogels [36]. Removing the biocompatibility requirement of the substrate would also enable a wider choice of materials, and a focus to be on other parameters like mechanical and thermal properties.

(a) Additive versus subtractive protocols

The steps of a nano fabrication protocol may generally be classed as either additive or subtractive, although the overall process is often a combination of the two for producing multi-layered structures requiring complex techniques. As the name suggests, additive methods involve deposition of a new layer such as a polymer, passivation layer or metal. Subtractive protocols remove an existing layer, or part of a layer, typically using chemical (wet) or dry (plasma) etching. A summary of general procedures is depicted in figure 3. Many photoresists including the epoxy-based SU-8 series (Microchem) and HD4100 polyimide series (Dupont) are photo-definable, and as a consequence, they can be processed additively with fewer steps, without the need for harsh processes like plasma etching, which require etch masks. An illustrative example of the difference is depicted in figure 2, which features the typical process steps that are required for producing metal patterns on a patterned photo-definable or non-photo-definable polyimide substrate. The benefits and drawbacks of these contrasting techniques will be discussed herein with regard to producing electronic circuits on miniaturized flexible substrates. A specific example, comparing photo-definable and non-photo-definable polyimides, is provided alongside more general approaches for other polymer substrates such as Parylene C or polydimethylsiloxane (PDMS).

(b) Polymer deposition

Thin polyimide films may be produced by spin-coating poly (amid acid) precursor onto a clean substrate, generally silicon or glass. Spin-speed curves for commercial precursors are well-documented; however, when the viscosity of the liquid polyimide is known, the theoretical thickness value may be predicted with the following equation

$$h(t) = \frac{h_0}{\sqrt{1 + 4(\rho\omega^2/3\eta)h_0^2t}}, \quad (2.1)$$

from [37]. The initial thickness at time $t = 0$ is h_0 , while the fluid density ρ and absolute viscosity η are properties of the polymer. Controlled spin speed is denoted by ω . The final thickness $h(t)$ of the film after curing may be determined with a contact profilometer which measures the step height between the substrate and polymer film. Bubbles, contaminants in the precursor, or particles

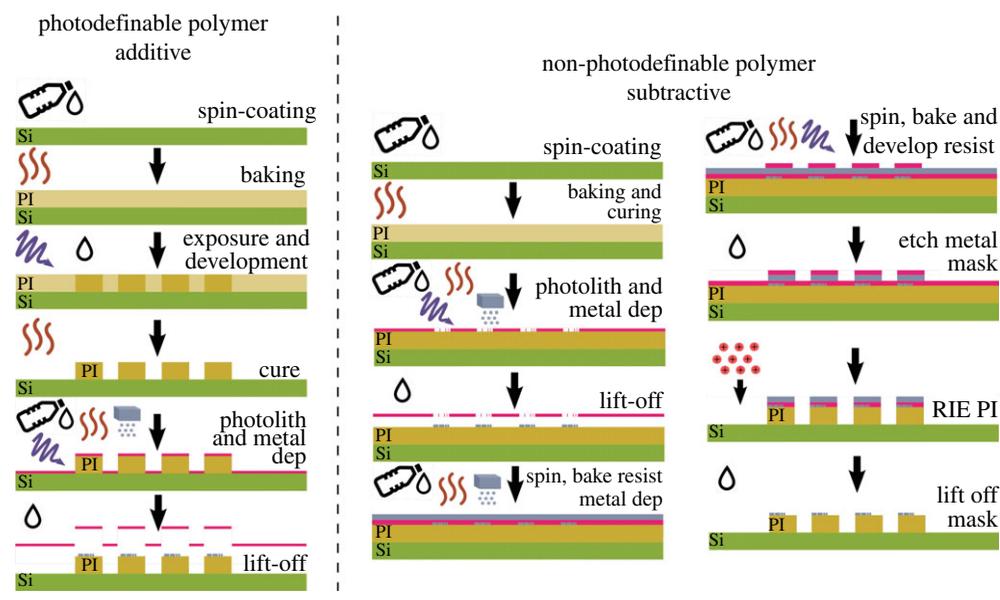


Figure 3. Schematic detailing an example of the process steps required for photolithographically producing electronic circuits on a flexible substrate. (a) Using a photodefinable polymer for the probe material typically involves spin-coating it to produce an even film, followed by baking to remove excess solvent, followed by exposure to harden (or break down if it is a positive rather than negative type) the pattern. This may need to be repeated multiple times depending on the desired substrate thickness. It is then normally cured at high temperature to remove the remaining solvent and if needed, complete chemical reactions, e.g. the imidization of polyimides. A second photolithographic step can then be carried out to produce the pattern for the metal pads/tracks/electrodes, followed by metal deposition via sputtering/vapour deposition and lift-off. (b) Using non-photodefinable polymers involves carrying out similar processes, but the undesirable polymer is removed via an etching process like ‘dry’ reaction ion etching (pictured), or ‘wet’ etching using strong base solutions. The harsh etching process requires a mask to be in place to protect the rest of the sample, which will normally be made of metal like aluminium. This then means an extra photolithographic step to produce the mask, and another step to remove it. PI = Polyimide and Si = Silicon. (Online version in colour.)

which land on the surface can cause defects in the film, generating comets during the spinning process. Despite this, in a carefully controlled clean room environment, spin-coated films will encounter fewer contaminants and typically have reduced surface roughness compared to pre-prepared commercial films [13]. Edge bead may occur, with a ring of thick polymer around the outside of the wafer, which may be removed with a short high-speed spin at the end of the spin-coating process, or by adapting photomask designs such that only the centre portion of the film is used as a circuit substrate.

Kapton film produced by Dupont is the most famous polyimide, used to create flexible printed circuit boards (PCBs) with a copper layer on one side. Due to its weak adhesion with untreated polyimide [38], copper may be coupled with an intermediary metal layer such as titanium, chromium or aluminium.

3. Photoresist

Positive photoresists are incredibly popular as they can produce high-resolution features, with excellent thermal stability [39], and are typically developed in alkaline solutions. By contrast, negative photoresists are prone to distortion during development. Since UV exposure hardens sections of the negative photoresist, leaving unexposed areas soluble, the entire photoresist layer is vulnerable to the developer. The cross-linking which occurs during UV exposure begins from

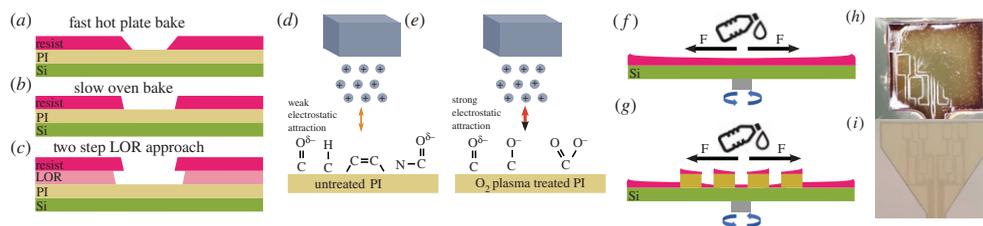


Figure 4. (a–c) Three processes options in photolithography. Hot plate baking is faster, but often produces more sloping sidewalls than an oven bake will. Metal lift-off is aided by producing a resist bilayer of the resist, plus a ‘lift-off resist’ or LOR. (d,e) example of surface bond activation for improved metal adhesion to a polyimide surface, (f,g) uneven resist profiles on thick existing structures, (h,i) comparison between using additive and subtractive processes for producing metal electronics on polyimide probe shapes respectively - (h) has a highly uneven resist profile due as it suffers from the issue shown in (g). (Online version in colour.)

the surface of the photoresist down to the substrate, which means that prolonged exposure is required to harden the resist fully, increasing the possibility of scattered UV radiation and compromising the pattern resolution [40].

In any case, the baking times of the resist should be closely controlled to prevent damage to the layer. Cracking or delamination of the photoresist will be detrimental to the final pattern regardless of whether the photoresist is used as an etch mask, or a lift-off layer [41]. Bilayers that incorporate a lift-off resist (LOR) underneath the top photoresist layer are useful to produce an undercut (figure 4c) which encourages clean metal features. The sidewalls of the resist layer can be sloped if the temperature and bake time is not fully optimized, which means the resist stripper will not be able to effectively dissolve the photoresist protected by the metal. An undercut produced by LOR prevents the metal layer from creating a seal over the whole surface of the wafer. Novel etching methods, employing photoresist as an etch mask, use sloped resist sidewalls to control the etch profile of lower layers [42]. Particular care must be given to photoresist spinning on patterned substrates, as depicted in figure 4f. The topology of flexible substrates, combining inherent surface roughness with etched/UV-defined probe shapes, may produce uneven resist profiles, further complicating the photolithography process. The order of process steps is equally as important as the success of each individual process.

4. Polymer patterning

The additive approach of polymer patterning recruits a photo-definable polyimide which may be simply patterned with a UV exposure step before development removes the unwanted polymer. An in-depth review of the topic is provided in Chapter 5 of [43], detailing the synthesis methods of photosensitive polyimides. A popular option is the HD-4100 series from HD Microsystems, which is negative in tone [44–47]. After UV exposure the polyimide is developed in cyclopentanone and rinsed in propylene glycol methyl ether acetate (PGMEA) at room temperature. Compared to positive tone photoresists, the negative polyimide requires a long exposure time on the order of several minutes, which must be tuned based on the polyimide thickness and feature size. Increased exposure time will ensure the adhesion of small features on the substrate. During development, the soluble polyimide forms a white milky substance before it can be rinsed away, which aids the researcher in determining the reaction end point. Negative tone polyimides may be sensitized through one of the following compositions: ester bonds, ionic bonds, acrylic monomers or photosensitizers such as naphthoquinonediazide, among others. A full discussion of the chemistry is provided in Chapter 5 of [43].

Prior to curing, certain polyimides such as PI-2545 from HD Microsystems may be wet etched in alkaline developer using photoresist as an etch mask. By contrast, after full curing of a

polyimide film, it is invulnerable to most solvents, requiring aggressive stripping techniques such as 49% hydrofluoric acid or hot sulphuric acid to remove the polymer from a silicon wafer (PI2545 Product Bulletin from HDMS).

For decades, oxygen plasma has been used to ablate polyimide layers in a reactive ion etch (RIE) process [48,49]. The etch rate may be increased with the inclusion of fluorine-containing gases such as CF_4 and SF_6 [50], which boost the concentration of oxygen atoms in the plasma as the etch gases react [51]. Fluorine is added to saturated carbon groups in the polyimide, breaking double carbon–carbon bonds after which point the oxygen atoms break the polymer chain [52], etching the polyimide from the surface. Hard etch masks are required for this dry etch process, as thin photoresist layers lack the etch selectivity required to allow the polyimide layer to be etched before the mask itself is etched away completely. Examples of etch mask materials include aluminium [53], chromium [54], titanium [50], nickel [55] and gold [56], although in some cases thick photoresist may also be used.

(a) Metal deposition

Lift-off is the primary photolithographic method for metal patterning. Photoresist coats the entire sample, and then through UV patterning and development, is removed in the areas intended to be metallized. When a layer of metal is evaporated or sputtered across the whole wafer, it can only make contact with the substrate in the areas the photoresist is not. As described in the previous section, the resist stripping step is not infallible. If the photoresist pattern is imperfect, under- or over-developed, then it is possible the metal will not adhere to the surface or remain in unwanted areas. This is particularly challenging with polymer substrates, as their surface roughness introduces uneven resist profiles. For many metals, the adhesion to polyimide is very poor, and the surface requires plasma treatment to increase its roughness in preparation for metal deposition [57], depicted in figure 4*d,e*. For additive style processes that are depicted in figure 3, it may be the case that the probe shape is defined first, making the thickness of the probe an order of magnitude or two greater than the thickness of any subsequent resist coatings. This presents a problem for obtaining even resist profiles, as the path of the resist away from the centre of the sample will likely be impeded by the probe structure. An experimental example of this issue is depicted in figure 4*f–i*. Resist thickness varies across the probe shape in figure 4*h*, leading to incorrect exposure doses, followed by simultaneous incomplete and overdevelopment of the resist in different parts of the probe. In this sense, a subtractive process may be advantageous where the probe shape is etched away later, allowing the higher resolution metal patterns to be put down on a flat surface figure 5.

Alternatively, photoresist may be used as an etch mask for a metal layer that covers the entire surface of the wafer in a subtractive process. Much in the way a hard mask protects the underlay during dry etching, the photoresist prevents a liquid etchant from attacking the metal on the polyimide surface, while the uncovered metal is etched away.

The substrate/polyimide interface determines the suitability of wet etching in this instance. When polyimide is spun on glass, it may be easily removed by cutting and peeling [58] or peeling after more than 2 h soaking in de-ionized water. However, when spun on silicon, a release or sacrificial layer such as aluminium [45] is generally employed such that after the final fabrication step, the electronics may be removed from their carrier wafer. Wet etchants, which are acidic solutions, can delaminate polyimide from the glass within a few minutes. On the other hand, if the signal metal layer and sacrificial layer are the same, or can be etched with the same acids, then the probes will delaminate during the metal patterning etch step.

(b) Heterogeneous bonding to flexible substrates

The integration of soft neural probes with rigid electronic components, for example, PCBs, is a key step in the overall functionalization of brain implantable devices since within these PCBs we

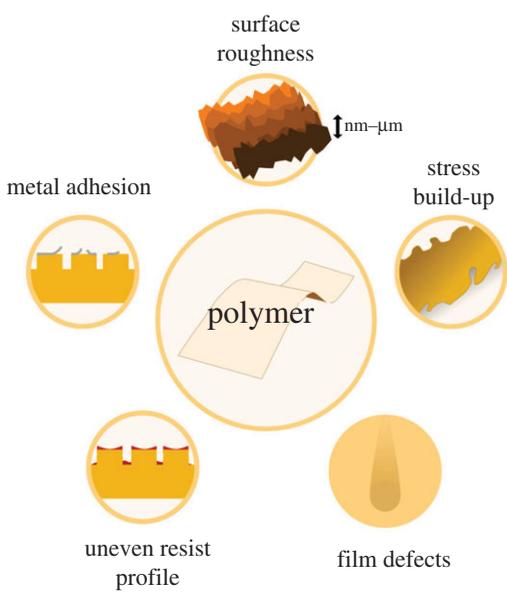


Figure 5. Visual summary of the challenges faced when fabricating electronic probes on flexible polymer substrates in a cleanroom setting using photolithography. (Online version in colour.)

can find essential components, ranging from capacitors to memristors, that allow the neural probe to work according to the function desired.

Wirebonding is a common and cost-effective option but is limited in that the minimum wire size of a typical commercially available laboratory wirebonder is 10–20 μm . Wires are generally bonded protruding at a high angle to the plane of the substrate and then encapsulated, limiting how thin the device can be. Wedge bonds offer a lower profile alternative to perpendicular ‘ball-bonded’ wires.

A study by Stieglitz *et al.* [59], however, presented a variation of the wire bonding technique called the ‘Microflex Interconnection Technique’ that allowed three-dimensional interconnects with biocompatible flexible substrates, something of great interest for neural probe integration research. Nonetheless, the small surface that is dealt with in neural probe research, as well as durability concerns, might still be an impediment when using this technique. One way to increase the durability of wire bonding is to encapsulate the wires with non-conductive epoxy.

Conductive epoxy mixtures which contain metallic elements have also been studied by various groups to create interconnections [23,58,60]. A comprehensive study by Yoo & Meng [61] showed that conductive epoxy-bonded interconnections between rigid and soft polymer samples demonstrated the greatest yield strength of the five studied methods, which included wire and bump bonds. A recent study published by Asad *et al.* [62] describes a novel method of ‘pasting and cutting’ GaN μLEDs from a sapphire substrate onto a flexible one using a laser. They carried out a two-step method consisting of first bonding the sapphire substrate containing the μLEDs onto a carrier substrate through spin-coating an adhesive layer that would be removed later through dry-etching, and then applying a laser to lift the μLEDs off the sapphire. The μLEDs were then coated with a conductive layer, flipped and bonded onto the flexible substrate, with the carrier substrate being released. The optoelectronic properties of the μLEDs were unaffected by the transfer process. The method has applications in fabricating optogenetic probes but is yet to be put into practice. One innovative technique was introduced recently in the previously mentioned study conducted by Yoo & Meng [61]. This bonding method called polymer ultrasonic on bump or PUB entails a pre-treatment of the rigid chip with a gold bump, then alignment and finally compression through ultrasonic force, which would finalize the bonding of the rigid chip to the

soft substrate, in this case Parylene. The authors demonstrated that compared to other bonding methods, such as wire bonding and epoxy, PUB interconnections showed better performance in terms of electrical parameters, with very low resistance being exhibited in the bonds. It should be noted that these bonds did not perform as well as other bonding methods such as wire bonding when subjected to cycled mechanical tests and pull testing [61].

Overall, integrating a rigid chip with a soft substrate is a crucial step in the fabrication of neural probes and should be carefully studied. Depending on the circumstances of the research, one could argue that wire bonding might be the best method to use for preliminary studies because of its simplicity and cost-effectiveness. Nonetheless, for more advanced stages where *in vivo* implantation is being considered and biocompatibility is essential, other methods such as medical-grade epoxy encapsulation might be considered given that they have been widely studied and offer very adequate results both mechanically and electrically. In the coming years, more research will be conducted on more recently presented methods like laser and PUB, which are showing very promising results and should not be disregarded.

5. Chip thinning methods

An additional fundamental step in the fabrication of neural probes is the thinning of the electronic components. When dealing with brain tissue, it is incumbent to obtain good integration between the neural probe and said surrounding tissue. This is achieved through various steps previously mentioned, such as the material selection and the bonding of the soft substrate with the rigid electronic components that control the neural probe. Nonetheless, there is an additional challenge in this case, and that is the size and flexibility of said electronic components. Research has been conducted to produce miniaturized components on silicon chips, among other materials, but the rigidity of silicon chips remains an obstacle. This is where chip thinning comes into place.

Chip thinning methods were first described within the aerospace sector back in the 1960s, during the space race, where a study was published regarding the use of thin silicon wafers for solar cells [63]. However, it has not been until the last three decades that there has been a clear increase of interest within the literature for flexible, high-performance electronics, achieved through chip thinning techniques. In an extensive review presented by Gupta *et al.* [64], the most prominent, as well as more novel methods of chip thinning were described. Based on this, the more relevant methods for neural probe fabrication, all based on silicon wafers, were identified and are presented as follows.

The first method and perhaps the most well-established one would be that of back grinding. This technique consists of a coarse-grinding step, followed by a fine-grinding one, done on the non-active back of the chip by a grinding wheel. The chip is stuck in place by an adhesive tape, which as mentioned in [64] has an effect on the total thickness variation. This technique has the advantage of being cost-effective, very rapid and has been shown to achieve very fine thicknesses of down to 3 μm [65], although it can cause some damage to the chip in the form of warping and breakage during manipulation of the chip. Some could also argue that given that neural probes are very delicate structures, such a technique should not be considered. However, if one were to perform chip thinning before the integration step of the soft substrate with the more rigid electronics, the risk of damage to the neural probe could be attenuated. In fact, a study performed by Sacher *et al.* [66] demonstrated that back grinding could be a suitable chip thinning method for photonic neural probes with a thickness ranging from 50–92 μm . In addition to this, there have been techniques explored to reduce mechanical damage to the chips caused by back grinding, such as the one explored by Morcom *et al.* [67], known as taiko, where grinding is not performed on the periphery of the back, non-active side of the wafer, leaving a ring structure that enhances the structural integrity of the wafer.

The second method has been gaining more interest within the literature in recent years. It is the process of chip thinning through etching, which can be done in two ways: dry etching or wet etching. In terms of dry etching, there are different types, mainly RIE, deep reactive ion etching (DRIE) and physical ion etching (PIE). The first two types use plasma to chemically

remove material, in this case, a layer of wafer or substrate, whereas PIE, as its name indicates, physically removes said layer using high energy beams of ions, photons or electrons [68]. There is a tendency for research groups investigating the fabrication of neural probes to use DRIE for thinning processes [21,69], hence for the purpose of this paper, the main focus was on this technique. The main advantage that using this technique provides instead of using others such as back grinding is the fact that it is not as physically aggressive and hence, in terms of the structural integrity of the wafer, the probability of it being compromised is extremely low. In addition, this technique has been proven to work for a variety of thicknesses, even going down to 2 μm in neural probes [69], which makes it incredibly versatile, while still maintaining good mechanical properties. However, it is safe to note that it is a more expensive, complex and long process and that there is a chance of contamination, so it should be taken into account during the selection process, in particular during prototyping and initial experimental stages of chip thinning.

On the other hand, there is wet etching, which has been described in [64] as a technique that requires both pre- and post-processing, unlike the two other techniques already described. The methodology would be as follows: first deposit a mask layer on the back side of the wafer, process the front side and then etch the back side. The advantages of using such a technique would be that, firstly, it is a well-established technique, with studies being done on neural probes as early as 1997 [70], meaning that there is substantial literature to compare to when performing experiments. Moreover, as reported in the literature, low thicknesses of approximately 15 μm have been achieved by Dahiya *et al.* [71] in flexible substrates using tetramethylammonium hydroxide (TMAH) as the etchant, demonstrating its potential for translation to neural probe scenarios, where low thicknesses are desirable. However, one should note that this technique also poses some challenges such as the fact the wafer could be too sensitive to the etchant concentration [72].

Furthermore, in more recent years, more research studies have been published on other methods of chip thinning such as layer transfer methods and epitaxial-based wafers, which will be briefly introduced. The former set includes methods such as proton-induced exfoliation which uses a beam of hydrogen ions to, as its name suggests, exfoliate a layer of the wafer when they are heated. This method, however, has been deemed unsuitable currently because it causes too much damage to the electronic components [64,73]. The latter method of epitaxial-based wafers includes techniques such as the one created by ChipFilm Technology [74] which entails the use of two porous layers, each of a different porosity, between the silicon epitaxial layer and the substrate. By lifting off the epitaxial layer, thinning is achieved. With this method, thicknesses of down to 15 μm have been obtained, as shown in [75]. However, warpage has been reported [76] and there are no studies found by the authors done on neural probes currently, so more research should be conducted on this method.

The process of chip thinning is a crucial one in the fabrication of neural probes, hence the selection of the methodology to follow for such a step must be carefully considered. It is undeniable that the process of back grinding is the simplest, most cost-effective and could prove most useful during initial stages of experimental testing. However, when carefully examining the literature one can see that different processes should be tested according to the application and the geometry of the neural probe. Dry etching seems to be the process that offers the greatest amount of thinning without compromising the integrity of the mechanical or electrical structure as much as the other methods, hence why most research groups perhaps tend to gravitate toward using this technique over the others.

6. Future perspective

Truly single nanometre scale devices such as transistors are routinely fabricated on a very large scale in state-of-the-art foundries and are present in the central processing units, memory and other components of devices such as smartphones all over the world. The technique behind this is of course photolithography, which has stretched the limits of the Rayleigh criterion (equation (1.1)). Computational photolithography methods such as phase-shift photomasks and optical proximity correction [77] take advantage of diffraction to go smaller than the criterion would

suggest. This staggering miniaturization has been possible in part due to the almost atomic flatness, crystallinity and purity of substrates like silicon, gallium arsenide, sapphire and others. In this aspect, polymer films will never be able to quite reach the same limits due to a lack of crystallinity, the larger size of the polymer fibres and movement of the fibres during flexing. There is still however—to quote the now cliché from Richard Feynman—plenty of room at the bottom [78]. The fact that a technique as simple as spin-coating can be used to produce homogeneous films with values of rms surface roughness of less than 1 nm [53] bodes well for further miniaturization into the nano-regime. The solution processability means that very large-scale integration (VSLI) is possible if applications are widely adopted. Providing that whatever flexing required is consistent, the design, materials and fabrication protocols can be optimized appropriately, allowing for further miniaturization. Although this work has focussed on metals—as their high conductivity lends itself well to micro- and nanoscale electronics—modern conductive polymers which can flex with the substrate may have a role to play instead but must have low enough impedance for devices to be efficient and prevent heating and device or tissue damage [4].

Integration with external components such as power sources, resistors, transistors, diodes and so on is perhaps the greatest challenge due to the mismatch between properties, and their size. There is however progress with miniaturization and increasing efficiency of electronics devices such as μ LEDs [79], which will be crucial for converting optogenetics from a tool for in-vivo animal neuroscience studies into a common medical treatment.

7. Conclusion

In this work, cleanroom-based strategies for overcoming some of the key issues holding back photolithographic fabrication of neural probes on flexible substrates have been described. This includes additive versus subtractive protocols, metal adhesion, uneven spin-coated films, surface roughness and inhomogeneity. Based on current technology, it is unlikely that flexible electronics will ever be fabricated with the resolution and high-density that is now the standard in the semiconductor industry for rigid substrates, for reasons that we have laid out. There is however still a lot of scope for improvement and miniaturisation using innovative improvements in photolithography and associated cleanroom processes.

Data accessibility. This article has no supporting data.

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References

1. Feigin VL, Nichols E, Alam T, Bannick MS, Beghi E, Blake N, Fischer F. 2019 Global, regional, and national burden of neurological disorders, 1990–2016: a systematic

- analysis for the Global Burden of Disease Study 2016. *Lancet Neurol.* **18**, 459–480. (doi:10.1016/S1474-4422(18)30499-X)
2. Yang X, McGlynn E, Das R, Paşca SP, Cui B, Heidari H. 2021 Nanotechnology enables novel modalities for neuromodulation. *Adv. Mater.* **33**, 1–29.
 3. Das R, Moradi F, Heidari H. 2020 Biointegrated and Wirelessly powered implantable brain devices: a review. *IEEE Trans. Biomed. Circuits Syst.* **14**, 343–358. (doi:10.1109/TBCAS.2020.2966920)
 4. McGlynn E, Nabaei V, Ren E, Galeote-Checa G, Das R, Curia G, Heidari H. 2021 The future of neuroscience: flexible and wireless implantable neural electronics. *Adv. Sci.* **8**, 2002693, 1–33. (doi:10.1002/advs.202002693)
 5. Walton F, McGlynn E, Das R, Zhong H, Heidari H, Degenaar P. 2021 Magneto-optogenetic deep brain multimodal neurostimulation. *Adv. Intell. Syst.* **4**, 2100082. (doi:10.1002/aisy.202100082)
 6. Musk E. 2019 An integrated brain-machine interface platform with thousands of channels. *J. Med. Internet Res.* **21**, e16194. (doi:10.2196/16194)
 7. Maynard EM, Nordhausen CT, Normann RA. 1997 The Utah intracortical electrode array: a recording structure for potential brain-computer interfaces. *Electroencephalogr. Clin. Neurophysiol.* **102**, 228–239. (doi:10.1016/S0013-4694(96)95176-0)
 8. Desai SA, Gutekunst CA, Potter SM, Gross RE. 2014 Deep brain stimulation macroelectrodes compared to multiple microelectrodes in rat hippocampus. *Front. Neuroeng.* **7**, 1–8.
 9. Gulino M, Kim D, Pané S, Santos SD, Pêgo AP. 2019 Tissue response to neural implants: the use of model systems toward new design solutions of implantable microelectrodes. *Front. Neurosci.* **13**, 1–24. (doi:10.3389/fnins.2019.00689)
 10. Bjerknes S, Skogseid IM, Sæhle T, Dietrichs E, Toft M. 2014 Surgical site infections after deep brain stimulation surgery: frequency, characteristics and management in a 10-year period. *PLoS ONE* **9**, e0105288. (doi:10.1371/journal.pone.0105288)
 11. Du ZJ, Kolarcik CL, Kozai TDY, Luebben SD, Sapp SA, Zheng XS, Cui XT. 2017 Ultrasoft microwire neural electrodes improve chronic tissue integration. *Acta Biomater.* **53**, 46–58. (doi:10.1016/j.actbio.2017.02.010)
 12. Khan SP, Auner GG, Newaz GM. 2005 Influence of nanoscale surface roughness on neural cell attachment on silicon. *Nanomedicine nanotechnology. Biol. Med.* **1**, 125–129.
 13. Liu F, Christou A, Dahiya R. 2019 3D integrated electronics with layer by layer printing of NWs. In *IEEE International Conference on Flexible and Printable Sensors and Systems*, pp. 2019. Glasgow, UK: FLEPS.
 14. Bei R, Qian C, Zhang Y, Chi Z, Liu S, Chen X, Aldred MP. 2017 Intrinsic low dielectric constant polyimides: relationship between molecular structure and dielectric properties. *J. Mater. Chem. C* **5**, 12807–12815. (doi:10.1039/C7TC04220E)
 15. Lee HC, Gaire J, Currlin SW, Mcdermott MD, Park K, Otto KJ. 2017 Foreign body response to intracortical microelectrodes is not altered with dip-coating of polyethylene glycol (PEG). *Front. Neurosci.* **11**, 1–11.
 16. Dai X, Hong G, Gao T, Lieber CM. 2018 Mesh nanoelectronics: seamless integration of electronics with tissues. *Acc. Chem. Res.* **51**, 309–318. (doi:10.1021/acs.accounts.7b00547)
 17. Bennett C, Samikkannu M, Mohammed F, Dietrich WD, Rajguru SM, Prasad A. 2018 Blood brain barrier (BBB)-disruption in intracortical silicon microelectrode implants. *Biomaterials* **164**, 1–10. (doi:10.1016/j.biomaterials.2018.02.036)
 18. Hopcroft MA, Nix WD, Kenny TW. 2010 What is the Young's Modulus of silicon? *J. Microelectromechanical Syst.* **19**, 229–238. (doi:10.1109/JMEMS.2009.2039697)
 19. Jeon M, Cho J, Kim YK, Jung D, Yoon ES, Shin S, Cho IJ. 2014 Partially flexible MEMS neural probe composed of polyimide and sucrose gel for reducing brain damage during and after implantation. *J. Micromech. Microengin.* **24**, 025010. (doi:10.1088/0960-1317/24/2/025010)
 20. Rezaei S, Xu Y, Id SWP. 2019 Control of neural probe shank flexibility by fluidic pressure in embedded microchannel using PDMS / PI hybrid substrate. *PLoS ONE* **14**, e0220258. (doi:10.1371/journal.pone.0220258)
 21. Schander A, Stemmann H, Tolstosheeva E, Roese R, Biefeld V, Kempen L. 2016 Design and fabrication of novel multi-channel floating neural probes for intracortical chronic recording. *Sens. Actuators A: Phys.* **247**, 125–135. (doi:10.1016/j.sna.2016.05.034)

22. Soscia DA, Lam D, Tooker AC, Enright HA, Triplett M, Karande P, Fischer NO. 2020 A flexible 3-dimensional microelectrode array for in vitro brain models. *Lab. Chip.* **20**, 901–911. (doi:10.1039/C9LC01148J)
23. Ji B, Wang M, Kang X, Gu X, Li C, Yang B. 2017 Flexible optoelectric neural interface integrated wire-bonding μ LEDs and microelectrocorticography for optogenetics. *IEEE Trans. Electron Devices.* **64**, 2008–2015. (doi:10.1109/TED.2016.2645860)
24. Waldrop MM. 2016 More than Moore. *Nature* **530**, 144–147. (doi:10.1038/530144a)
25. Nabaei V, Panuccio G, Heidari H. 2020 Neural Microprobe Device Modelling for Implant Micromotions Failure Mitigation. In *2020 IEEE international symposium on circuits and systems (ISCAS)*, pp. 1–5. New York, NY: IEEE.
26. Kil D, Carmona MB, Ceysens F, Deprez M, Brancato L, Nuttin B, Puers R. 2019 Dextran as a resorbable coating material for flexible neural probes. *Micromachines* **10**, 61.
27. Das R, Heidari H. 2021 Biointegrated implantable brain devices. In *Engineering and technology for healthcare*, pp. 81–93. Chichester, UK: Wiley Online Books.
28. Dentinger PM, Cardinale GF, Henderson CC, Fisher A, Ray-Chaudhuri AK. 2000 Photoresist film thickness for extreme ultraviolet lithography. In *Proceedings of SPIE*. Santa Clara, CA: SPIE.
29. Altuna A, Menendez de la Prida L, Bellistri E, Gabriel G, Guimerá A, Berganzo J, Fernández LJ. 2012 SU-8 based microprobes with integrated planar electrodes for enhanced neural depth recording. *Biosens. Bioelectron.* **37**, 1–5. (doi:10.1016/j.bios.2012.03.039)
30. Microchem. SU-8 2000 Permanent Epoxy Photoresist Processing Guidelines [Internet]. 2025, 2035, 2050, 2075. 2006. See papers3://publication/uuid/E7A575F7-4BEF-4981-8E02-277673CABC12.
31. HD Microsystems GmbH. 2009 Product Bulletin HD-4100 Series.
32. Luo C, Govindaraju A, Garra J, Schneider T, White R, Currie J, Paranjape M. 2004 Releasing SU-8 structures using polystyrene as a sacrificial material. *Sens. Actuators A: Phys.* **114**, 123–128. (doi:10.1016/j.sna.2004.02.042)
33. Guo L, DeWeerth SP. 2010 An effective lift-off method for patterning high-density gold interconnects on an elastomeric substrate. *Small* **6**, 2847–2852. (doi:10.1002/smll.201001456)
34. Li B, Liu M, Chen Q. 2005 Low-stress ultra-thick SU-8 UV photolithography process for MEMS. *J Micro/Nanolithography, MEMS. MOEMS* **4**, 043008, 1–6. (doi:10.1117/1.2117108)
35. Zhong Y, Bellamkonda RV. 2007 Dexamethasone-coated neural probes elicit attenuated inflammatory response and neuronal loss compared to uncoated neural probes. *Brain Res.* **1148**, 15–27. (doi:10.1016/j.brainres.2007.02.024)
36. Park S, Yuk H, Zhao R, Yim YS, Woldegebriel EW, Kang J, Anikeeva P. 2021 Adaptive and multifunctional hydrogel hybrid probes for long-term sensing and modulation of neural activity. *Nat. Commun.* **12**, 1–12. (doi:10.1038/s41467-020-20314-w)
37. Tyona MD. 2013 A theoretical study on spin coating technique. *Adv. Mater. Res.* **2**, 195–208. (doi:10.12989/amr.2013.2.4.195)
38. Koo S-B, Lee C-M, Kwon S-J, Jeon J-M, Hur J, Lee H-K. 2019 Study on aging effect of adhesion strength between polyimide film and copper layer. *Met. Mater. Int.* **25**, 117–126. (doi:10.1007/s12540-018-0167-7)
39. Quero JM, Perdigonos F, Aracil C. 2018 11 - Microfabrication technologies used for creating smart devices for industrial applications. In *Woodhead publishing series in electronic and optical materials* (eds S Nihtianov, ABT-SS Luque, E Second, Mem), pp. 291–311. Sawston, UK: Woodhead Publishing. See <https://www.sciencedirect.com/science/article/pii/B9780081020555000115>.
40. Madou MJ. 2011 *Fundamentals of microfabrication and nanotechnology*, 3rd edn. Boca Raton, FL: CRC Press.
41. Kumar N, Jat RK, Kumar P, Saini HK, Lata S, Chaubey RK, Laishram R, Agarwal VR, Rawal DS. 2019 Thermal Control of Stress in Photoresist Film for Improving Selectivity in Electro-Plating Process. In *2017: the physics of semiconductor devices* (eds RK Sharma, DS Rawal, IWPSD), pp. 269–272. Cham, Switzerland: Springer International Publishing.
42. Buyong MR, Larki F, Takamura Y, Majlis BY. 2017 Tapered microelectrode array system for dielectrophoretically filtration: fabrication, characterization, and simulation study. *J Micro/Nanolithography, MEMS. MOEMS* **16**, 044501.

43. Ghosh M. 1996 *Polyimides: fundamentals and applications*, 1st edn. Boca Raton, FL: CRC Press.
44. Tsang WM, Stone AL, Aldworth ZN, Hildebrand JG, Daniel TL, Akinwande AI, Voldman J. 2010 Flexible split-ring electrode for insect flight biasing using multisite neural stimulation. *IEEE Trans. Biomed. Eng.* **57**, 1757–1764. (doi:10.1109/TBME.2010.2041778)
45. Xiang Z, Yen S-C, Xue N, Sun T, Tsang WM, Zhang S, Lee C. 2014 Ultra-thin flexible polyimide neural probe embedded in a dissolvable maltose-coated microneedle. *J. Micromech. Microeng.* **24**, 65015. (doi:10.1088/0960-1317/24/6/065015)
46. Grady ME, Geubelle PH, Sottos NR. 2014 Interfacial adhesion of photodefinable polyimide films on passivated silicon. *Thin Solid Films* **552**, 116–123. (doi:10.1016/j.tsf.2013.11.085)
47. Cao H, Li A, Nguyen CM, Peng Y, Chiao J. 2012 An integrated flexible implantable micro-probe for sensing neurotransmitters. *IEEE Sens J.* **12**, 1618–1624. (doi:10.1109/JSEN.2011.2173674)
48. You A, Be MAY, In I. 2002 Optimized oxygen plasma etching of polyimide films for low loss optical waveguides. *J. Vac. Sci. Technol.* **20**, 1587. (doi:10.1116/1.1494816)
49. You A, Be MAY, In I. 2011 Oxygen plasma etching of thick polymer layers;743(June 1998).
50. Zhang L, Liu Y, Li Z, Wang W. 2018 SF₆ optimized O₂ plasma etching of parylene C. *Micromachine* **9**, 162. (doi:10.3390/mi9040162)
51. Egitto FD. 1990 Plasma etching and modification of organic polymers. *Pure Appl. Chem.* **62**, 1699–1708. (doi:10.1351/pac199062091699)
52. Cain SR, Egitto FD, Emmi F. 1987 Relation of polymer structure to plasma etching behaviour: Role of atomic fluorine. *J. Vac. Sci. Technol., A* **5**, 1578–1584. (doi:10.1116/1.574568)
53. Joshi S, Savov A, Shafqat S, Dekker R. 2018 Investigation of ‘fur-like’ residues post dry etching of polyimide using aluminum hard etch mask. *Mater. Sci. Semicond. Process* **75**, 130–135. (doi:10.1016/j.mssp.2017.11.025)
54. Westerhausen M *et al.* 2020 Passivated electrode side walls by atomic layer deposition on flexible polyimide based samples. *Microelectron. Eng.* **227**, 111315. (doi:10.1016/j.mee.2020.111315)
55. Lecomte A *et al.* 2017 Deep plasma etching of Parylene C patterns for biomedical applications. *Microelectron. Eng.* **177**, 70–73. (doi:10.1016/j.mee.2017.02.012)
56. Arevalo A, Byas E, Conchouso D, Castro D, Ilyas S, Foulds IG. 2015 A Versatile Multi-User Polyimide Surface Micromachining Process for MEMS Applications. In *Proceedings of the 10th IEEE Int. Conf. on Nano/Micro Engineered and Molecular Systems*, pp. 561–565. New York, NY: IEEE.
57. Cen-puc M, Schander A, Gleason MGV, Lang W. 2021 An assessment of surface treatments for adhesion of polyimide thin films. *Polymers (Basel)* **13**, 1955. (doi:10.3390/polym13121955)
58. Chang JHC, Huang R, Tai YC. 2011 *High-density IC chip integration with parylene pocket*. In *NEMS 2011 - 6th IEEE Int. Conf. Nano/Micro Eng Mol Syst*, pp. 1067–1070. New York, NY: IEEE.
59. Stieglitz T, Beutel H, Meyer JU. 2000 ‘Microflex’ - A new assembling technique for interconnects. *J. Intell. Mater. Syst. Struct.* **11**, 417–425.
60. Szostak KM, Grand L, Constandinou TG. 2017 Neural interfaces for intracortical recording: requirements, fabrication methods, and characteristics. *Front. Neurosci.* **11**, 665. (doi:10.3389/fnins.2017.00665)
61. Yoo J, Meng E. 2021 Bonding methods for chip integration with Parylene devices. *J. Micromech. Microeng.* **31**, 1–17.
62. Asad M, Li Q, Sachdev M, Wong WS. 2020 Thermal and optical properties of high-density GaN micro-LED arrays on flexible substrates. *Nano Energy* **73**, 104724. (doi:10.1016/j.nanoen.2020.104724)
63. Crabb RL, Treble FC. 1967 Thin silicon solar cells for large flexible arrays. *Nature* **213**, 1223–1224. (doi:10.1038/2131223a0)
64. Gupta S, Navaraj WT, Lorenzelli L, Dahiya R. 2018 Ultra-thin chips for high-performance flexible electronics. *NPJ Flex Electron* **2**, 1–17. (doi:10.1038/s41528-018-0021-5)
65. Mizushima Y, Kim Y, Nakamura T, Uedono A, Ohba T. 2017 Microelectronic Engineering Behavior of copper contamination on backside damage for ultra-thin silicon three dimensional stacking structure. *MEE* **167**, 23–31.
66. Sacher WD *et al.* 2021 Implantable photonic neural probes for light-sheet fluorescence brain imaging. *Neurophotonics* **8**, 1–26. (doi:10.1117/1.NPh.8.2.025003)

67. Morcom WiR, Ahrens SC, Spindler JP, Ford RT, Lauffer JE. 2000 United States Patent 6,162,702. p. 3.
68. Bhushan B. 2012 *Encyclopedia of Nanotechnology*. Berlin, Germany: Springer.
69. Otte E, Cziumplik V, Ruther P, Paul O. 2020 Customized Thinning of Silicon-based Neural Probes Down to 2 μm . New York, NY: IEEE.
70. Chen J, Wise KD, Hetke JF, Bledsoe SC. 1997 A multichannel neural probe for selective chemical delivery at the cellular level. *IEEE Trans. Biomed. Eng.* **44**, 760–769. (doi:10.1109/10.605435)
71. Dahiya RS, Member S, Gennaro S. 2013 Bendable ultra-thin chips on flexible foils. *IEEE Sens. J.* **13**, 4030–4037. (doi:10.1109/JSEN.2013.2269028)
72. Wang S, Weil BD, Li Y, Wang KX, Garnett E, Fan S. 2013 Large-area free-standing ultrathin single-crystal silicon as processable materials. *Nano Lett.* **13**, 4393–4398. (doi:10.1021/nl402230v)
73. Lee H *et al.* 2019 Random nanohole arrays and its application to crystalline Si thin foils produced by proton induced exfoliation for solar cells. *Sci. Rep.* **9**, 19736. (doi:10.1038/s41598-019-56210-7)
74. Chiou PY, Ohta AT, Jamshidi A, Hsu HY, Wu MC. 2008 Light-actuated AC electroosmosis for nanoparticle manipulation. *J. Microelectromechanical Syst.* **17**, 525–531. (doi:10.1109/JMEMS.2008.916342)
75. Burghartz JN, Harendt C, Hoang T, Kiss A, Zimmermann M. 2009 Ultra-Thin Chip Fabrication For Next-Generation Silicon Processes. New York, NY: IEEE.
76. Burghartz JN, Appel W, Rempp HD, Zimmermann M. 2009 A new fabrication and assembly process for ultrathin chips. *IEEE Trans. Elec.* **56**, 321–327. (doi:10.1109/TED.2009.2010581)
77. Chan SH, Wong AK, Lam EY. 2008 Initialization for robust inverse synthesis of phase-shifting masks in optical projection lithography. *Opt. Express* **16**, 14746–14760. (doi:10.1364/OE.16.014746)
78. Feynman RP. 1960 Plenty of room at the bottom. *Eng. Sci.* **1**, 60–66. (doi:10.1109/84.128057)
79. Hang S *et al.* 2021 A review on the low external quantum efficiency and the remedies for GaN-based micro-LEDs. *J. Phys. D.* **54**, 153002. (doi:10.1088/1361-6463/abd9a3)