Current Leakage Mechanisms related to Threading Dislocations in Ge-rich SiGe heterostructures grown on Si(001)

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Abstract

The present work investigates the role of threading dislocation densities (TDD) in the low density regime on the vertical transport in $Si_{0.06}Ge_{0.94}$ heterostructures integrated on Si(001). The use of unintentionally doped $Si_{0.06}Ge_{0.94}$ layers enables the study of the impact of grown-in threading dislocations (TD) without interaction with processing-induced defects originating e.g. from dopant implantation. The studied heterolayers, while equal in composition, the degree of strain relaxation, and the thickness, feature three different values for the TDD: 3×10^6, 9×10^6 and 2×10^7 cm^{-2}. Current-voltage measurements reveal that leakage currents do not scale linearly with TDD. The temperature dependence of the leakage currents suggests a strong contribution of field-enhanced carrier generation to the current transport, with the trap-assisted tunneling via TD-induced defect states identified as the dominant transport mechanism at room temperature. At lower temperature and at high electric fields, direct band-to-band tunneling without direct interaction with defect levels becomes the dominating type of transport. Leakage currents related to emission from mid-gap traps by the Shockley-Read-Hall (SRH) generation is observed at higher temperatures (>100 °C). Here, we see a reduced contribution coming from SRH in our material, featuring the minimal TDD (3×10^6 cm^{-2}), which we attribute to a reduction in point defect clusters trapped in the TD strain fields.

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Germanium (Ge) and Ge-rich silicon-germanium (SiGe) alloys are gaining ever more relevance for the fabrication of novel devices for a variety of different applications. These include, among others, high-performance MOSFETs [1], near-infrared integrated light sources [2], detectors [3], THz quantum cascade lasers [4], spintronic devices [5] and semiconductor based qubits [6].

All these devices need to be manufactured using CMOS-compatible processes and, consequently, they have to be realized on (001)-oriented silicon (Si) substrates. Owing to the large lattice mismatch between Ge and Si (4.2%), lattice-strain management issues has to be considered. This includes the need for a full plastic relaxation of some of the layers, constituting the device material in order to tailor the strain and thus the electron- and/or hole-energy band profiles of the active layers. For Ge-rich SiGe/Ge heterostructures, this is commonly achieved by realizing a reverse graded SiGe virtual substrate (RGVS) on Si in which a relaxed Ge buffer is first deposited on Si; in the subsequent layer the Ge content is gradually decreased to promote the full relaxation of the lattice by formation of misfit dislocations (MD), while minimizing the density of threading dislocations (TD) [7,8]. Indeed, TDs are unavoidable in hetero-epitaxial growth and extend from the defective heterointerface running through the entire heterostructure, all the way up to the free surface of the crystal. Consequently, TDs can have a significant impact on the device performance. It is then of paramount importance to clarify the conduction mechanisms through TDs and gain an in-depth understanding of the electrical activity of TDs to provide a solid basis for device simulation and improved designs.

Early studies on the electrical activity of extended defects have been performed on plastically deformed high purity Ge bulk crystals. These studies pointed to the formation of TD-related one-dimensional (1D) bands of shallow states, which split off from the valence and conduction band, most likely related to stress fields associated with dislocations [9,10]. In case of Ge(Si) layers integrated on Si substrates, a network of dislocations forms at the Ge/Si heterointerface impacting the junction leakage current and generation-recombination properties [11]. Reported leakage currents in p-n junctions depend on the Ge content and increase proportionally with the amount of TDD [11,12], but the leakage current becomes independent of the TDD below ~10^7 cm^{-2} [13]. A post-deposition thermal anneal leads to a reduction in leakage current, that cannot be explained by the reduction of TDs, but is rather associated to a removal of point defect clusters in the material [12]. Previous investigations were carried out on devices featuring TDDs in the range of 10^7 - 10^{10} cm^{-2} [11,13,14] and the variation of TDD was limited to a post-growth anneal.

Device physics as well as device design requirements push towards a further reduction in TDD, making it crucial to obtain a quantitative understanding of the impact of TDs on device performance particularly in the low density regime of 10^5 – 10^7 cm^{-2} TDs.

Here we present a comprehensive analysis of the influence of the grown-in TDD on the vertical transport mechanisms in as-grown intrinsic $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructures featuring the same thickness and degree of plastic relaxation without introducing implantation-induced defects [15]. We conveniently use these Ge-rich SiGe RGVS because of the recent demonstrated capability to tune their TDD down to the low 10^6 cm^{-2} range, thanks to the presence of the $Si_{0.06}Ge_{0.94}$/Ge heterointerface [16]. Furthermore, this composition range is of special interest for applications using superlattice structures due to the requirement of strain-symmetrization between quantum-wells and tunnel barriers [17]. To study the influence of TDs on the vertical transport, we have realized 3D mesa diodes featuring a buried n^+-p homojunction close to the relaxed SiGe/Ge heterointerface by phosphorus (P) co-doping for the n-type side and exploiting the p-type nature of the defect states in the nominally intrinsic SiGe layer. Our goal is to investigate how the TDD correlates with leakage currents in the formed junctions and differentiate the dominating transport mechanisms by investigating the leakage behavior at different temperatures.

The analyzed Ge-rich SiGe heterostructures were grown on 200 mm diameter Si(001) wafers in a commercial ASM Epsilon 2000 reduced pressure chemical vapor deposition reactor at a pressure of 80 Torr. After wet chemical cleaning of the substrate and a prebake in a hydrogen (H_2) atmosphere in order to remove the native

oxide, a 100 nm-thick seed Ge layer was grown at 350 °C using a germane-nitrogen gas mixture. After the seed layer formation, variable thickness and fully relaxed Ge buffer of 4.5 µm, 2.3 µm and 1.2 µm were grown at a temperature of 550 °C. On top of the Ge/Si heterostructure, a 150 nm thick highly P-doped $Si_{0.06}Ge_{094}$ layer (1×10^{19} cm^{-3}) was deposited using silane and germane as reactant gas and phosphine as dopant gas. Finally, an intrinsic 1.2 µm thick $Si_{0.06}Ge_{0.94}$ layer was deposited at 550 °C. More details on the deposition process can be found in Ref. [16] .

The three $Si_{0.06}Ge_{0.94}$ epilayers feature the same thickness and degree of relaxation (R= 106% [16]) but different TDD values of 3×10^{6} (sample SA), 9×10^{6} (SB) and 2×10^{7} cm^{-2} (SC) as measured by the Secco etch pit count over a surface area of 55 μm^2. The surface of SC after etching is displayed in Fig.1 (a). The different TDD values were obtained relying on the procedure introduced in Ref. [16], i.e. by tuning the Ge buffer thickness. Related transmission electron microscopy (TEM) images can be found in Ref. [16]. Secondary ion mass spectroscopy (SIMS) results show that dopants (P, B) are below the detection limits in the intrinsic region of $3x10^{16}$ at/cm³ and $1x10^{17}$ at/cm³ for phosphorus and boron, respectively. The used process conditions resulted in diffusion lengths of P towards the surface of less than 5 nm/decade, allowing sharp buried homojunctions. Vertical mesa diode devices were fabricated out of the heterostructures as shown in Fig.1 (b). A 50 nm nickel (Ni) layer as a top metal contact was deposited on top of the intrinsic $Si_{0.06}Ge_{0.94}$ layers for defining the diode area. Subsequently, the remaining SiGe material was etched by inductively coupled plasma (ICP) mesa-etching [18]. Ohmic contacts with an average contact resistance over all devices of 30 Ω were formed on the n^+-$Si_{0.06}Ge_{0.94}$ layer using deposited Ni metal annealed at 330 °C for 30 s to form NiGe [19]. Ti-Al was deposited on top of the NiGe contacts to form bond pads. The size of the diodes was varied ranging from 250 µm to 1000 µm in diameter for separation of geometrical current components. Current-voltage (I-V) and capacitance-voltage (C-V) measurements were performed in a low-vacuum PMV200 probe station connected with a Keithley 4200A-SCS parameter analyzer. The temperature-dependent I-V characteristics were obtained at temperatures from 210 K to 475K. In all measurements, the NiGe bottom contact was connected to the ground (V=0V).

The diode we investigate in the following is the buried n^+-p junction formed between the highly n-doped and the nominally intrinsic $Si_{0.06}Ge_{0.94}$ layers (see Fig. 1 (b)). In fact, the intrinsic region behaves as lightly p-type doped, which has been verified by lateral Hall effect measurements, pointing to a p-type conductivity of the studied intrinsic material, featuring an effective hole density (averaged over the intrinsic region) in the 10^{15}-10^{16} cm^{-3} range (data not shown). Our observation is in agreement with previously published results on Ge-rich SiGe layers [20,21], GeSn films grown on Ge substrates [22], and plastically deformed Ge bulk material [23]. Nonetheless, the origin of this p-type conduction of the intrinsic Ge-based material is currently under discussion in literature, and is generally attributed to acceptor-like defect states caused by plastic deformation and/or strain relaxation [20,23].

As a consequence our devices behave like n^+-p junctions with the depletion region predominantly extending into the i-$Si_{0.06}Ge_{0.94}$ epilayer. As such, we can probe the vertical transport along the TD direction avoiding any possible interactions with dopant atoms.

In Fig.1 (c) we show the current density-voltage (J-V) characteristics at 25 °C of the three representative devices with identical geometries and mesa diameters of 250 µm, classified by their TDD. After correcting the data for the series resistance (R_S), the forward characteristics of the diodes is similar having ideality factors averaged over all diode sizes of 1.17, 1.23 and 1.43 for samples SA, SB and SC, respectively. In contrast, in the reverse bias regime (V_R) we observe an increase of more than 2 orders of magnitude in current density for an increase in TDD of one order of magnitude.

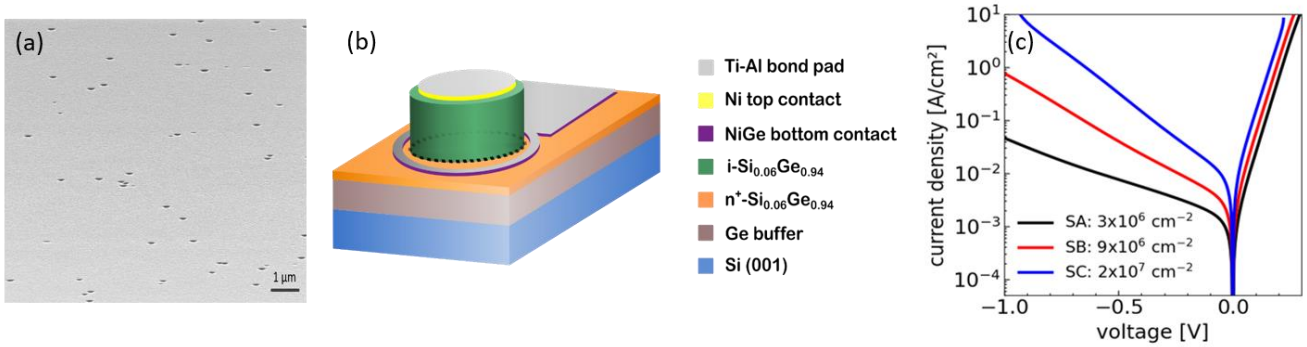

Fig. 1: (a) A scanning electron microscopic image of etch pits after 15 minutes of Secco etching, (b) a sketch of the devices fabricated on Ge-rich SiGe material, the dashed line display the investigated homojunction and (c) comparison of J-V characteristics of n^+-p homojunctions.

We can write the leakage currents (I_{leak}) as the sum of the contributing leakage current densities occurring at the perimeter P of the diode (J_P) and across the area A (J_A), as

$$I_{leak} = A \times J_A + P \times J_P . \quad (1)$$

By measurements carried out on diodes featuring different perimeter to area P/A ratios, we can separate J_A and J_P using a linear fit of I_{leak}/A versus P/A at certain reverse voltages [24]. The comparison of J_A and J_P for the samples SA, SB and SC is reported in Fig.2 (a). We first notice that J_P is almost identical for the three samples featuring different TDDs, witnessing a high reproducibility of the fabrication process. In contrast, J_A shows a clear dependence on the TDD [25,26]. Indeed, we observe a super-linear relationship $J_A \propto TDD^{\beta}$ [27], with $\beta(V_R)$ values always greater than 1 (see Fig.2 (b)). This is different from what is observed in low-Ge content $Si_{1-x}Ge_x$ layers (x< 0.3), where a linear relation between leakage currents and TDD has been reported [26]. The increase of β with higher V_R suggests an electric field dependence of the carrier generation, as we will discuss in the following. Like in Ge, the rather small bandgap of our $Si_{0.06}Ge_{0.94}$ layers ($E(L_c)$-$E(\Gamma_v)$=0.7 eV at 300 K) can enhance tunnel processes of carriers through the bandgap in presence of a strong electric field [28].

According to the Shockley-Read-Hall (SRH) theory [29,30], the reverse current of an abrupt one-sided n^+-p junction comprises a diffusion current (J_{diff}) and a generation current (J_{gen}) contribution [31,32], which can be expressed as

$$J_A = J_{diff} + J_{gen} = \frac{q n_i^2 D_n}{N_A L_n} + \frac{q n_i W_D}{\tau_{gen}} , \quad (2)$$

where q is the elementary charge, n_i is the intrinsic carrier concentration, N_A is the acceptor density in the p-type doped material, W_D the depletion width, τ_{gen} the generation lifetime, and D_n and L_n are the diffusion coefficient and diffusion length of the electrons, respectively. Eq. (2) predicts a linear increase of J_A for increasing W_D. Instead, this increase is found to be super linear as demonstrated in Fig. 2(c), where J_A is plotted as a function of W_D (J-W plot [33]) as measured by capacitance-voltage (C-V) measurements (not shown) that point towards an additional contribution of field-enhanced generation mechanisms [34]. It should be noticed here that W_D extends from the top of the n^+- into the i-$Si_{0.06}Ge_{0.94}$ layer, which is only 150 nm apart from the SiGe/Ge heterointerface. Close to the junction interface we have measured a positive charge density of $2x10^{17}$, $5x10^{17}$ and $7x10^{17}$ cm^{-3} for samples SA, SB, and SC by C-V profiling, respectively. In consequence of a higher N_A and consequently a narrower depletion width, the electric field at the junction is increased in higher TDD samples, e.g. the initial maximum electric field (V_R=0V) doubles from $1.5x10^7$ V/m to $3x10^7$ V/m in the range of TDDs investigated here. We notice that this narrowing of W_D plays a key role in tunnel-related

transport such as trap-assisted tunneling (TAT) or band-to-band (BTB) tunneling [35] as shown schematically in the inset of Fig. 2(c). In particular it can be responsible of an increase of the leakage current contribute related to the BTB tunneling with the TDD even if the BTB tunneling does not depend explicitly on defect levels [35]. Field-enhanced tunneling mechanisms such as TAT and BTB tunneling have been observed previously in Ge p-i-n photodetectors [36], p^+-n Ge junctions for MOSFETs [37], strained SiGe source/drain junctions [38] and Ge pFET junctions [39].

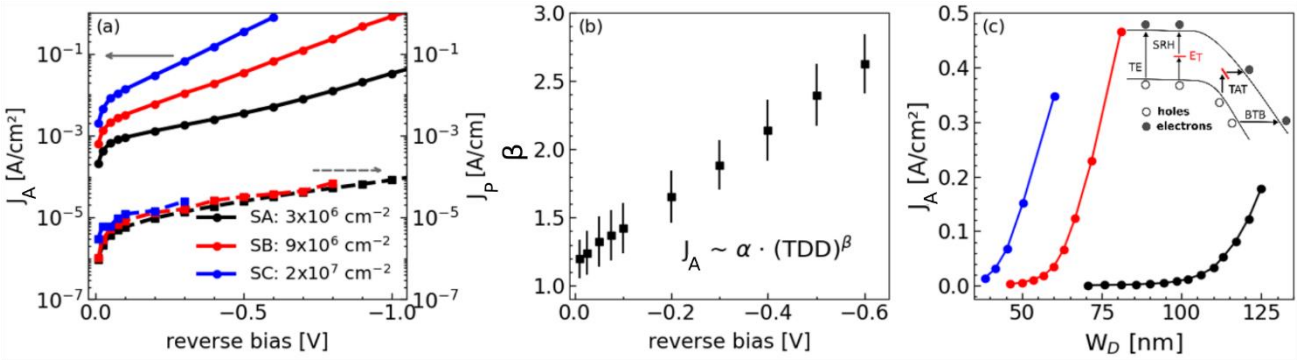

Fig. 2: The reverse current density at 25°C depending on the TDD. Panel (a) shows the area J_A and perimeter J_P current densities versus the applied reverse bias. (b) The super linear increase in J_A with applied bias is illustrated by a power law that models the relation between J_A and TDD. (c) The rise in J_A with increasing W_D. The inset shows a schematic picture of the discussed processes of carrier transport.

In order to assess the dominant mechanism of transport along TDs in i- $Si_{0.06}Ge_{0.94}$/Ge layers, the J-V diode characteristics were measured at temperatures ranging from 210K to 475K. As shown in panel a-c of Fig.3, the temperature dependence of the leakage current diminishes strongly with the applied reverse bias, pointing to the action of rather weakly temperature-dependent mechanisms, such as tunneling. The leakage current activation energy E_A, which is a product of all contributing transport mechanisms, is estimated by Arrhenius plots at different V_R [28]; in Fig.3 (d-f) we plot $\ln(J_R)$ vs 1/kT for different reverse biases with the Boltzmann constant, k and substrate temperature, T. For all three samples we identify three temperature regimes (T > 100°C, 25°C < T < 100°C, and T < 25°C) characterized by different slopes of the semi-logarithmic plot.

For temperatures above 100 °C, the calculated E_A at low V_R of all three samples are approximately half the $Si_{0.06}Ge_{0.94}$ bandgap ($E_g/2 \approx 0.35$ eV), suggesting a generation via the SRH mechanism: the second term in eq. (2) shows a dependency of the SRH generation rate on n_i and, consequently, its thermal activation energy corresponds to half the bandgap energy. The presence of these mid-gap traps may be related to the TDs, as such traps have been found in plastically deformed or heteroepitaxial n-type Ge layers, where they are attributed to the presence of point defect clusters trapped in the strain field of TDs [14]. Since we have not carried out any implantation processes in our samples, here we argue that these point defects should be related to growth induced defects such as vacancy complexes, which have been reported to show a strong recombination activity in Si when dislocations are present in the material [40,41]. It should also be noted that for the sample SA featuring the minimal TDD, the E_A at higher T is lower than those of samples SB and SC, pointing towards a reduced influence of the SRH generation mechanism. This is in line with our interpretation, since at lower TDDs the emergence of point defect clusters in the strain field of TDs is reduced.

At lower reverse bias (V_R > -1V), we observe a decrease in E_A with decreasing temperature, which indicates a major contribution of TAT in our material. For TAT, the SRH generation is increased by the field enhancement

factor, which in turn decreases exponentially with rising temperature [28]. It has previously been argued that TAT becomes the dominant mechanism of leakage currents for activation energies between $E_g/2$ and 0.1 eV in Ge based junctions, which are similar to our devices [28]. In the intermediate temperature range 25°C < T < 100°C, E_A is close to 0.1 eV in all three samples and we, thus, conclude that TAT is the dominant type of transport here. The tunneling via traps may become possible by the defect centers induced in our structures during the relaxed heteroepitaxial growth and the high electric fields present at the homojunction.

For temperatures below 25°C, the estimated E_A are far below 0.1 eV, and thus likely related to BTB tunneling without interaction of any defect levels this is similar to results obtained from samples with higher dislocation densities [28,32]. As suggested in Ref. [10], a possible local reduction of the bandgap energy due to the strain field around a TD may lead to an enhanced BTB tunneling.

By operating in a high electric field regime, increased band bending results in enhanced tunneling [36]. For applied reverse voltages < -1.0 V, the E_A of all three tested devices are below 0.1 eV suggesting BTB tunneling as the dominant leakage contribution probably caused by an increasing electric field present at the probed junction.

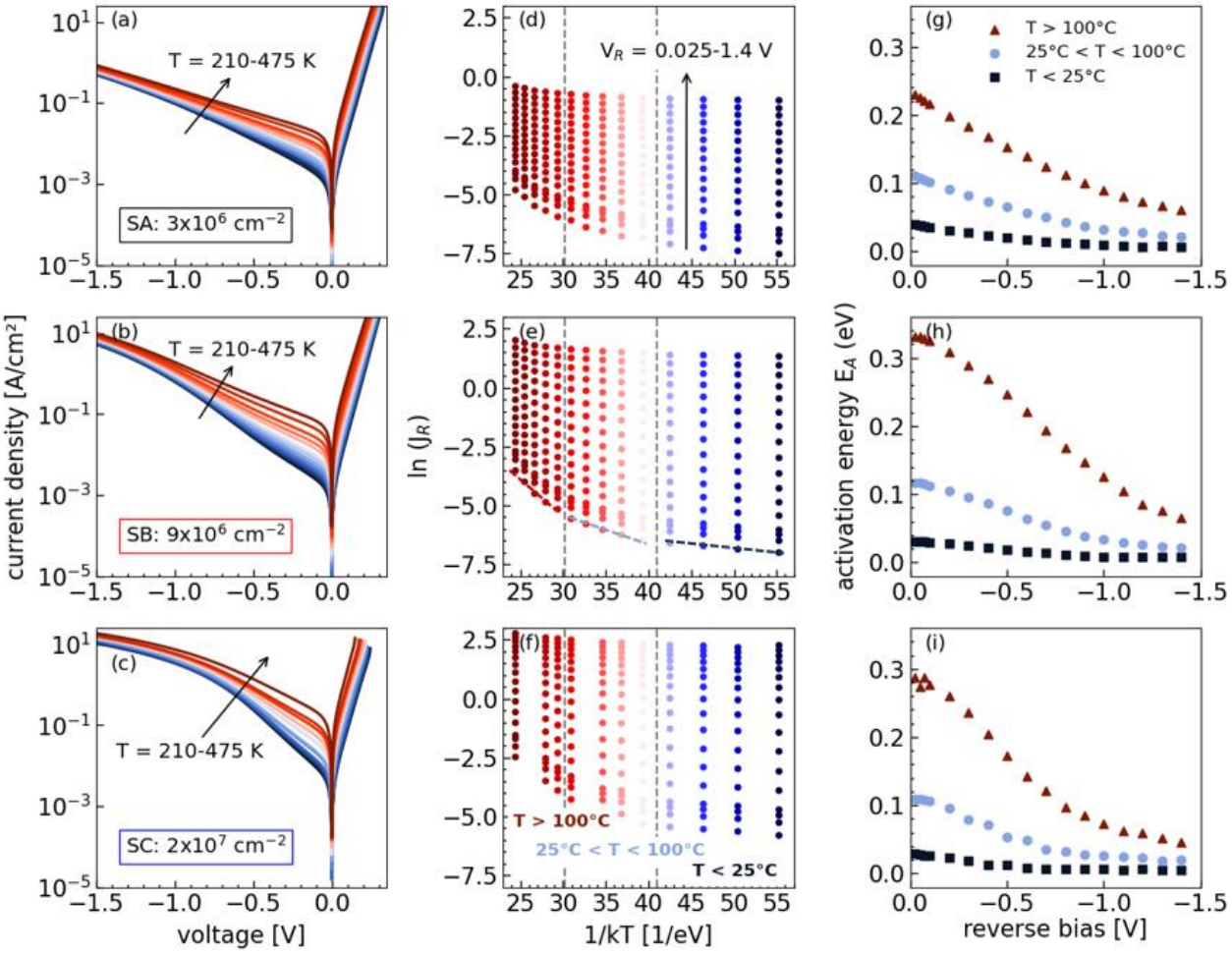

Fig. 3: The temperature dependent J-V characteristics ranging from 210K to 475 K of studied samples (a) SA, (b) SB and (c) SC. Arrhenius plots of the corresponding current densities at different V_R are shown in (d-f). The associated E_A for the three defined temperature ranges are plotted versus applied reverse bias in (g- i).

In conclusion, we produced intrinsic $Si_{0.06}Ge_{0.94}$ epitaxial layers, which are equal in composition, degree of relaxation and thickness but featuring different values of TDD to investigate the vertical transport along the grown-in TD direction in Ge-rich SiGe heterostructures integrated on Si(001). Based on the observed p-type conductivity of the unintentionally doped $Si_{0.06}Ge_{0.94}$ layer, a systematic study was performed on buried n^+-p homojunctions. It has been shown that the dependence of the area leakage current on the TDD shows a power law dependence, whereas the perimeter leakage current do not depend on the TDD. Temperature dependent J-V measurements revealed that the vertical transport is dominated by SRH generation via mid-gap traps for temperatures above 100 °C, whereas the influence of TAT increases with decreasing temperature becoming the dominating contribution to the leakage current at 25°C. Below 25°C and at high electric fields ($V_R < -1V$), leakage currents are dominated by BTB tunneling in our material. While SRH and TAT are directly linked to the presence of defect states in the forbidden band probably caused by the grown-in TDs, is the BTB tunneling more likely related to the existing high electric fields at the studied homojunction. Reducing the TDD leads to a strong reduction in area leakage currents in our devices, but our investigation also points towards an interplay between TDs and point defect clusters as the origin of the leakage currents. Due to the electric field dependence of the observed tunnel processes the leakage currents depend super-linearly on the TDD.
For device applications, a further reduction in leakage currents would be desirable. Future experiments could investigate the interplay of TDs and point defect clusters further and a systematic investigating of the influence of annealing steps on the leakage currents can provide a way towards reducing leakage currents.

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Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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