Biodegradable zinc oxide thin film transistors

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Abstract— In this work, biodegradable thin film transistors (TFTs) based on Zinc Oxide (ZnO) active layers are reported. To manufacture high performing devices, a planarization layer was applied onto the biodegradable substrate which led to a substantial decrease in the surface roughness and ensured that the substrate were smooth enough for device fabrication. ZnO TFTs were fabricated onto the planarized surface, tested and data supplied from the transfer curves showed a mobility of 2.9 cm^2/s, an on/off ratio of 8×10^6 and a threshold voltage of 2.5 V. Methods to further improve device performance and future applications are discussed.

Keywords—biodegradable electronics, ZnO, thin film transistors

I. INTRODUCTION

Bioresorbable and biodegradable electronic materials, are a category of materials which dissolve into benign and biocompatible by-products, thus providing unique opportunities for applications in new optoelectronic, electronic and sensing components[1,2]. These transient electronic devices can potentially disappear at pre-defined time intervals by redesign of the encapsulation or by controlling the media surrounding them. Although several examples of bioresorbable and biodegradable components and systems have been successfully reported over the last decade, there are many important challenges to be addressed before applications become widespread. In particular the lifetime of components made with such materials needs to be enhanced for longer term applications[3] and there are few reports of full electronic systems being developed, as most of the research focus has been on discrete devices. In the case of bioresorbable electronics, a number of reported applications have been demonstrated including for electronic skin (E-skin)[4] and biomedicine[5], where they systems can be used for monitoring, diagnosis and treatment of diseases. Biomedicine is a particularly exciting area, and such systems could dissolve in a controlled manner with respect under *in vivo* physiological conditions and leave behind no toxic by-products after dergradation[6].

Bioresorbable materials include metals, semiconductors, insulators and polymers. Table 1 lists some examples from each category adapted from La Mattina et al.[7]. Many of the materials used in bioresorbable electronics can also naturally degrade in landfill or other waste control systems. Developing electronics that are biodegradable, reusable or recyclable is of high importance as electronic waste (e-waste) is growing rapidly leading to significant health and social issues. E-waste is particularly problematic in developing countries as a result of the importation of e-waste from developed countries[8]. It is estimated that 40% of all e-waste in some developed countries is being exported illegally currently[9]. Much of the recycling in developing nations is done on a manual basis. There is a greater need to recycle e-waste in developing nations and traditional metallurgical processes for recycling can be extended to e-waste treatment technologies with moderate success. Nevertheless, materials can be lost in recycling process and require further refinement of purity after recovery.

In this paper, the manufacture of biodegradable thin film transistor (TFT) arrays using zinc oxide (ZnO) semiconductors is reported. Whilst this cannot remove all e-waste, we show the potential to reduce a portion of it as the end-products are benign. ZnO is a useful material to use for such purposes as it degrades via a hydrolysis reaction, leaving benign and non-toxic by end-products[10]. Zinc oxide (ZnO) is a distinct material owing to excellent transparency, chemical stability and high mobility; these characteristics have been exploited for TFTs, memory devices, and LEDs in the past. The approach reported here shows the fabrication of a TFT, however the approach can be adopted for manufacture of logic circuits and Radio Frequency Identification Tags (RFIDs) in the future.

TABLE I. EXAMPLE BIO-RESORBABLE AND -DEGRADABLE MATERIALS USED IN ELECTRONIC DEVICES*)*

LAYER	BIODEGRADABLE MATERIAL
CONDUCTORS/ METALS	*Metals:* Mg, Ca, Fe, Zn, Mo W, Mg alloy; *Organic*: CNTs, Graphene, Graphite, PEDOT:PSS.
SEMICONDUCTOR MATERIALS	*Inorganic: ZnO,* SiNM, *Organic*: PDPP-PD, PEDOT, Polypyrrole ; *Naturally derived:* Indigo, melanin
DIELECTRIC MATERIALS	*Inorganic:* MgO, SiO_2, Si_3N_4, AlO_x *Naturally derived* variety of polyshaccarides, polypeptide, lipids
SUBSTRATES/ ENCAPSULANTS	Silk, cellulose, PLA, PLGA, PCL, PVA, PHB, PHV, Ecoflex

II. Experimental

A. Substrate development

In this study, Poly(3-hydroxybutyrate-*co*-3-hydroxyvalerate) (PHBV) was used as the substrate for TFT device fabrication. PHBV is a biodegradable, nontoxic, biocompatible plastic produced naturally by bacteria and undergoes bacterial degradation in the environment. It is obtained by the copolymerization of 3-hydroxybutanoic acid and 3-hydroxypentanoic acid. One of the challenges of using PHBV directly in electronics are the low glass transition temperature (T_G) and relatively high surface roughness. As a result, the processing temperatures had to be kept below the T_G throughout the processing. In order to reduce the high surface roughness required the spin coating of polyvinyl acetate (PVA) was conducted. For TFT fabrication, the surface properties of the substrate are very demanding as the electrodes and semiconductor needs to be deposited onto a low roughness underlying substrate (typically average surface roughness (R_A) <20 nm), otherwise the semiconductor layer will inevitably contain many traps at the dielectric - semiconductor interface. Therefore, the PVA layer was used to planarise the surface prior to device fabrication. PVA with a typical molecular weight (M_w) of 80,000-100,000 was used, as received from Sigma-Aldrich. PVA (3 wt%) were spun onto the PHBV substrates at 3000 rpm. To ensure that all the solvents were removed from the PVA films, these films were annealed at 50°C in air atmosphere for 1 hour.

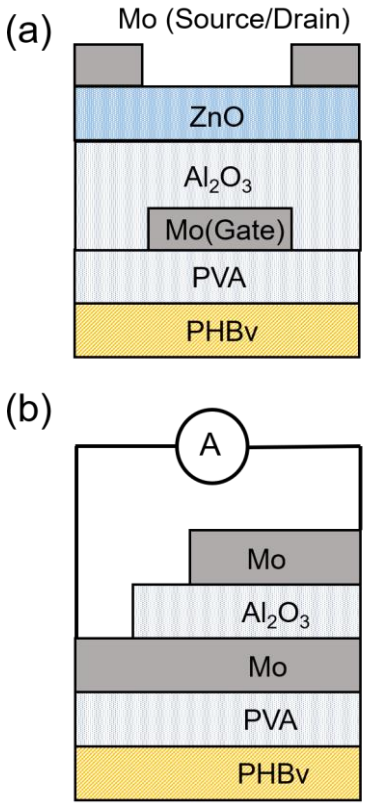

Fig. 1. (a) Schematic of the ZnO device used in this work using a bottom gate, top contact configuration and (b) schematic of the device used to verify the dielectric properties.

B. Thin film transistor fabrication and testing

Molybdenum (Mo) metal (50nm) was sputter coated on these film substrates using a Leybold350 sputter coater to form the gate metal. Subsequently, an aluminum oxide (Al_2O_3) dielectric layer of 60nm thickness was deposited using Leybold350 Electron-beam evaporator using 1-3mm of clear Al_2O_3 pieces with 99.99% purity, which were obtained from Testbourne Ltd (Al-5017-M Al_2O_3). Deposition rate was kept below 0.2 Angstrom(Å)/second for uniform layer deposition, the approach report by Kumar et al. [11]. Gate-oxide film thicknesses were varied but the optimum thickness was measured at 60nm based upon electrical data. ZnO layers were deposited using radio frequency (RF) sputtering technique at 75W and 1.2×10^{-2} mbar base pressure. The 99.99% pure ZnO target was pre-sputtered under closed shutter conditions for 5 min to eliminate any surface contaminants. A low sputter rate of 0.05 nm/s was used for the best uniformity. The ZnO layer thickness during deposition by sputtering was monitored with pre-installed thickness detector. Finally, source and drain electrodes using Mo were deposited with a range of channel widths. A schematic of the final device is shown in figure 1(a). This configuration was chosen because all of the materials within the TFT array are biodegradable and bioresorbable.

All the electrical measurements were performed at room conditions, avoiding exposure to ambient light, since ZnO presents persistent photoconductivity when irradiated by UV-light. For the TFT measurements, a two-channel source-measure unit (SMU, Keithley) was used, with probe connectors to perform the contacts to the electrodes (drain, source, and gate) and a voltage sweep ratio of 0.5 V/s for both V_{DS} and V_{GS}. For all measurements of ZnO TFTs, the electrical properties I_{on} , I_{off}, I_{on}/I_{off} ratio and mobility (μ) were extracted from transfer characteristics of TFT using equations 1 and 2

$$I_{DS} = \mu C_i \frac{W}{L}(V_{GS} - V_{th})^2 \quad (1)$$

$$\mu_{Sat} = \left(\frac{\partial\sqrt{I_{DS}}}{\partial I_{GS}}\right)^2 \frac{2L}{WC_i} \quad (2)$$

where, W is channel width and L is channel length, C_i is dielectric capacitance, μ is carrier mobility, V_{GS} applied gate voltage, V_D is drain voltage, and V_{th} is the TFT threshold voltage.

Surface roughness was characterised using mechanical profilometry because it allows for surface roughness measurements to be conducted over large areas. A large surface area needs to be mapped because a small number of surface topography issues could lead to poor TFT performances in larger arrays. Profilometry allows for large processing anomalies to be identified, but also allows for the surface

roughness to be accurately characterized as the resolution of our system is 5 Å.

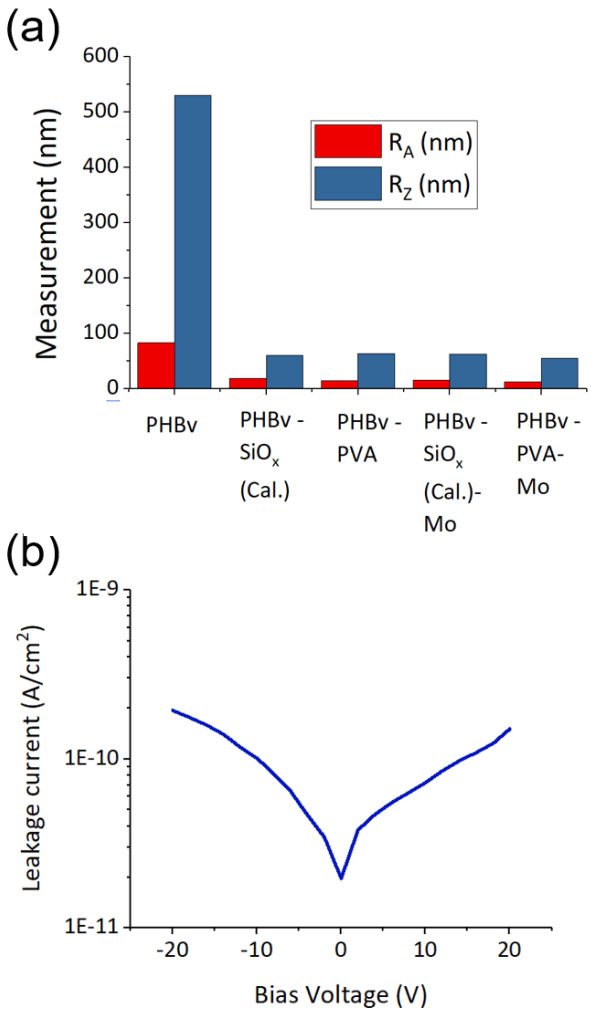

Fig. 2. (a) Mean (R_a) and (b) peak-to-valley (R_z) roughness of substrates developed in this work. Coating the samples with PVA showed the best reduction in roughness. "Calendaring" the samples after coating with a layer of SiO_2 showed a good roughness reduction as well. (b) Leakage current measurements conducted of between the Mp-Al_2O_3-Mo contacts using the device depicted in Figure 1(b)

III. RESULTS

A. *Planarisation results*

In this work PVA was applied to level and minimize the surface roughness of the PHBV to allow for high quality TFT to be subsequently fabricated. Figure 2(a) reports the roughness determined using mechanical profilometer scans for the four samples which have been planarized using two different approaches, which are compared to the surface roughness of the initial PHBV film. As it can be observed the roughness decreased significantly during the planarization step, especially the peak-to-valley (R_z) parameter, but also the R_A. Initially studies was conducted by depositing an e-beam evaporated SiO_2 layer; however, the surface roughness didn't significantly alter, probably as a result of the conformal nature of e-beam deposition. Despite this, an additional post processing was conducted using an Obducat nanoimprint machine to 'calendar' the sample[12,13], which was able to reduce the average surface roughness (R_A) to 19nm and R_Z to 61nm. After deposition of the gate metal (Mo, the surface roughness did not change significantly either (see figure 2a). However, the most successful method for levelling the surface was to spin coat PVA; in this case the R_A was reduced to 16nm and R_Z to 55nm. Despite the improved surface roughness, concerns remain about whether or not a thin dielectric and be deposited onto the gate metal and ensure no leakage current. Additional tests were conducted with the schematic showing in figure 1(b), where the gate dielectric was evaluated for its insulative behaviour. In terms of leakage current, it can be seen in figure 2(b), leakage currents are below 1nA/cm^2 using the PVA dielectric

B. *Device results*

ZnO TFT arrays were manufactured on planarized substrate. The results are presented in figure 3 where example output (a) and transfer curves (b) are shows for the device; the latter is used for the evaluation of the TFT mobility (μ) from the slope of the curve and the threshold voltage (V_{th}) from the extrapolation of the linear region to the horizontal axis. From the transfer curves, a mobility of 2.9 cm^2/s, an on/off ratio of 8 × 10^6 and a threshold voltage of 2.5 V were obtained. The performance parameters "on" current, "off" current, and on/off ratio were defined as the maximum channel current in accumulation, the lowest channel current in depletion, and their ratio, respectively. It is worth noting that the efficiencies of the devices are slightly lower than the state of the art in this field. The reason for this is twofold; firstly, the surface roughness of the dielectric is still relatively higher than conventional substrates (typically glass), and could be improved with further optimization and reductions in the surface roughness. Secondly the ZnO could not be annealed due to the underlying PHBV substrate and PVA layer, which means the device cannot be processed at temperatures greater than 80°C. Typically, annealing at temperatures greater than 300°C lead to substantive improvements in device performance[14,15].

IV. CONCLUSION

The result for a fully biodegradable TFT made using ZnO is reported. To our knowledge this is one of the first fully biodegradable TFTs made using ZnO-based TFTs. The performance is shown to be lower than state of the art devices but is limited by i) the surface roughness of the biodegradable substrate and ii) the consideration that annealing of the ZnO is not possible. The next steps are to build larger arrays of devices. Interconnects can be made using the materials set out in Table 1. There is also the possibility of creating complementary devices using a biodegradable *p*-type organic semiconductor.

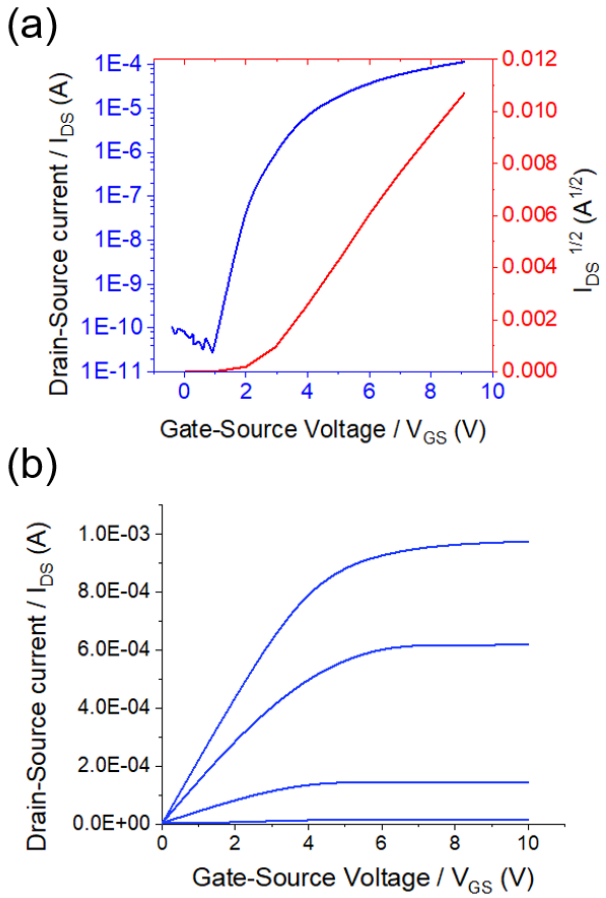

Fig. 3. (a) Transfer and (b) and output characteristics of ZnO biodegradable TFT with transfer characteristics obtained with V_{DS} =8 V

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