

Frontend Electronics for high-precision single photo-electron timing

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The next generation of high-luminosity experiments requires excellent particle identification detectors, which calls for imaging Cherenkov counters with fast electronics to cope with the expected hit rates. A Barrel DIRC will be used in the central region of the Target Spectrometer of the planned PANDA experiment at FAIR. A single photo-electron timing resolution of better than 100 ps RMS is required for the Barrel DIRC to disentangle the complicated patterns created on the image plane. R&D studies have been performed to provide a design based on the TRB3 readout using FPGA-TDCs with a typical precision of 10 ps RMS and custom frontend electronics with high-bandwidth pre-amplifiers and fast discriminators. The discriminators also provide time-over-threshold information, thus enabling walk corrections to improve the timing resolution. Two types of frontend electronics cards optimised for reading out 64-channel PHOTONIS Planacon MCP-PMTs were tested: one based on the NINO ASIC and the other, called PADIWA, based on FPGA discriminators. Promising results were obtained in a full characterisation using a fast laser setup and in a test experiment at MAMI, Mainz, with a small scale DIRC prototype.

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1. Introduction

The international Facility for Antiproton and Ion Research (FAIR), currently under construction at Darmstadt, Germany, will provide high luminosity beams for the planned PANDA experiment [1]. Particle identification in the target spectrometer will rely on a barrel DIRC (Detection of Internally Reflected Cherenkov light) [2, 3]. The low photon density per event in this type of detector requires very efficient single photon detection devices. The DIRC readout will use PHOTONIS (XP85012) Microchannel Plate (MCP-PMT) photodetectors, which provide an array of 64 channels with a timing resolution of about 37 ps RMS [4]. The DIRC detector will need about 15 000 channels which call for the use of high channel-density electronics. Considering that the average interaction rate is expected to be 20 MHz (with peaks up to 50 MHz) the readout electronics must be fast enough to sustain a rate of about 50-100 kHz/channel. Moreover, high precision timing on Single Photo-Electron (SPE) ($\sigma_{time} < 100$ ps RMS) is required for pattern reconstruction and background suppression [2].

2. The TDC Readout System

The third version of the TDC Readout Board (TRB3), developed at GSI, has been chosen as Data Acquisition System (DAQ) [5]. The TRB3 offers a multi-hit TDC and the capability to

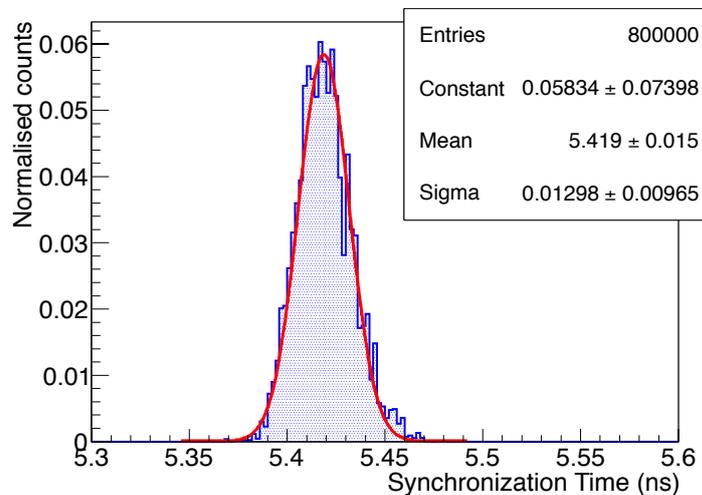


Figure 1: Synchronisation time precision between 2 FPGAs on a TRB3 board.

measure leading and trailing edge with 10 ps RMS time precision of input LVDS signals with a minimum pulse width of 500 ps. The actual maximum hit rate capability is 50 MHz while the maximum readout trigger rate is 700 kHz. The board comprises 5 commercial FPGAs¹: the central FPGA that can work as readout controller providing a Gigabit Ethernet link as well as central trigger system with 4 TDC channels; 4 peripheral FPGAs are programmed to provide 64 TDC channels

¹Lattice ECP3-150EA

each and a synchronisation time. The synchronisation of two different FPGAs in the same board is well defined with a timing precision of ≈ 13 ps RMS as shown in Fig. 1.

3. Frontend Electronics

R&D studies during the last years have focused on the realisation of FrontEnd Electronics (FEE) cards compatible with the TRB3 system to read out MCP-PMT signals. Two different FEE cards have been investigated:

- *NINO card* [6, 7] features a modular design with a current feedback amplifier² card (18 dB, up to 1.8 GHz bandwidth) followed by a discriminator board based on the NINO ASIC [8];
- *PADIWA* (PAnda DIrc WAsa) is a single card with pre-amplifiers³ (23 dB, up to 2.2 GHz bandwidth) and an FPGA⁴ programmed as discriminator.

Both cards are capable of reading out 16 channel (4 cards per MCP-PMT). The power consumption is about 160 mW/channel for the NINO card and 80 mW/channel for the PADIWA. The idea behind both cards is the same: after amplifying the small SPE signals (≈ 5 mV for this type of MCP-PMT) the discriminator returns an LVDS signal, whose leading edge corresponds to the arrival time of the photon and the width to the Time-over-Threshold (ToT), thus providing a coarse and fast measurement of the deposited charge. Both cards have been tested under realistic conditions illuminating an MCP-PMT with a fast laser pulser (35 ps FWHM, $\lambda \approx 633$ nm, for a photon level of 0.3 γ /event). The measured ToT, in both cases, is clearly correlated with the arrival time relative

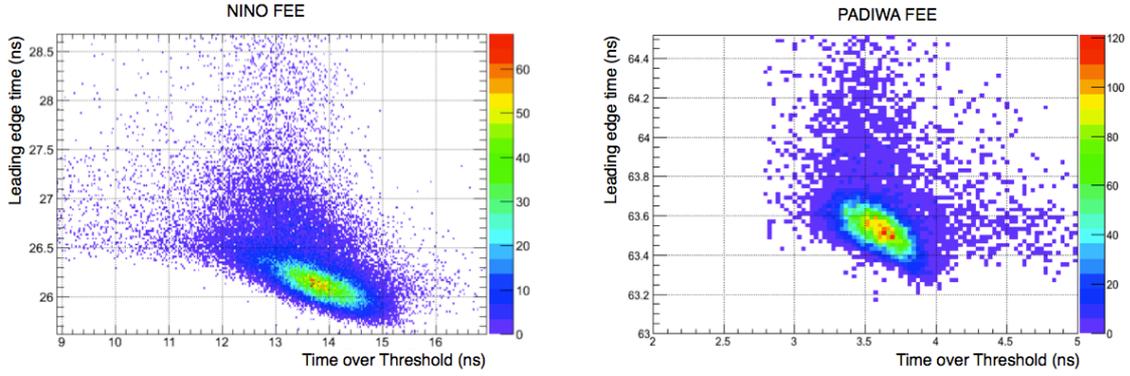


Figure 2: Photon arrival time as function of ToT showing walk dependence for NINO (*left*) and PADIWA (*right*) cards.

to the trigger from the laser, see Fig. 2, and can be used for a walk correction as given below:

$$t_{corrected} = t_{measured} - t^*(ToT) \quad (3.1)$$

where $t^*(ToT) = m \cdot ToT + q$ is a linear parametrisation of the distributions in Fig. 2.

²Texas Instruments, THS3201

³NXP, BGA2803

⁴Lattice MachXO2

Defining the timing resolution $\sigma_{t_{corrected}}$ as the standard deviation of $t_{corrected}$, the walk correction returns $\sigma_{t_{corrected}} \approx 75$ ps RMS for NINO and $\sigma_{t_{corrected}} \approx 70$ ps RMS for PADIWA, driven by the laser trigger uncertainty.

4. Test Experiment with DIRC prototype

The full electronics chain comprising MCP-PMTs, FEE and TRB3 has been extensively studied during a test experiment at the MAMI accelerator in Mainz. The continuous wave beam provides electrons with an energy of 855 MeV, a spot diameter of 1 mm and a negligible divergence. A small scale DIRC prototype, see Fig. 3 left, with a fused silica radiator bar and an expansion volume filled with mineral oil has been instrumented with a matrix of 6 MCP-PMTs, with a total of 384 channels read out with 4 TRB3 boards (3 slave + 1 master).

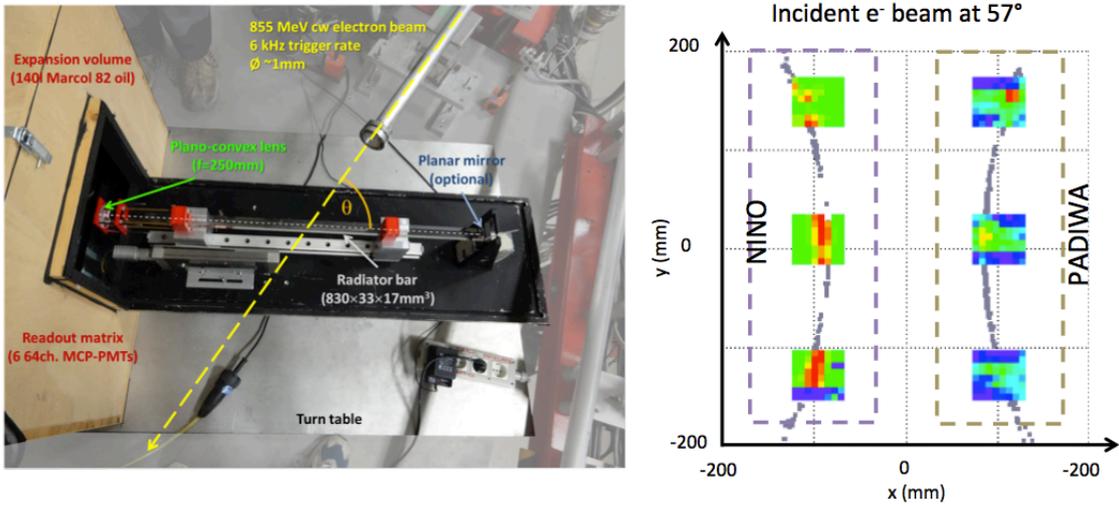


Figure 3: *left:* DIRC prototype setup. *Right:* observed Cherenkov pattern at 57° incidence angle: 3 MCP-PMTs on the left with NINO cards, 3 on right with PADIWA cards. Monte Carlo simulation is shown in grey.

Fig. 3 right shows the result for a configuration with 3 MCP-PMTs featuring NINO FEE cards (3 on the left) and 3 MCP-PMTs with PADIWA cards (3 on the right), the incidence angle between the radiator and the beam was 57° and the image shows an overlay of 1 million events. The gain of the MCP-PMTs was set to 1×10^6 . The Cherenkov ring pattern is clearly visible, especially for the NINO, using a time window of 50 ns and was confirmed by varying the incidence angles. The results agree with the Monte Carlo simulation (shown in grey and used only to verify the correct position). The PADIWA cards showed a lower efficiency caused by mistakes with the threshold settings. However, the visible spots in the central right and the top right MCP-PMTs moved in accordance with the simulation when changing the track angle.

4.1 Time studies

Time studies have been performed for a setup with MCP-PMTs equipped with NINO cards. The timing resolution σ_{SPE} on the SPE, which mainly depends on the electronics, has been mea-

sured taking the advantage of the charge sharing between neighbouring pixels in the same MCP-PMT, see Fig. 4 right. The low number of detected photons per event (2-3) guarantees the identification of charge sharing as SPE events. The results, shown in Fig. 4 left (red, raw differences; blue, corrected with walk corrections), can be fit with a sum of two Gaussians taking into account the presence of back-scattered photo-electrons inside the MCP-PMT. The timing resolution is $\sigma_{SPE} = \sigma_t$ where σ_t is the standard deviation of the narrow peak. The walk correction improves σ_{SPE} by about 70%, with an excellent value of $\sigma_{SPE} \approx 53$ ps RMS, mostly dependent on FEE and TRB3.

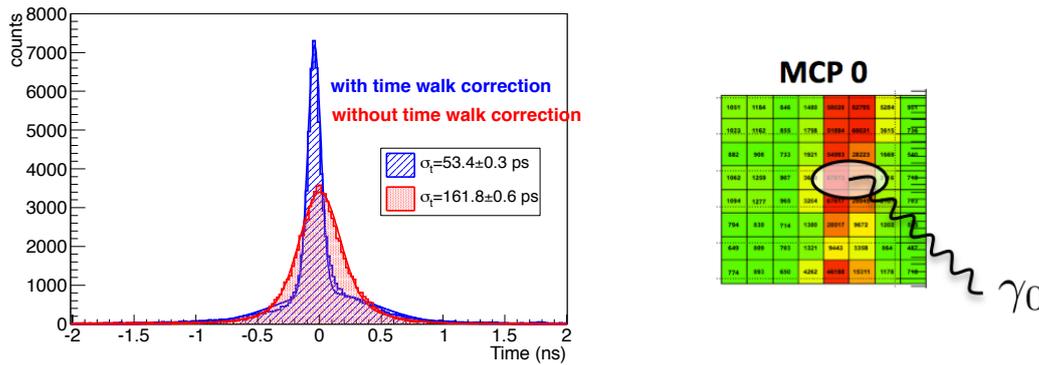


Figure 4: Left: measured timing resolution between neighbouring MCP-PMT pixels: corrected data (blue), uncorrected data (red). Right: sketch of the measurement, one photon hits the border of two pixels, generating charge sharing.

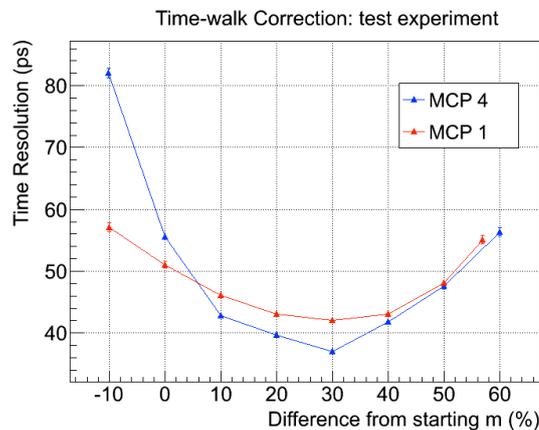


Figure 5: Optimisation for the slope parameter of the time walk correction. The red and blue dots show the result for two different pixels in two MCP-PMTs.

The different running conditions (e.g. temperature and gain), between the laser characterisation and the test experiment, demand an optimisation algorithm for the coefficients of $t^*(ToT)$ in the eq. 3.1. A simple solution has been investigated for the slope m , varying its value found with the laser studies and looking for a minimum of the corrected time resolution σ_{SPE} . Fig. 5 shows a minimum of σ_{SPE} at 30% from the original m value for two distinct pixels in two different MCP-

PMTs. The procedure improves the timing resolution σ_{SPE} on average to ≈ 40 ps RMS.

The timing resolution of the prototype $\sigma_{prototype}$ has been measured considering the time differences of pixels from different MCP-PMTs in the horizontal line ($y \approx 0$), which refer to photons with a symmetric path from the radiator to the focal plane, as described in Fig. 6 right. The results,

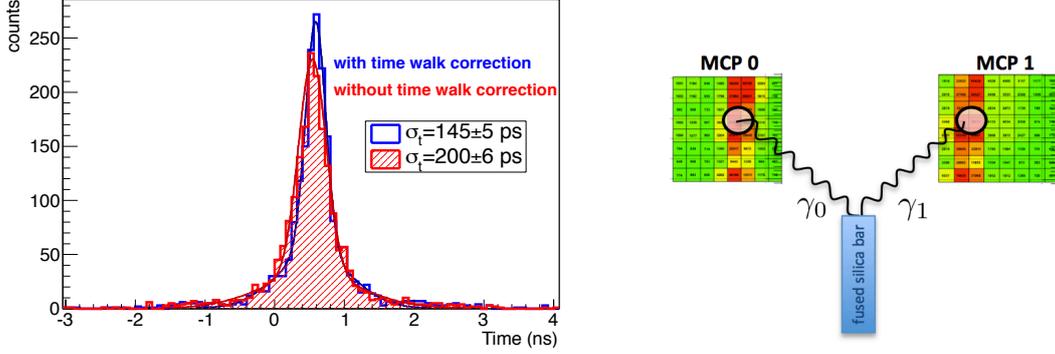


Figure 6: *Left:* measured timing resolution between different MCP-PMTs: corrected data (blue), uncorrected data (red). *Right:* sketch of the measurement, two photons, produced in the bar, hit at the same time two MCP-PMTs.

see Fig. 6 left (red, raw differences; blue, corrected with optimised walk corrections), are obtained with the same fitting techniques employed for σ_{SPE} . In this case the timing resolution corresponds to $\sigma_{prototype} = \sigma_t / \sqrt{2}$. The walk correction reduces the value of $\sigma_{prototype}$ from about 141 ps RMS down to 103 ps RMS improving the performance by about 25%.

The Monte Carlo simulation, used for the Cherenkov pattern, estimates the timing contribution of the radiator bar as $\sigma_{propagation}^{sim} \approx 63$ ps RMS. The measured $\sigma_{propagation}^{meas}$ can be obtained in first approximation with:

$$\sigma_{propagation}^{meas} = \sqrt{\sigma_{prototype}^2 - \sigma_{SPE}^2 - \sigma_{MCP-PMT}^2} \approx 87 \text{ ps RMS}, \quad (4.1)$$

where $\sigma_{prototype} \approx 103$ ps RMS, $\sigma_{SPE} \approx 40$ ps RMS and $\sigma_{MCP-PMT} \approx 37$ ps RMS. The difference between the simulation and the measurement is mainly due to synchronisation between different TRB3 boards and can be estimated as

$$\sqrt{\left(\sigma_{propagation}^{meas}\right)^2 - \left(\sigma_{propagation}^{sim}\right)^2} \approx 60 \text{ ps RMS}, \quad (4.2)$$

in agreement with the preliminary laboratory tests.

4.2 Global performances

The optimisation of the SPE detection has been studied with different MCP-PMT gains. Fig. 7 shows the average time over threshold for SPE events at different gains and, as expected, a qualitative linearity is observed. The timing resolution, as shown in Tab. 1, gets worse by lowering the MCP-PMT gain. The ability to correct for time walk shows also a substantial deterioration at lower gain. This indicates that every gain setting calls for proper walk coefficients.

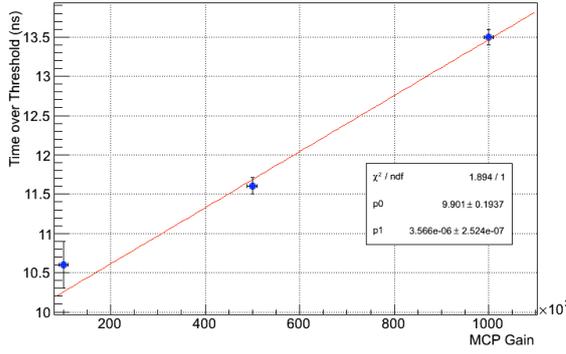


Figure 7: Average time over threshold for SPE events at different MCP-PMT gains.

Gain	Timing Resolution (ps RMS)	
	not corrected	corrected
1×10^5	190	180
5×10^5	175	130
1×10^6	161	40

Table 1: Timing resolution at different MCP-PMT gains.

The timing performance, as established in Fig. 8, was shown to be stable over an extended period. The TRB3 DAQ proved a high efficiency with < 1 lost event in a million and lost hits in less than 1% of the events.

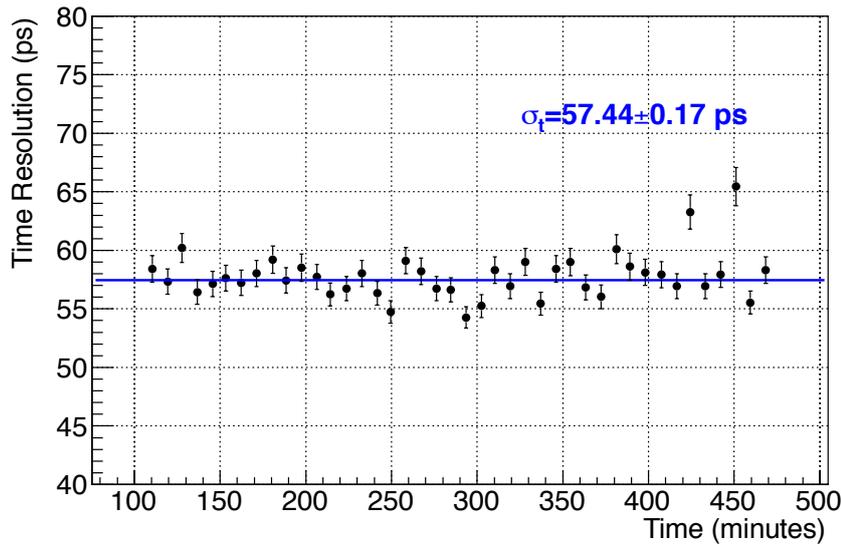


Figure 8: Measured σ_{SPE} over a extended period of data taking.

5. Conclusion

R&D studies for fast and high precision FEE for the PANDA Barrel DIRC show encouraging results. The TRB3 provides a stable DAQ system and high precision TDC. A full characterisation of NINO and PADIWA FEE with a fast laser pulser proves the feasibility of using ToT to correct the time walk. The results of a test experiment demonstrate an excellent timing, which meets PANDA requirement of $\sigma_{SPE} < 100$ ps RMS.

Further activities will focus on the rate capability of the full chain in order to achieve the desired values. The optimisation of the power consumption is another key point of the future developments.

A test experiment of a full system prototype with PADIWA FEE readout is foreseen in Summer 2014.

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