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A sectorial scheme of gate-all-around field effect transistor with improved electrical characteristics

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ABSTRACT

Reliability and controllability for a new scheme of gate-all-around field effect transistor (GAA-FET) with a silicon channel utilizing a sectorial cross section is evaluated in terms of I_{on}/I_{off} current ratio, transconductance, subthreshold slope, threshold voltage roll-off, and drain induced barrier lowering (DIBL). In addition, the scaling behavior of electronic figures of merit is comprehensively studied with the aid of physical simulations. The electrical characteristic of proposed structure is compared with a circular GAA-FET, which is previously calibrated with an IBM sample at the 22 nm channel length using 3D-TCAD simulations. Our simulation results show that sectorial cross section GAA-FET is a superior structure for controlling short channel effects (SCEs) and to obtain better performance compared to conventional circular cross section counterpart.

1. Introduction

To improve the device performance, reliability against SCEs and scalability, several structures and materials have been proposed during last decades. It has been shown that the electrical characteristics of a single gate Field Effect Transistor (FET) can be improved by applying device engineering methods in the gate [1,2], active region [3–6], and buried oxide [7–9] or switching to other structures like double gate MOSFET [10–12], Fin-FET [13–15], nanowire FET [16,17], and gate-all-around (GAA) FET structures [18–21], due to increase of the gate electrostatic control over the channel. Furthermore, there is a consensus in the community to incorporate other transport mechanisms and materials in MOSFETs comprising of tunnel FETs (TFETs) [22–24], 2D graphene sheet and graphene nanoribbon structures [25–27], and carbon nanotubes [28,29], to ensure continuous device performance improvement. However, TFETs have the drawbacks of low drive current and ambipolar conduction, which restricts their application in digital and analogue circuits [30–36]. Recently several techniques have been proposed to overcome mentioned drawbacks including incorporation of high-k dielectric material [37], utilizing silicon source stack [38], and using auxiliary gate above the source side [39]. On the other hand, making FETs comprised of graphene and nanotubes need more research and development in the fabrication process for deploying them in digital circuits [40,41].Touching upon above mentioned facts, it seems that GAA-FETs are ultimate structure of scaling [42,43]. Wrapping gate around the channel of this structure leads to better electrostatic control which results in better remedy of short channel effects in these devices [44]. Although GAA-FETs are of promising structures for deep scaling compared to Fin-FETs, Omega-FETs, double gate-MOSFETs, and single gate MOSFETs, weak subthreshold characteristic is among serious concerns regarding to these devices which limits their applications in low power and steep switching circuits [45].

In this work we propose a scheme of sectorial cross section gate-all-around field effect transistor (Sec-GAAFET) and consider its electrical characteristics against SCEs by scaling the channel length. The electrical characteristics of proposed structure are compared with a circular cross section GAAFET (Cir-GAAFET) sample of IBM, which had previously been calibrated by ATLAS simulator. In order to have reliable results, quantum models have been utilized in our simulations so that quantum mechanical confinement phenomenon obviously influence on the carrier distribution

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and electrical characteristics of the proposed device. Furthermore, Self-consistent solution of Schrödinger and Poisson equations in the transverse direction of GAAFETs under study is obtained to calculate carrier concentration and potential in the device more accurately.

The rest of this paper is arranged in the following form. We introduce the device geometric parameters and TCAD-simulation settings and incorporated models in Section 2. Simulation results are presented and discussed in Section 3 and a comprehensive conclusion regarding this study is coming in Section 4.

2. Device structure and simulation setting

A schematic view of the proposed structure is illustrated in Fig. 1(a). During this work the electrical characteristics of this structure is compared with a circular cross section GAA-FET as shown in Fig. 1(b). All geometric parameters related to these devices are presented in Table 1. It is worth noting that the oxide thickness, silicon radius, and incorporated angles of the proposed structure have selected such that both devices have equivalent oxide and silicon areas in the cross section view in order to make a fair comparison. The proposed fabrication process of the Sec-GAAFET structure is shown in Fig. 1(c). Complex tilt lithography and deposition fabrication process can realize this structure [46]. The silicon wafer in step (1) is angularly dry etched in step (2) and then gate material is deposited in step (3). After another dry etching in gate material in step (4), SiO_2 is deposited in step (5). Then a tilt angular etching is done in the oxide and silicon is

Table 1
Parameters of Cir-GAA-FET and SEC-GAAFETstructures.

Parameter		Value	
		Cir-GAA	SEC-GAA
Circular silicon/SiO_2 radius	r_1	6.4 nm	1 nm
	r_2	–	11.13 nm
Side oxide Angle (theta 1)		–	15 deg
Silicon Angle (theta 2)		–	120 deg
Gate oxide thickness		1.5 nm	1.1 nm
Channel Length (L_G)		22 nm	22 nm
Source/Drain extended length (L_S/L_D)		20 nm	20 nm
Lateral Gaussian doping fall off in drain/source		0.02	0.02
Source/Drain n-type doping		$5 * 10^{19}$ cm^{-3}	$5 * 10^{19}$ cm^{-3}
Gate Workfunction (WF)		4.512 eV	4.512 eV

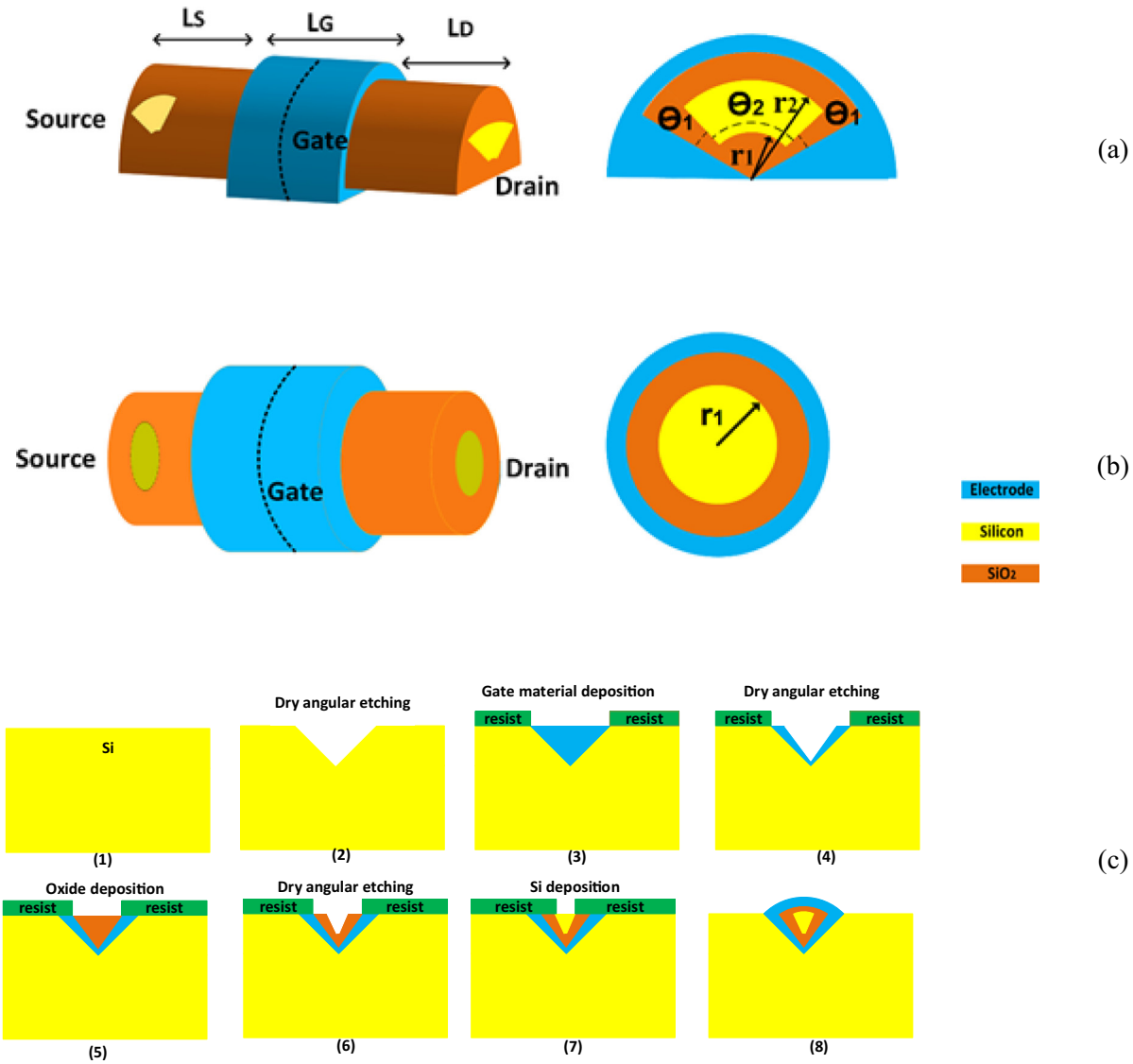

Fig. 1. Schematic view along with cross section of (a) Sectorial GAA-FET and (b) circular GAA-FET under study. (c) The proposed fabrication process of the Sec-GAAFET.

deposited in steps (6) and (7). Afterward by a proper deposition the whole structure is formed in step (8).

All of simulations in this work have performed using 3D-ATLAS version 5.22.1.R which is a popular simulator for predicting electrical performance of semiconductors devices at special bias conditions. In this work we utilized Schrödinger and drift-diffusion mode-space (DD_MS) quantum models. Schrödinger model predicts eigen energy and eigen function of each subband in the transverse direction of silicon channel, and DD_MS model is a semi classical transport model for devices with intense confinement in the transverse direction [47]. Due to the fact that this model uses classical ATLAS models comprising of drift-diffusion and mobility models in the transport direction, calculation time is less than fully quantum transport model of NEGF mode-space (NEGF_MS) which considers ballistic transport in the device. Also, von Neumann boundary conditions for potential is applied in the source and drain contacts. Enabling this type of boundary condition along with Schrödinger model is useful for devices with transverse confinement. And, as the potential in the source and drain are float, thus total carrier concentration in these contacts change with the bias. In fact, the current calculation in the device starts with electron concentration estimation using the following equation [47]:

$$n_{vb} = 2\frac{K_B T}{A\pi\hbar^2}\sum_{v}\ln\left[1+\exp\left(-\frac{E_{vb}-E_{F,vb}}{K_B T}\right)\right]\sqrt{m_1^{vb}m_2^{vb}} \quad (1)$$

where parameters n_{vb}, $E_{F,vb}$, E_{vb}, and $m_{1,2}$ denote electron concentration, quasi-Fermi level, electron energy and electron effective mass in subband v with effective mass b, respectively. Also K_B, h,T, and A are Boltzmann's constant, Planck's constant, absolute temperature, and normalized area, respectively. The calculated electron concentration is substituted in the charge part of Poisson's equation and then calculated potential is substituted back into Schrödinger equation to extract eigen energy and eigen function. This iterative calculation process continues until a self-consistent solution is obtained between two equations. Afterward, the current of each subband is calculated using the following one dimensional drift-diffusion transport model [47]:

$$J_{vb} = q\mu_{vb}n_{vb}\frac{\partial E_{vb}}{\partial z} - qD_{vb}\frac{\partial n_{vb}}{\partial z} \quad (2)$$

where q, μ_{vb}, and D_{vb} are electronic charge, carrier mobility and diffusion coefficient of each subband in z direction.

The Cir-GAAFET in this study is an approximation of a non-uniform cross section IBM GAAFET sample with a 22 nm channel length and a perimeter of 40.21 nm which is estimated by a circle with radius r_{Si} = 6.4 nm as given in the literature [21,48]. Fig. 2(a) compares the transfer characteristics of our simulation and IBM experimental results at V_{DS} = 0.05 V and V_{DS} = 1.0 V [21,48] which achieved using the Gaussian doping profile shown in Fig. 2(b) similar to [48]. Based on this profile, this device is not junctionless, since junctionless devices have uniform doping profile. According to this figure there is a good agreement between the results obtained by calibration of fitting parameters like electron mobility and effective mass. Thus it is expected that our following simulation results have enough accuracy and they are reliable to report. It is worth noting that the main idea behind proposition of this structure is to improve the electrical characteristics of GAA-FET in terms of subthreshold characteristics, I_{ON}/I_{OFF} ratio and to remedy short channel effects with stronger electrostatic control of the gate over the channel.

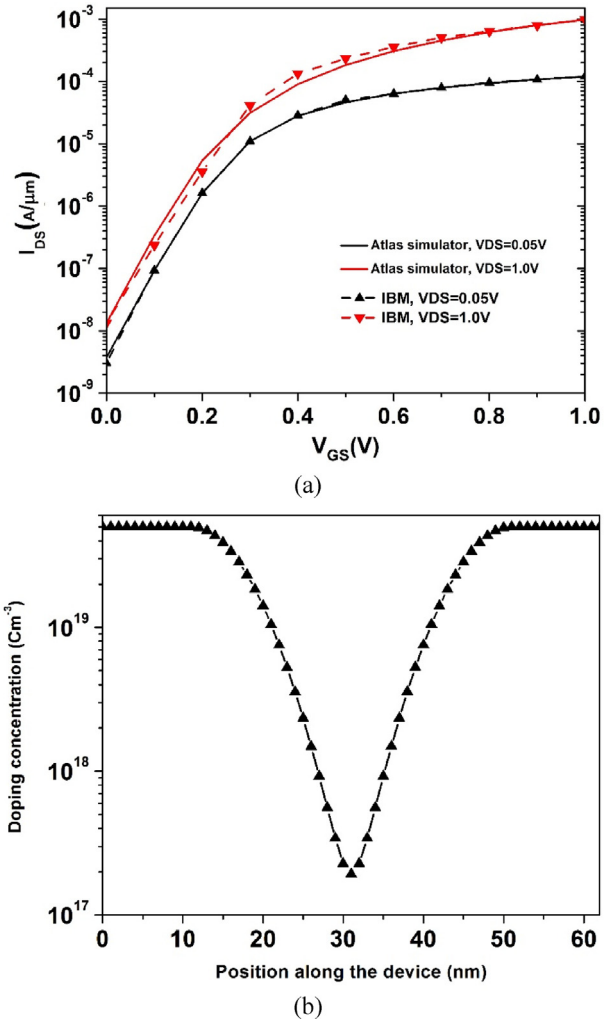

Fig. 2. (a) Calibration of ATLAS simulator against experimental results [21,48] and (b) Gaussian doping profile considerations in calibration.

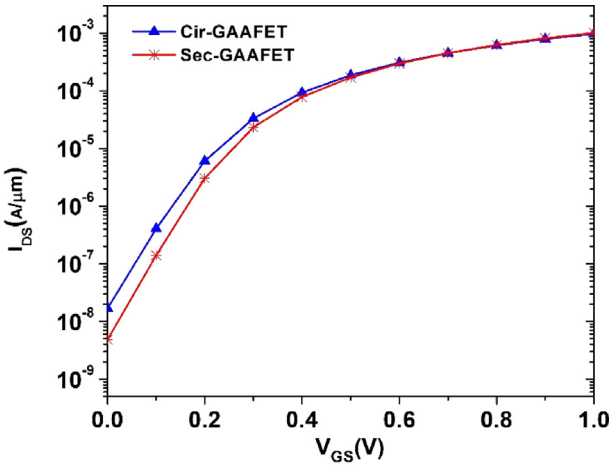

Fig. 3. Transfer characteristics of Cir-GAAFET and Sec-GAAFET at V_{DS} = 1.0 V.

3. Results and discussion

Fig. 3 depicts the transfer characteristics of both Cir-GAAFET and Sec-GAAFET at V_{DS} = 1.0 V and gate workfunction of WF = 4.512 eV. It is obvious that the Sec-GAAFET has better subthreshold characteristics and drive current compared to its counterpart. We believe the lower off-state current in the proposed device is due to better gate electrostatic control over the channel

of this structure. In fact, as the silicon channel perimeter in the Sec-GAAFET is more compared with Cir-GAAFET (45.6 nm vs 40.21 nm), so it is expected that its gate electrode has more influence on the channel region and the carriers passing through the channel. Higher drive current in the proposed structure is indebted to its better transconductance condition which is discussed later. It should be noted that by increasing the gate workfunction, threshold voltage increases and then the transfer characters shift to the right side. In such a case, both I_{OFF} and I_{ON} currents will be reduced. Also, if the gate workfunction is decreased, then reversed results is obtained or transfer characteristic shifts to the left; threshold voltage reduces; and both I_{OFF} and I_{ON} currents increase [46].

Transconductance in a FET is defined by the following relation [49]:

$$g_m = \frac{dI_D}{dV_{GS}}|_{V_{DS}=const} \quad (3)$$

This parameter reveals the amount of drain current increase with V_{GS} and also has influence on the device amplification amount. Due to the fact that transconductance in the Sec-GAAFET is more than its counterpart according to Fig. 4, therefore it is expected that the gate has stronger control over the channel in the proposed device compared to Cir-GAAFET and this causes a higher drive current in the Sec-GAAFET. The ratio of g_m/I_D in a device depicts amplification (g_m) over power dissipation (I_{DS}) rate and it is an interesting parameters for device and circuit designers [50]. Based on Fig. 4, this rate is higher in the proposed device, which shows improvement in the device performance from efficiency perspective.

Fig. 5 depicts electron current density in the devices under study at bias V_{GS} = V_{DS} = 1.0 V. As it is obvious, electron current density in the silicon channel of two devices is more intensive than silicon-oxide interface, which is due to the fact that electron quantum mechanical confinement phenomenon occurs in the transverse direction of both structures [44]. Moreover, since Cir-GAAFET has symmetrical cross section, electron current density distribution is also symmetric in this device. However, asymmetric cross section in the Sec-GAAFET has led current density to concentrate near the sharp corners of sector where gate potential has more influence on the electrons moving in the channel.

In another investigation we have studied scaling effect on three parameters: I_{ON}/I_{OFF}, subthrehold slope (SS), and threshold voltage (V_{TH}). Fig. 6 shows I_{ON}/I_{OFF} ratio of both structures at two drain voltages of V_{DS} = 0.05 V and V_{DS} = 1.0 V. It confirms a higher on-state to off-state current ratio for Sec-GAAFET. As the drain voltage increases, due to drive current enhancement, the excellence of the proposed structure is significantly seen in terms of having better I_{ON}/I_{OFF}.

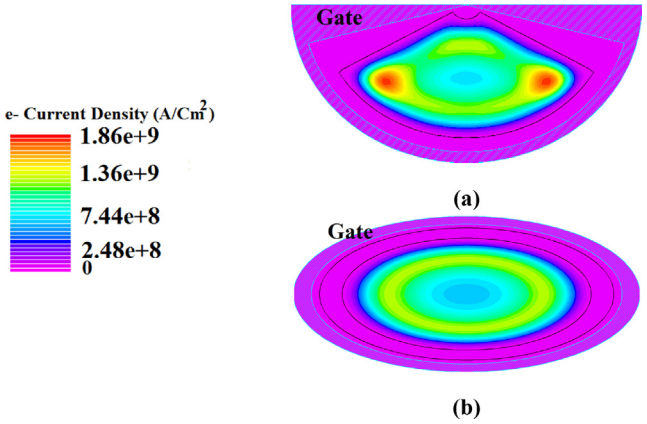

Fig. 5. Electron current density counterplot of (a) Sec-GAAFET and (b) Cir-GAAFET at V_{GS} = V_{DS} = 1.0 V.

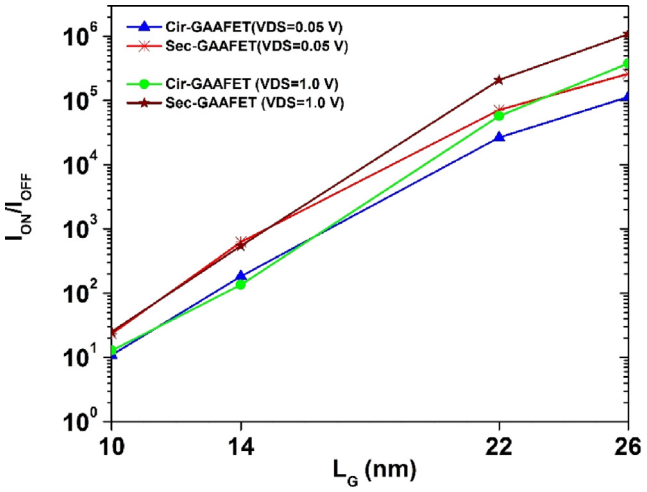

Fig. 6. On-state current over off-state current ratio variation by scaling at V_{DS} = 0.05-V and V_{DS} = 1.0 V.

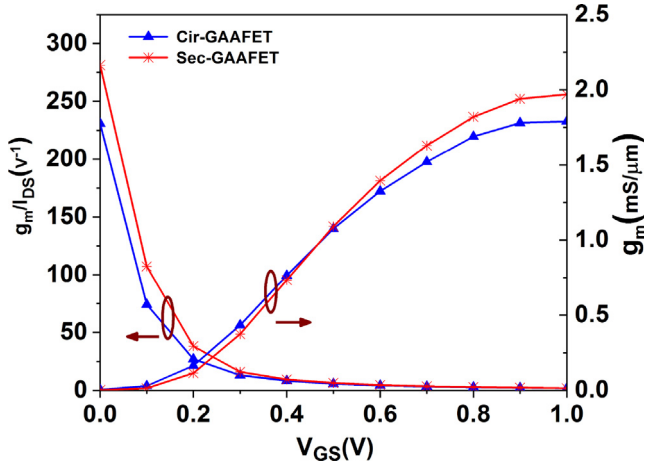

Fig. 4. Transconductance over drain current ratio (left axis) and transconductance (right axis) versus gate voltage at V_{DS} = 1.0 V.

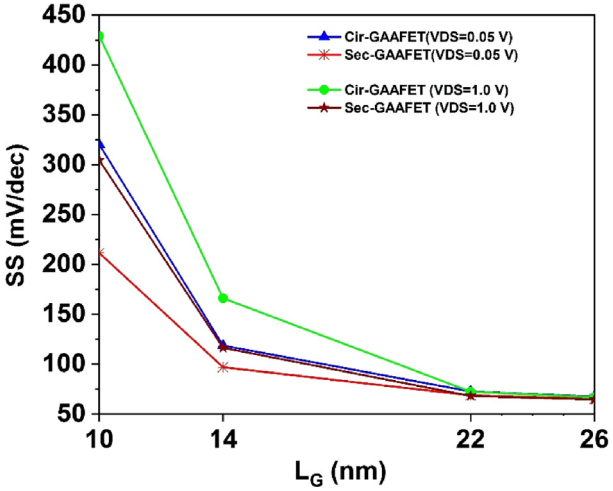

Fig. 7. Subthreshold slope (SS) variation by scaling at V_{DS} = 0.05 V and V_{DS} = 1.0 V.

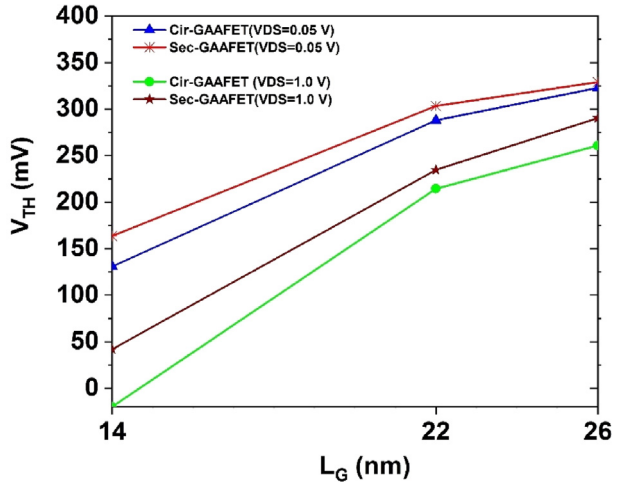

Fig. 8. Threshold voltage variation by scaling at V_{DS} = 0.05 V and V_{DS} = 1.0 V.

Subthreshold slope (SS) is another serious concern for GAA-FETs. This parameter has better status in Sec-GAAFET as scaling occurs according to Fig. 7. Since gate has an enhanced control over the channel in the proposed device, this parameter is lower for this device compared to its counterpart for both high and low drain bias conditions.

In Fig. 8 threshold voltage variations of both devices under study have been shown. To extract V_{TH}, constant current criteria at $I_{DS} = 1 * 10^{-5}$ A is used. This figure contains two SCEs improvement. First, it is obvious that V_{TH} roll-off in the proposed device is lower than its counterpart by scaling. Second, since V_{TH} roll-offs are lower in Sec-GAAFET under two biases of V_{DS} = 0.05 V and V_{DS} = 1.0 V, it means that the influence of drain bias on the channel region has been limited [51]. So, it is expected that the short channel effect of DIBL to be reduced in the proposed device compared to its counterpart.

It should be noted that using hetero-junction at the source region can modify the electrical characteristics. Germanium for instance owing to (a) lower bandgap, (b) higher carrier mobility compared to silicon and (c) pinning its fermi level close to the valance band in the equilibrium, can degrade subthreshold characteristics and increase short channel effects by modifying energy band profile of carriers in the device [46].

4. Conclusion

In this paper we introduced a new scheme of GAA-FET with a sectorial cross section. The proposed structure has shown better gate electrostatic control over silicon channel compared to a 22 nm counterpart from IBM sample. This improvement is indebted to more silicon channel perimeter in the Sec-GAAFET than circular GAAFET in equal silicon channel area conditions. Based on our simulation results the proposed device has better electrical performance in terms of subthreshold characteristics and drive current. Furthermore, Sec-GAAFET has shown more endurance against short channel effects comprising of threshold voltage roll-off and DIBL by scaling. Therefore, it is a good method to switch toward ultimate structures of GAAFETs by increasing channel perimeter to area ratio with fabrication and lithography progress for deep scaling.

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