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A nano-FET structure comprised of inherent paralleled TFET and MOSFET with improved performance

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ABSTRACT

In this paper we unveil of a new structure in which a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is paralleled with a Tunneling Field Effect Transistor (TFET) to increase on-state current. In order to enhance tunneling current injection rate in the device, workfunction engineering in gate and substrate electrodes and doping engineering in channel (source pocket) are utilized. For further on-state current enhancement of device, thermionic injection mechanism is used by incorporating a MOSFET in the structure. In addition, hetero gate dielectric is used to reduce parasitic capacitances. Our analysis show PTM-FET transistor has several excellences in comparison to DW HGD SP TFET in terms of transconductance, I_{on}/I_{off} current ratio, short channel effects like DIBL, Early voltage, maximum transducer power gain, unilateral power gain, gain bandwidth product, unity gain frequency and parasitic capacitances. The mentioned advantages for PTM-FET transistor can be a window of utilizing this device in both low power and high performance integrated circuit applications.

1. Introduction

Continuous downscaling and increasing the number of transistors in unit area, has led to aggressive increase in short channel effects and chip power density and temperature, which these effects in turn degrade device performance [1–12]. Although supply-voltage scaling reduces dynamic power, but threshold voltage should also be reduced with the same rate to have enough on-current in the device [13]. Threshold voltage reduction causes off-current increase, which this leads to static power increase in the device. In fact, off-current increase is originated from subthreshold swing (*SS*) limitation of 60 mV/dec, due to Boltzmann distribution of carriers at room temperature [13].

In order to overcome abovementioned restrictions and to control short channel effects, different structures comprised of FinFET, nanowire, and TFET have proposed [14–17]. In the meantime Tunnel-FET can operate at lower voltage and has excellent subthreshold characteristics compared to MOSFETs [18]. Unlike MOSFETs which their carrier injection mechanism is dominated by thermionic emission and drift–diffusion, current flow in TFET is based on interband tunneling [19–21]. Since valence band electrons do not follow the Boltzmann's distribution and carriers tunnel through a barrier whose width is a function of bias voltage, interband tunneling is a non-thermal process [21]. Therefore TFET transistor has a lower *SS*, off-current and lattice temperature. Among these advantages, TFET device has its drawbacks too. It suffers from lack of on-current compared to MOSFET and it has ambipolar current for negative gate voltages [13,21]. Although to increase on-current various suggestions based on bandgap engineering [22,23] and doping and work function engineering have been proposed [24]. However, they are not very functional and can't satisfy ITRS requests very well [25].

In this work the use of source pocket doping and a material with lower work function near the channel-source interface creates band bending and on current increase. Utilizing HfO_2 with high-K dielectric in the source side, improves the coupling of the gate to the source-body junction, which results in the increase of on-state current [24]. For significant increase of on-current in the device a thin MOSFET has embedded underneath the channel. In addition, using low-K dielectric gate material on the drain side

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reduces gate to drain capacitance [24]. Abovementioned techniques are incorporated in our proposed structure (PTM-FET) and it results in improved transconductance (g_m), unity gain frequency (f_T), gain bandwidth product (GBP) and parasitic capacitances compared to DW HGD SP TFET structure, a pre-optimized device which has been published recently [24].

The remaining of this work is divided into three sections. In Section 2 we present a schematic cross section view of the proposed structure and DW HGD SP TFET device with related parameters. In Section 3, the simulated and extracted results are illustrated. In the last section, we explain comprehensive conclusion for the presented study.

2. PTM-FET device design

The main aim of our design is on-state current enhancement of a TFET. Fig. 1(a–b) illustrates a cross-sectional view of DW HGD SP TFET and the proposed structure i.e. PTM-FET. For this, we considered DW HGD SP TFET, a device in which different techniques like workfunction engineering, doping engineering and hetero gate dielectric applied in it to increase its on-state current. Although these techniques improved on current, but this current is not sufficient and it limits the device for many applications. In order to overcome this limitation, we locate a MOSFET device underneath the channel parallel to TFET device. Due to thermal injection mechanism in MOSFETs, current can be significantly improved in the structure. The paralleled TFET and MOSFET dimensions and physical parameters in the PTM-FET structure have optimized somehow that TFET device merits like low SS (<60 mV/dec) and low leakage current dominate in subthreshold region, while at high gate bias the structure benefits from high drain current of MOSFET structure. To control subthreshold characteristics and proper I_{ON}/I_{OFF} current ratio, MOSFET part has lower thickness. Also, all parameters related to both devices are presented in Table 1.

Fig. 2 which shows the proposed fabrication method for PTM-FET structure, it highlights the necessary modifications to come up with the new structure. The process start with a silicon wafer in step (1). Then by precise masking, phosphorous ion implantation with proper density is carried out in steps (2–4) to form n-type doping of drain, and channel regions. In step (5), Boron ion implanted to form source region. Afterward in step (6), annealing process in O_2 ambient is done or Oxygen is implanted to form SiO_2 as gate oxide. In step (7) HfO_2 is sputtered from a Hf target with O_2 modulation method, followed by ex-situ annealing [23,26]. Then gate metallization is done in step (8), according to the standard procedure which is utilized for a conventional MOSFET [6]. By rotation of silicon wafer in step (9), it is polished to be thinned enough. Then all steps of (2–8) with proper masking and resisting are done to form MOSFET part of the structure.

Table 1
Parameters for PTM-FET and DW HGD SP TFET structures.

Parameter	Values	
	PTM-FET	DW HGD SP TFET
Top and down oxide thickness (**Tox**)	2 nm	2 nm
Silicon channel thickness	10 nm	10 nm
TFET device thickness	7 nm	–
MOSFET device thickness	3 nm	–
Channel Length ($\mathbf{L_G}$)	50 nm	50 nm
Source/Drain Extension Length ($\mathbf{L_S}$, $\mathbf{L_D}$)	100 nm	100 nm
Source pocket Length ($\mathbf{L_P}$)	2 nm	2 nm
M1/**M3** Length	35 nm	35 nm
M2/**M4** Length	15 nm	15 nm
M5 Length	50 nm	–
M1/**M4** workfunction	4.6 eV	4.6 eV
M2/**M5** workfunction	4.0 eV	4.0 eV
M3 workfunction	4.8 eV	–
Channel doping (n-type)	1e17 cm^{-3}	1e17 cm^{-3}
Channel doping (p-type)	6e19 cm^{-3}	–
Source pocket doping (n-type)	5e19 cm^{-3}	5e19 cm^{-3}
Source doping (p-type)	1e20 cm^{-3}	1e20 cm^{-3}
Source doping (n-type)	1e20 cm^{-3}	–
Drain doping (n-type)	5e18 cm^{-3}	5e18 cm^{-3}

To simulate and examine the different electrical characteristics of abovementioned devices, 2-D ATLAS device simulator was used. In this work, we used Fermi-Dirac distribution function model. Nonlocal band to band tunneling applied to model carrier tunneling. SRH and Auger models were used to consider generation/recombination. BGN model accounted for applying doping dependence of band gap in simulations. We also considered the low field mobility model as suggested in Ref. [27]. To consider leakage current from source to drain or vice versa, nonlocal band to band tunneling models is used. It is worth noting that activating more than one quantum tunneling model in the ATLAS is not suggested and so did not take the gate leakage current into account. To calculate band to band tunneling in TFET devices, nonlocal BTBT model is mostly recommended since this model more accurately takes the spatial variation of energy bands into account. Local BTBT models are extensively used in analytical modeling and generation-recombination calculation at each point in the device since this model is solely based on field value at that point [27]. In order to show the reliability of the models used in this work, we obtained similar transfer characteristics with Ref. [28], which was previously calibrated against an IBM experimental data [29], as shown in the Fig. 3.

3. Results and discussion

This section investigates the reliability of the PTM-FET in terms of both DC and AC electrical performances, comprehensively.

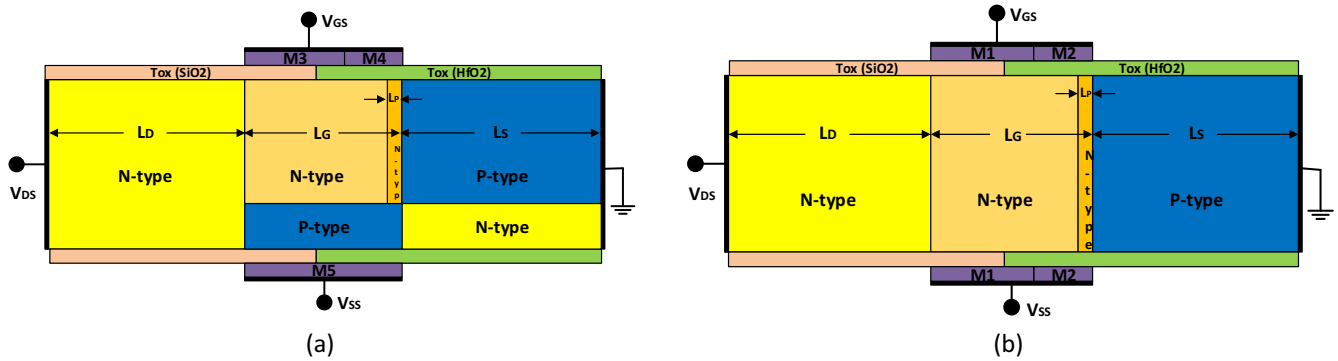

Fig. 1. Cross section view of: (a) PTM-FET and (b) DW HGD SP TFET structures.

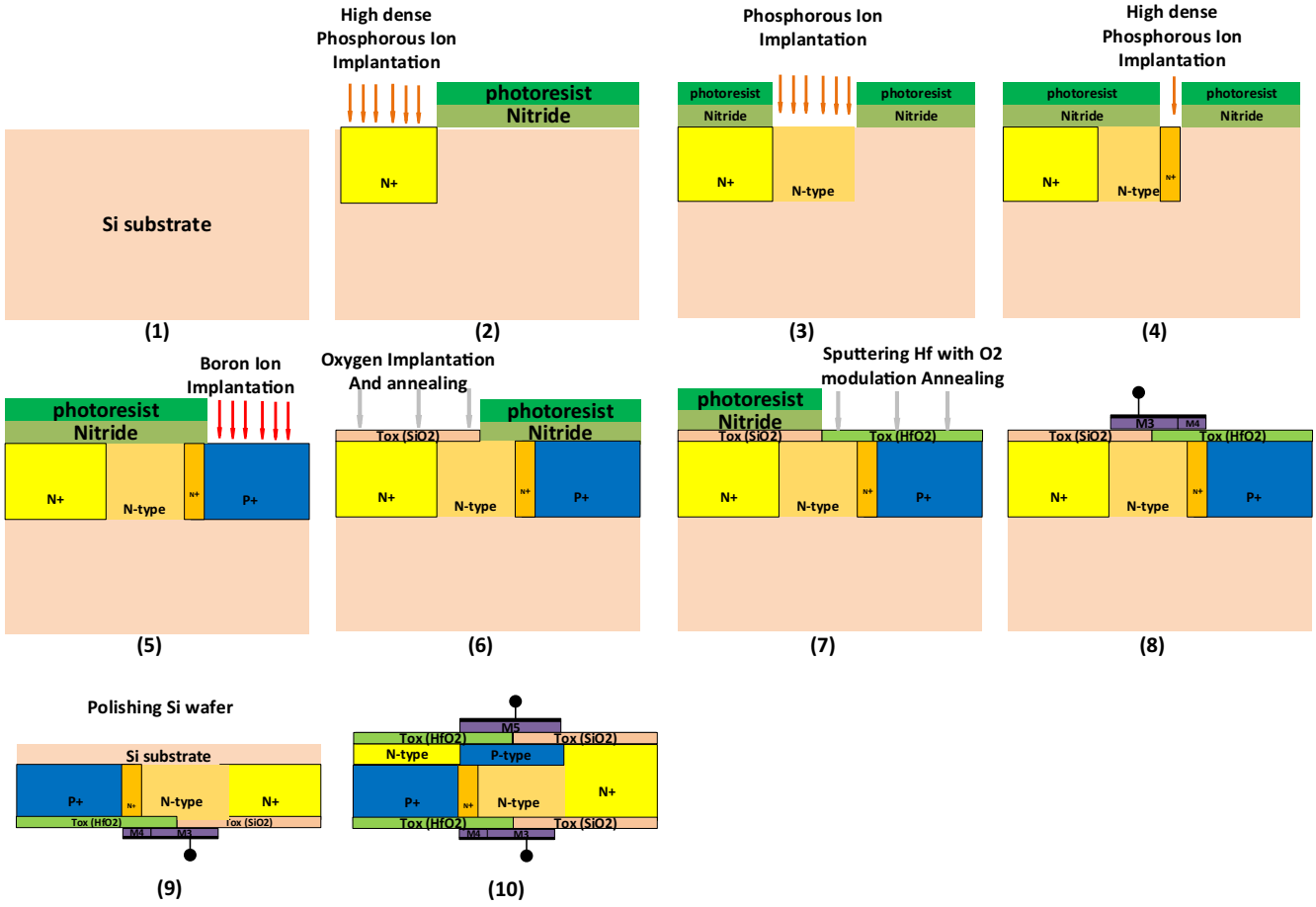

Fig. 2. Proposed fabrication process for PTM-FET structure.

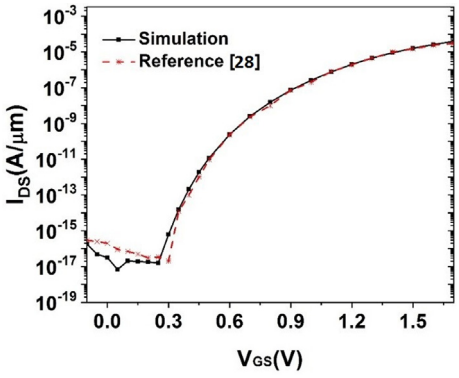

Fig. 3. Calibration of TCAD simulator against data taken from Ref. [28] at V_{DS} = 1.0 V.

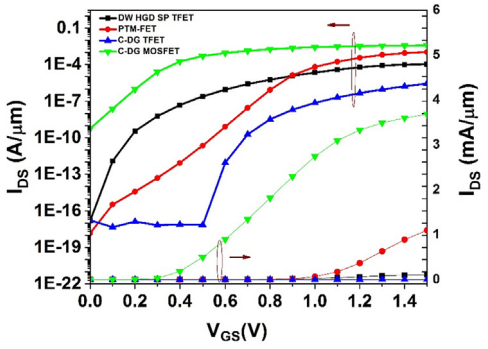

Fig. 4. Transfer characteristics of the DW HGD SP TFET, PTM-FET, C-DG MOSFET and C-DG TFET in logarithmic (left axis) and linear (right) view at V_{DS} = 1.0 V.

3.1. DC figures of merit

Fig. 4, shows transfer characteristics of DW HGD SP TFET, PTM-FET along with a conventional double gate TFET (C-DG TFET) and a conventional double gate MOSFET (C-DG MOSFET) with optimized characteristics based on their related parameters in Table 1. It should be noted that for conventional devices, we used SiO_2 as oxide and the gates workfunction of C-DG TFET are assumed 4.0 eV in the optimum condition of parameters in Table 1. According to this figure both off-state and on-state currents in PTM-FET is better than DW HGD SP TFET. Better drive current is related to MOSFET part at the bottom of PTM-FET device. It is obtained in this figure that at nonlinear subthreshold regime of the proposed device, the point subthreshold swing (SS_{point}) which is measured at V_{GS} = 0.0 V, is higher than its TFET counterparts. The measured value is SS_{point} = 43 mV/Dec (<60 mV/dec). This shows PTM-FET still benefits this advantage of TFET devices. The reason of subthreshold degradation compared to DW HGD SP TFET is related to an inherent parallel MOSFET in the proposed structure. Based on this figure, as it is clear the C-DG TFET has very low drive current, while C-DG MOSFET has weak subthreshold characteristics which it singly cannot satisfy the demand of high I_{ON}/I_{OFF} current ratio. For this, to have fair comparison among the characteristics of the devices, we only consider the performance of DW HGD SP

TFET, PTM-FET structures and C-DG TFET in the following discussions thereafter.

For a better understanding the reason behind electrical behavior of the proposed structure, Fig. 5 illustrates the energy band diagrams for the proposed device and its counterparts which were taken by two cutlines along the top and bottom of the active region. Since, the potential barrier widths (Fig. 5(a)) and height (Fig. 5(b)) in energy diagram of PTM-FET are more than DW HGD SP TFET and C-DG TFET, so electron transition is limited in this device. For this, we expect off-current in PTM-FET becomes less than its counterparts, as Fig. 6 compares current density of three devices under study. Furthermore, a vertical cutline is also considered through the source side of the gate edge (lateral position = 150 nm in Fig. 6) down to the bottom of the channel and then the potential and electron concentration profiles of three devices are extracted at equilibrium condition, according to the Fig. 7. Based on this figure, since the potential at the bottom of the channel increases, this leads to increase of electron concentration in the channel of MOSFET part of PTM-FET which is desired to be reduced to control the leakage current in this device.

Transconductance (g_m) which shows the rate of change in drain current with respect to the gate voltage, is defined as [30]:

$$g_m = \frac{dI_{ds}}{dV_{gs}} \tag{1}$$

Fig. 8 compares the transconductance of three considered devices. As it is clear, PTM-FET has g_m value much higher than DW HGD SP TFET and C-DG TFET. In fact, drain current enhancement shows its positive effect in g_m parameter. Because g_m has effective role in RF gains and unity gain frequency [24], it is expected that our proposed device has better RF performance compared to its counterparts.

Fig. 9 depicts output characteristics of three devices under study. According to this figure PTM-FET has significant drive current and it enters into saturation region at lower drain voltages. Therefore, this device can also be excellent candidate for analogue applications. Tunneling injection mechanism in DW HGD SP TFET and C-DG TFET, has limited their drive current. Slight increase of the drain current at voltages up to 0.6 V in DW HGD SP TFET is another drawback and it delays saturation regime of this device compared PTM-FET. In fact, at V_{GS} = 1.5 V the lucky electrons which have tunneled from source-channel junction, will face channel-drain barrier. At V_{DS} > 0.6 V this barrier becomes low enough to let the electrons pass the channel and current flows in this device.

At the saturation region, it is seen that three devices have slope at their output characteristics and a drain current increase is caused by associated drain voltage increase. Tangents to the characteristics at large voltages extrapolate backward to intercept the voltage axis at a voltage called the Early voltage, often denoted by the symbol V_A and in MOSFETs it reflects "channel-length modulation" which is among short channel effects. This parameter is very important in analogue applications [30]. The calculated Early voltage for PTM-FET and DW HGD SP TFET are −20.2 V and −6.71 V respectively. Thus, the early voltage is almost three times larger in the proposed device compared to DW HGD SP TFET.

Drain Induced Barrier Lowering (DIBL) is a short channel effect which considers drain voltage effect on the lowering of the conduction band of channel. This problematic effect should be reduced, because it leads to leakage current increase and undesired threshold voltage decrease. In order to consider DIBL effect in devices, we use the following relation:

$$DIBL = \frac{V_{g1} - V_{g2}}{V_{DS2} - V_{DS1}} \tag{2}$$

where V_{g1} and V_{g2} are the gate voltages corresponding to drain currents of $I_{DS} = 7 \times 10^{-5}$ A at V_{DS1} = 1.0 V and V_{DS2} = 2.0 V, respectively. It should be noted that the mentioned drain current value is quite optional and we chose it according to device characteristics. According to Table 2, PTM-FET devices is more persistence against this short channel effect and the embedded MOSFET with heavy doping in the channel, improved this phenomenon. In fact, heavy doping of the channel reduces drain control over the channel or at least more effort is needed to affect the channel region.

3.2. AC figures of merit

In the following we are going to point to some preferences of our device that is a figure of merit in RF performance. Maximum transducer power gain is a very important parameter in RF applications [31]. As it is observed from Fig. 10, the PTM-FET device has presented much more power gain than the DW HGD SP TFET device at this range of frequency while it is comparable with C-DG TFET.

Unilateral power gain is another RF parameter which can be stated as [8]:

$$U = \frac{|y_{22}|^2}{4\mathrm{Re}(y_{11})\mathrm{Re}(y_{22})} \tag{3}$$

where y_{ij} denotes elements of the admittance matrix. For instance, $Re(y_{22})$ means output conductance. As Fig. 11 indicates, this parameter is less for the proposed structure compared with its counterparts. Therefore, the proposed structure may have more power according to the above relation.

Gain bandwidth product (GBP) is also a figure of merit in RF, which is calculated as [24]:

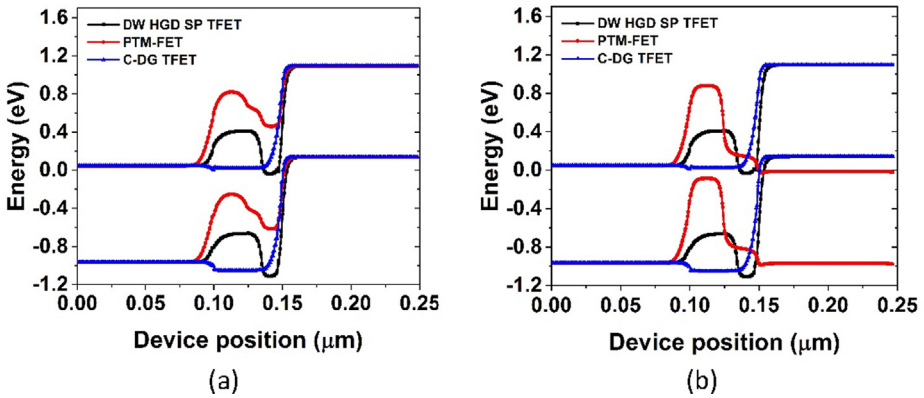

Fig. 5. Energy band profile of the three structures at: (a) top of the channel and (b) bottom of the channel at equilibrium.

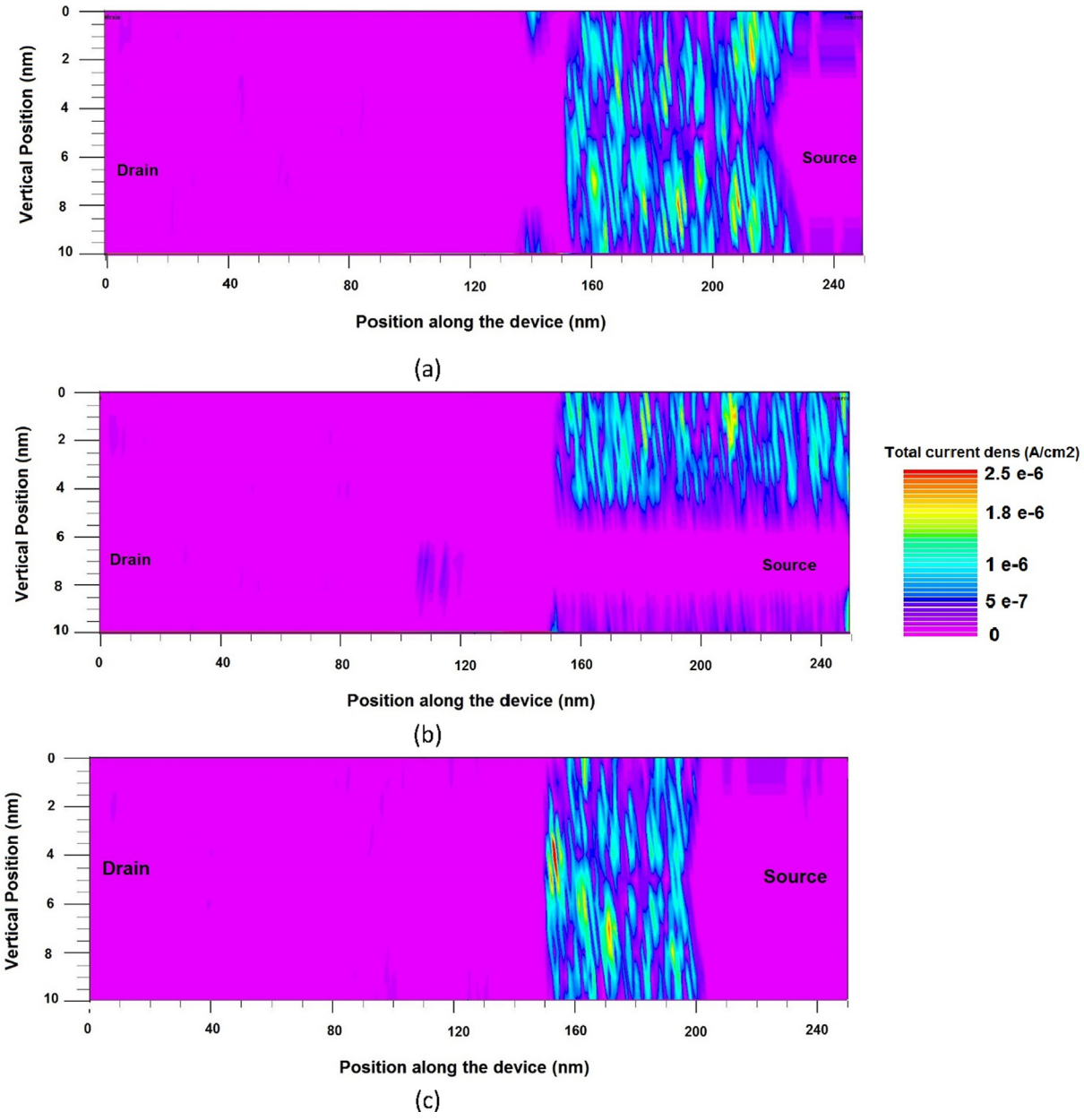

Fig. 6. Total current density contours of (a) DW HGD SP TFET, (c) PTM-FET and (c) C-DG TFET at equilibrium.

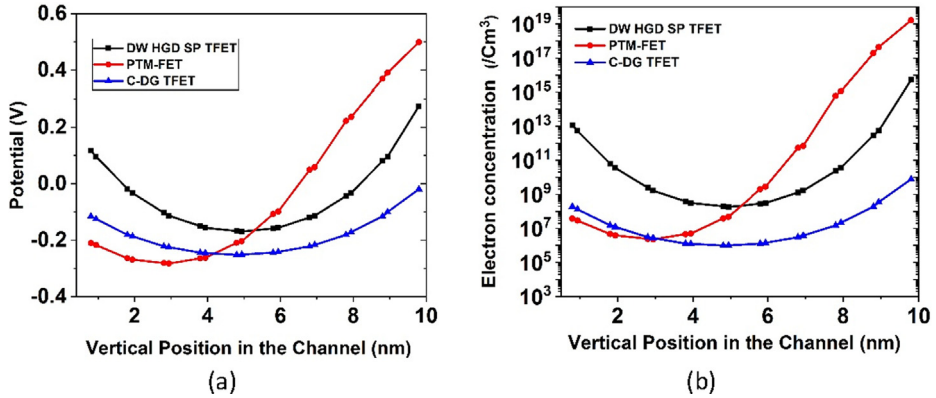

Fig. 7. (a) Electrostatic potential and (b) electron concentration profiles of DW HGD SP TFET, PTM-FET and C-DG TFET along the channel thickness, at equilibrium condition.

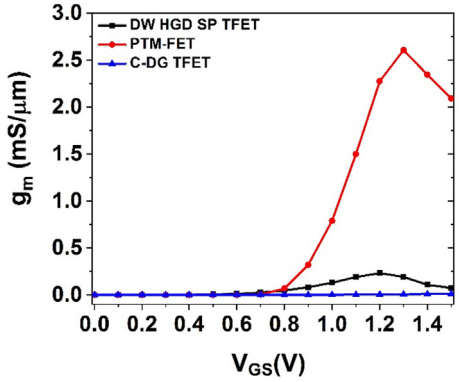

Fig. 8. Transconductance in DW HGD SP TFET, PTM-FET and C-DG TFET at V_{DS} = 1.0 V.

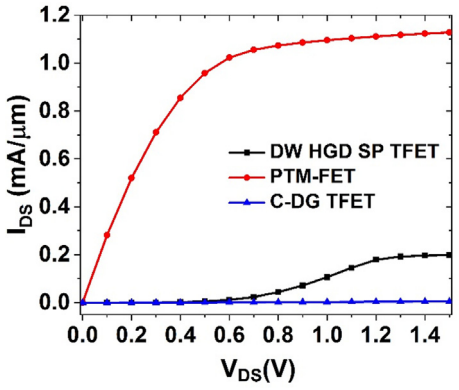

Fig. 9. Output characteristics of DW HGD SP TFET, PTM-FET and C-DG TFET at V_{GS} = 1.5 V.

Table 2
DIBL value of DW HGD SP TFET, PTM-FET and C-DG TFET devices.

	V_{gs1} (V)	V_{gs2} (V)	DIBL (mV/V)
PTM-FET	1.0047	0.9848	19.8
DW HGD SP TFET	1.241	1.213	27.8
C-DG TFET	2.60174	2.05999	541.75

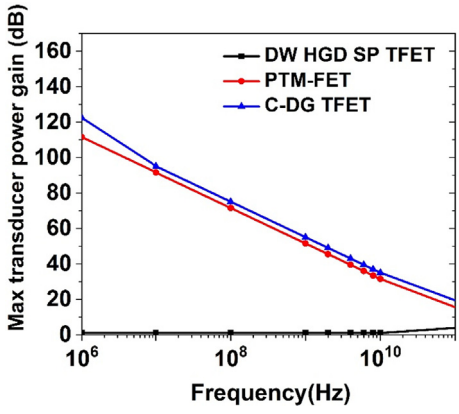

Fig. 10. Maximum transducer power gain as a function frequency for the three devices at V_{GS} = V_{DS} = 1.0 V.

$$GBP = \frac{g_m}{(20\pi * C_{gd})} \tag{4}$$

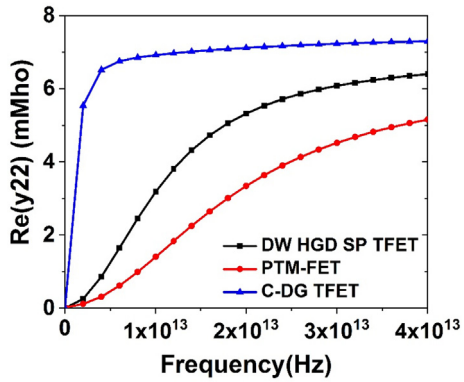

Fig. 11. Output conductance as a function of frequency for three devices at bias V_{GS} = V_{DS} = 1.0 V.

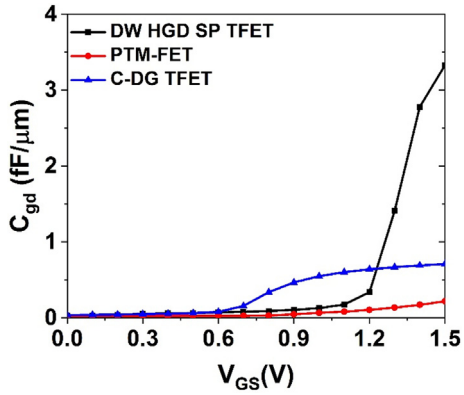

Fig. 12. Gate-drain capacitance as a function of gate-source voltage for three devices at bias V_{DS} = 1.0 V and f = 1 MHz.

where g_m and C_{gd} are transconductance and gate-drain capacitance. Fig. 12 indicates C_{gd} of three devices as a function of gate voltage at f = 1 MHz. The lower C_{gd} and higher g_m in PTM-FET confirm the higher GBP for this device compared to its counterparts in the Fig. 13.

Unity gain frequency (f_T) is the frequency at which the short circuit current gain becomes unity. The more f_T means a better transistor in RF applications. It is calculated by the following relation [24]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{5}$$

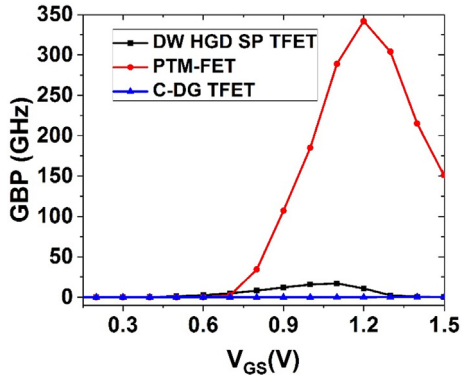

Fig. 13. Gain bandwidth product (GBP) as a function of gate-source voltage for three devices at bias V_{DS} = 1.0 V and f = 1 MHz.

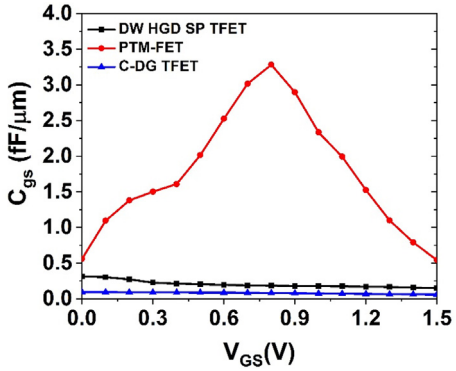

Fig. 14. Gate-source capacitance as a function of gate-source voltage for three devices at bias V_{DS} = 1.0 V and f = 1 MHz.

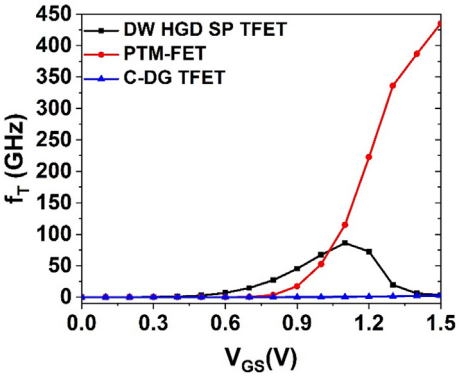

Fig. 15. Unity gain frequency as a function of gate-source voltage for three devices at bias V_{DS} = 1.0 V and f = 1 MHz.

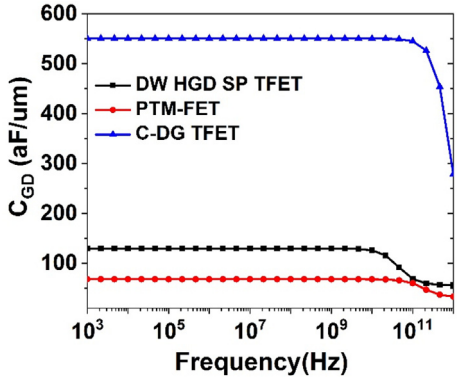

Fig. 16. Gate-drain capacitance as a function of frequency for three devices at bias V_{DS} = V_{GS} = 1.0 V.

where g_m, C_{gs} and C_{gd} are transconductance, gate-source and gate-drain capacitances, respectively. Even though PTM-FET has higher C_{gs} in Fig. 14, it has higher unity gain frequency at V_{gs} > 1.0 V according to Fig. 15. This enhancement is related to much better gm values in PTM-FET device compared to DW HGD SP TFET and C-DG TFET devices.

To evaluate the switching speed of the devices, gate-drain and substrate-drain capacitances were simulated at bias conditions of V_{GS} = V_{DS} = 1.0 V as shown in Figs. 16 and 17, respectively. In all cases, parasitic capacitances for PTM-FET are lower. As a result, delay time and dynamic power dissipation is improved in our proposed device.

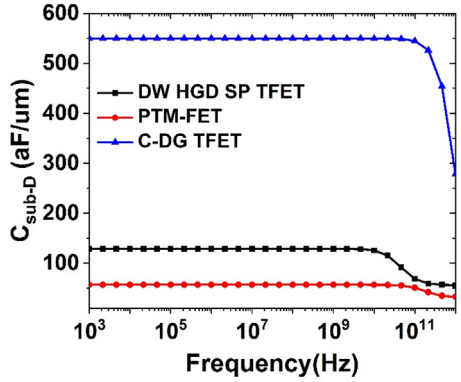

Fig. 17. Substrate-drain capacitance as a function of frequency for three devices at bias V_{DS} = V_{GS} = 1.0 V.

4. Conclusion

In this paper a PTM-FET device was proposed comprised of 70% TFET and 30% MOSFET in its silicon film thickness. We observed that the on-state current was enhanced significantly, due to changing of current injection mechanism from tunneling (nonthermal) to thermionic emission. Moreover, transconductance and RF parameters related to it like gain bandwidth product and unity gain frequency were improved compared to DW HGD SP TFET. Our proposed device was persistence against short channel effects including DIBL and channel length modulation. Due to the fact that PTM-FET showed significant improvement in RF gains, lower parasitic capacitance, higher I_{on}/I_{off} current ratio and SS less than 60 mV/dec, this device can be a serious candidate for low power, high performance and system on chip applications.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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