Compact Model for Flexible Ion-Sensitive Field-Effect Transistor

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***Abstract*— This paper presents the theoretical modelling, and simulation of bending effects on an ion-sensitive field-effect transistor (ISFET), towards futuristic bendable integrated circuits and microsystems for biomedical applications. Based on variations of threshold voltage and drain current under different bending conditions and orientations of the channel of the device, the bendable ISFET macro-model has been implemented in Verilog-A, and compiled into the Cadence environment. The effects of bending on the behaviour of the device have been simulated over a user-defined range of pH, and sensitivities in a standard 0.18-µm CMOS technology. It has been found that the transfer curves (I_D-V_G) of ISFET vary up to 4.46% for tensile and up to 5.15% for compressive bending stress at pH 2, and up to 4.99% for tensile and 5.61% for compressive bending stress at pH 12 with respect to its planar counterpart, while the sensitivity of the device has been found to remain the same irrespectively of the bending stress. The proposed model has been validated by comparing the results with those obtained by other macro-models and experimental results in literature.**

Keywords— Bendable Electronics, ISFET, Compact Device Modelling

I. INTRODUCTION

Less than forty years ago medicine and nanofabrication were unrelated to one another. Nowadays, these two are indispensable partners in bio-medicine. One of the numerous examples towards this direction is the invention of the Ion Sensitive Field-Effect Transistor (ISFET) in 1970 [1]. One of the promising advantages of ISFETs is their implementation using standard CMOS processes and their large-scale integration with readout circuit topologies and compensation techniques. With CMOS transistors scaling-down from micrometer to nanometer regime, their performance has improved and so has the cost and power consumption. During this transformation to nanotechnology, various fabrication techniques were used to enhance the performance [2, 3]. Among them the strain engineering is at the forefront as it leads to enhanced carriers' mobility [4]. ISFET-based microsystems have also benefited from this progress and show promising results for numerous applications [5, 6]. However, traditional CMOS devices are fabricated using rigid and planar silicon substrate with thickness ranging from 200 µm to 1 mm and this limits their usage in the applications where flexibility of devices is not required.

Bendability and conformability of electronic devices opens a new range of applications, in particular for biomedical purposes [7]. New challenges arise when external stress is applied on MOSFETs fabricated on ultra-thin Si chips. CMOS electronic devices depend largely on stress-induced changes in semiconductor materials. Therefore, stress analysis becomes essential for investigations on bending strength and stiffness of the substrate, and performance of devices in terms of stability, speed, and response, which can be influenced either constructively or destructively depending on the stress conditions [8]. To realize futuristic high-performance Si-based bendable sensing microsystems based on ISFET technology that could work reliably under both planar and bending conditions, there is need to consider various stress conditions in the design process. The theoretical modelling, and the analysis of flexible integrated circuits (ICs) using computer-aided-design (CAD) tools is essential for IC designers, since it will enable the understanding of the behavior of devices, and thus the response of integrated circuits, under different bending stresses.

However, a few attempts have been made to include the effects of externally applied stress on devices and circuit performance in models using CAD tools [9]. Recently, we proposed high-performance bendable ultrathin chips complimented with compact models of NMOS and PMOS implemented in Verilog-A and compiled in Cadence environment as a promising approach to achieve this goal [10, 11]. As a step forward towards flexible ISFET-based sensing microsystems, illustrated in Fig. 1, this paper extends our previous work to provide a new compact model of bendable ISFET, which will allow us to predict the electrical behavior of sensor under arbitrary bending conditions. In this regard, there is need to evaluate the changes in performance of bendable ISFETs as bending induced stresses may lead to offsets, which eventually influence their sensitivity.

This paper is organized as follows: The formulation of the proposed model is presented in Section II. The simulated results and the comparison between our model and previously reported experimental data from literature are given in Section III. Finally, the key outcomes are summarized in Section IV.

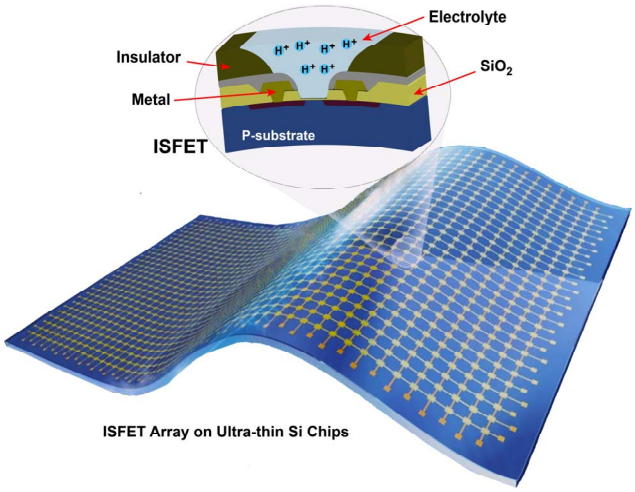

Figure 1: The concept of bendable ISFET array on the ultra-thin Si chips.

II. BENDABLE CMOS ISFET MODEL

A. Overview

ISFET consists of a pH-sensitive layer of metal oxide (usually Si_3N_4, or Ta_2O_5) deposited on top of a MOSFET structure. The device operation is similar to a MOSFET device, described initially by Bergveld and Sibbald [12]. ISFET pH-sensitivity is theoretically defined with a combination of models describing the formation of the electrical double-layer (EDL) at the surface of the metal oxide, and the proton adsorption. Each metal oxide deposited as the pH-sensitive layer shows a different sensitivity to pH, which can be expressed as a function of the double layer capacitance and the intrinsic buffer capacity of the oxide.

The most common approach to describe metal oxides' charging mechanism when immersed into a solution, and to calculate the surface charge density and intrinsic buffer capacity, uses the site-dissociation model introduced by Yates et al. [13]. The oxide surface charge density (σ_0) after the introduction of the electrolyte is given by:

$$\sigma_0 = q \cdot N_S \left(\frac{a_{H_S^+}^2 - K_a \cdot K_b}{K_a \cdot K_b + K_b \cdot a_{H_S^+} \cdot a_{H_S^+}^2} \right) \quad (1)$$

where q is the electronic charge, N_S is the density of surface sites, $a_{H_S^+}$ is the activity of hydrogen ions, and K_a and K_b are the intrinsic dissociation constants, which are given by:

$$K_a = \frac{1}{10^{pK_a}} \quad (2)$$

In colloid science, the diffuse model of the double layer structure is commonly described by the Gouy-Chapman-Stern model as a function of the ionic strength. The charge in the diffuse layer is given by [14]:

$$\sigma_d = -(8kT\varepsilon\varepsilon_0 n^0)^{1/2} sinh\left(\frac{zq\Phi_{GCd}}{2kT}\right) = -C_{DL}V_{chem} = -\sigma_0 \quad (3)$$

where ε is the dielectric constant of the solution, ε_0 is the permittivity of free space, n^0 is the bulk density of electrolyte ions, and Φ_{GCd} is the potential at the plane of the diffuse layer which has the minimum distance from the surface of the metal oxide. C_{DL} is the double layer capacitance including the diffuse, and inner and outer Helmholtz layer, and V_{chem} is the potential across the double layer capacitance. Differentiation of Eq. (3) gives the series capacitance of the diffuse layer and the outer Helmholtz layer:

$$C_D = \frac{\partial \sigma_d}{\partial \Phi_{GCd}} = \frac{\left(\frac{2\varepsilon\varepsilon_0 z^2 q^2 n^0}{kT}\right)^{1/2} cosh\left(\frac{zq\Phi_{GCd}}{2kT}\right)}{1+\left(\frac{x_{gcd}}{\varepsilon\varepsilon_0}\right)\left(\frac{2\varepsilon\varepsilon_0 z^2 q^2 n^0}{kT}\right)^{1/2} cosh\left(\frac{zq\Phi_{GCd}}{2kT}\right)} \quad (4)$$

where x_{gcd} is the distance in which the potential is Φ_{GCd}. Because $x_{gcd} \ll$, Eq. (4) can be approximated with the equation:

$$C_D = \left(\frac{2\varepsilon\varepsilon_0 z^2 q^2 n^0}{kT}\right)^{1/2} cosh\left(\frac{zq\Phi_{GCd}}{2kT}\right) \quad (5)$$

Based on Graham's theory of the development of the double layer [15] there is another layer termed as inner Helmholtz layer, which effectively creates another capacitance in series with C_D. The inner Helmholtz unit-area capacitance can be described using the following equation:

$$C_{IHP} = \frac{V_{OHP} - V_{IHP}}{Q_{OHP}} \quad (6)$$

where V_{OHP} is electrostatic potential of the outer Helmholtz plane, V_{IHP} is electrostatic potential of the inner Helmholtz plane, and Q_{OHP} is the charge within the outer Helmholtz plane. In [16] an equation based on Eq. (6) was derived, which is also used in the presented model:

$$C_{IHP} = \frac{\varepsilon_{OHP} \cdot \varepsilon_{IHP}}{\varepsilon_{OHP} \cdot d_{IHP} + \varepsilon_{IHP} \cdot d_{OHP}} \quad (7)$$

where ε_{OHP} and ε_{IHP} are the outer and inner Helmholtz plane dielectric constants, respectively, and d_{OHP} and d_{IHP} are the distances between the metal-oxide and the outer and inner Helmholtz planes, respectively. Therefore, the total double-layer capacitance can be written as:

$$C_{DL} = \frac{C_D \cdot C_{IHP}}{C_D + C_{IHP}} \quad (8)$$

B. Bendable ISFET Model Formulation

Several physico-chemical models have been developed using CAD tools since the introduction of ISFET [17-19]. To this goal, these models have considered ISFET as two uncoupled stages. One stage representing the behavior at the electrolyte-oxide interface, and a second stage representing the electronic behavior of the device (MOSFET). However, none of them has included the effects of external mechanical bending into the simulations.

The proposed model has been implemented in a standard 0.18-µm CMOS technology, where the Si_3N_4 is considered for pH-sensitive metal oxide. However, the model can be simply extended to other materials by changing the values of N_S, K_a and K_b. The surface of Si_3N_4 bears both silylamine (Si-NH_2) and silanol (Si-O-H) sites. The equilibrium reactions between the electrolytic solution and the surface of Si_3N_4 are:

$$Si - OH_2^+ + H_2O \leftrightarrow Si - OH + H_3O^+$$

$$Si - OH + H_2O \leftrightarrow Si - O^- + H_3O^+$$

and

$$Si - NH_3^+ + H_2O \leftrightarrow Si - NH_2 + H_3O^+$$

The values that were used in the present model for pK_a, and pK_b of silanol sites are 6.2, and 2.5, respectively. The used pK value for silylamine sites is 10. The total surface density for silanol and silylamine sites is 10^{15} cm^{-2} [20].

The condition of charge neutrality of the electrochemical stage of ISFET is given by:

$$\sigma_d + \sigma_0 = 0 \tag{9}$$

Therefore, by using Eq. (5) and (7) to calculate Eq. (8), and Eq. (1), (3), and (8), we obtain the electrolyte-oxide surface potential as a function of the pH and the surface potential itself:

$$V_{chem} = N_{Silanol} \cdot f_1(pH, V_{chem}) + N_{Silylamine} \cdot f_2(pH, V_{chem}) \tag{10}$$

The electronic stage of the ISFET is modelled by using our previously reported bendable MOSFETs [10]. Based on the theoretical concepts and experimental results in [10], and the threshold voltage and mobility parameters extracted from BSIM4 the modified drain-current and threshold-voltage equations of the MOSFET shown below were implemented in Verilog-A and simulated in Cadence environment.

$$I_{D(stress)} = I_{D_0}\left(1 \pm \Pi_{I_D} . \sigma_{I_D}\right) \tag{11}$$

$$V_{th(stress)} = V_{th_0}\left(1 \pm \Pi_{V_{th}} . \sigma_{V_{th}}\right) \tag{12}$$

where I_{D_0}, V_{th_0}, $I_{D(stress)}$, $V_{th(stress)}$, and Π_{I_D}, $\Pi_{V_{th}}$ are the drain current and threshold voltage of the transistor under planar conditions, and the drain current and threshold voltage under bending conditions, and the piezoresistive coefficients proportional to the drain-current and threshold voltage, respectively.

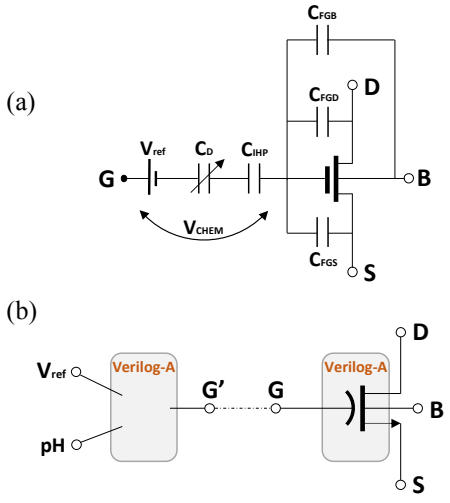

Figure 2: (a) ISFET equivalent electronic circuit including the floating gate-to-bulk (C_{FGB}), floating gate-to-drain (C_{FGD}), and floating gate-to-source (C_{FGS}) capacitances, and (b) Block diagram circuit of ISFET including the external connections.

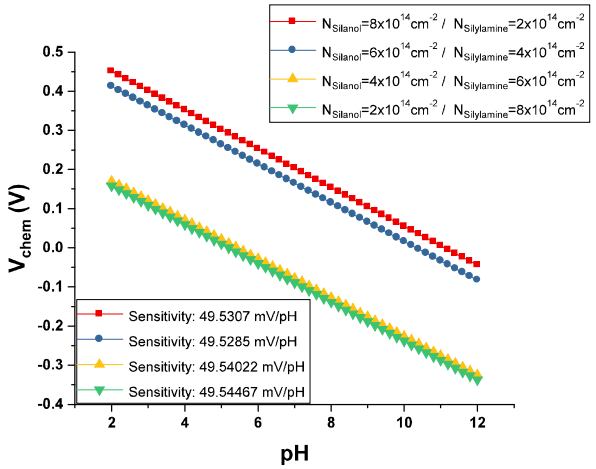

Figure 3: Simulated sensitivities of ISFET at different ratios of silanol and silylamine surface densities.

III. Simulation Results and Discussion

The electrochemical stage of ISFET was modelled using Eq. (8) and (10), while the electronic stage using Eq. (11) and (12), compiled in Cadence environment. The equivalent electronic circuit of ISFET structure is illustrated in Fig. 2(a), and the outer connections are shown in Fig. 2(b), where Vref, pH, G', G, D, B, and S stand for voltage of the reference electrode, the independent applied pH source modelled as a voltage source, the connection of the electrochemical stage towards the gate of the bendable MOSFET model, and the gate, drain, bulk, and source of MOSFET, respectively. The bendable ISFET macromodel can be used to simulate the behavior of ISFET-based microsystems that will operate in a wide range of pH values and under various bending and planar conditions.

The simulation results have been compared with experimental data from the literature [17], and with our previously validated bendable MOSFET model results [10]. Fig. 3 shows the shift in sensitivity of the device due to the offset depending on the ratios of surface densities of silylamine and silanol binding sites. The simulation results point out a positive shift in the sensitivity as a result of an increase of the surface density of silylamine sites, as has been reported in literature [21]. Fig. 4 shows the simulated transfer characteristics of an ISFET device in planar mode. The simulated results show a good matching with the reported

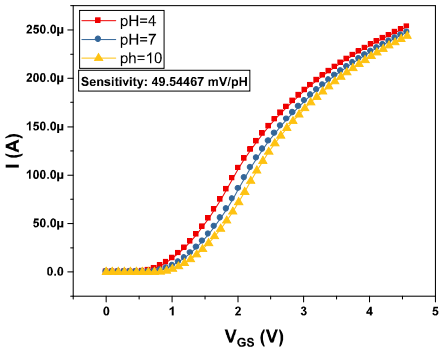

Figure 4: Plots showing the simulated data using the proposed ISFET model in planar mode matching the experimental results in [17].

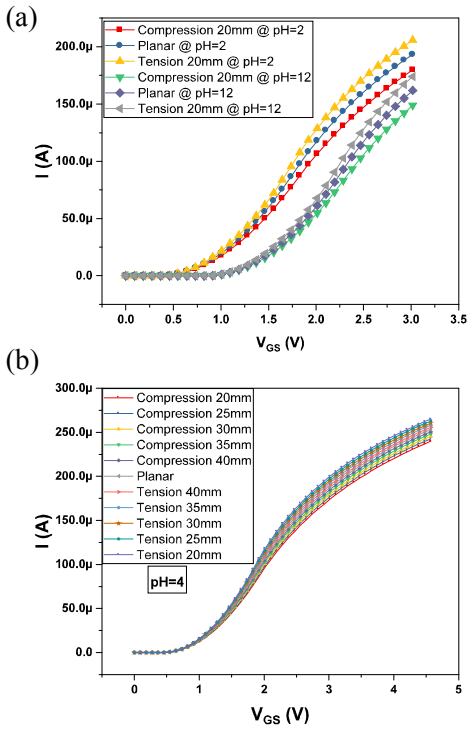

Figure 5: Simulated transfer characteristics at: (a) pH 2 and 12 under 20mm compressive and tensile bending stress, and (b) pH 4 under different compressive and tensile bending stress (from 20mm to 40mm).

experimental data in literature under the same pH values, and bias conditions [17]. Finally, Fig. 5(a) shows the simulated results at pH 2 and 12 under compressive (20mm bending radius) and tensile (20mm bending radius) bending stress, at the same bias conditions as used in Fig. 3. Fig. 5(b) shows the different transfer characteristics at a fixed pH 4, and under different compressive and tensile bending conditions.

IV. Conclusion and Outlook

This work proposed a method of simulating bendable ISFET devices under various bending conditions using Cadence environment for futuristic high-performance applications where the overall size of the system could be below 100-µm. Such futuristic biomedical systems could revolutionize applications like brain recording and point-of-care testing and diagnosis due to their small size and structural conformability. The simulated results confirm a good agreement with experimental data extracted from literature under planar condition. During bending conditions the simulations show shift in drain-current up to 4.46% for tensile and up to 5.15% for compressive bending stress at pH 2, and an up to 4.99% for tensile and up to 5.61% for compressive bending stress at pH 12, with respect to its planar counterpart. As a future work, the model will be extended in order to simulate non-ideal behaviors of ISFETs in weak-inversion region under different bending conditions, and will be experimentally validated with our fabricated devices.

V. Acknowledgments

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