



Tan, C., Chen, Q., Zhou, K. and Zhang, L. (2019) A simple high-performance current control strategy for V2G three-phase four-leg inverter with LCL filter. IEEE Transactions on Transportation Electrification, (doi:10.1109/TTE.2019.2936684).

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A Simple High-Performance Current Control Strategy for V2G Three-phase Four-leg Inverter with LCL Filter

Cuilan Tan, Qihong Chen, *Member, IEEE*, Keliang Zhou, *Senior Member, IEEE*, Liyan Zhang, *Member, IEEE*

Abstract—Electric vehicles (EVs) can behave as distributed energy storage devices for providing on-demand smart grid support service, that is an emerging Vehicle-to-Grid (V2G) technology. A high-performance and easy-implementation current control strategy for V2G Three-phase four-leg inverter with LCL filter is proposed. It consists of a deadbeat (DB) controller and a paralleled repetitive controller (RC). The DB controller is based on weighted average inductor current (WAIC) scheme, which simplifies the third-order LCL filter to be an equivalent 1st order L filter. The stability of the DB controlled inverter with the unmodelled system time delay is analyzed. DB controller is of very fast response and easy implementation, but is not immune to system time delay and various uncertainties. To overcome the disadvantages, a plug-in RC is added to reinforce the DB controller to remove harmonic distortion from the feed-in current in the presence of parameter uncertainties. A lab prototype of 10kW grid-connected three-phase four-leg inverter has been built up to validate the proposed current control strategy. The simulations and experiments are provided to demonstrate the validity of the proposed control strategy.

Index Terms—V2G, weighted average inductor current, three-phase four-leg inverter, deadbeat control, repetitive control, stability analysis.

I. INTRODUCTION

Vehicle-to-grid (V2G) technology allows electric vehicles (EVs) to act as distributed energy storage devices. It can provide smart grid support services by "valley filling" and "peak shaving" [1-4]. Fig. 1 shows a V2G application example, where the EVs can improve the efficiency, stability and economy of the grid[5, 6].

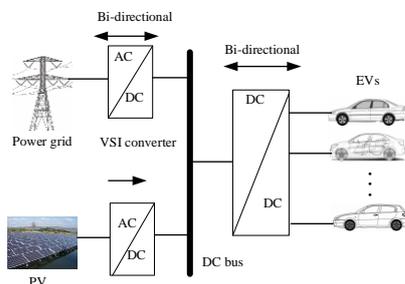


Fig. 1. V2G application system.

This work was partially supported by the National Natural Science Foundation of China under Grant 61673305, 61673306 and the National Key Research and Development Program of China under Grant 2017YFB0103001. (Corresponding author: Liyan Zhang.)

Cuilan Tan is with the Department of School of Automation, Wuhan University of Technology, Wuhan 430070, China, and with School of Physics and Information Engineering, Jiangnan University, Wuhan 430056, China (e-mail: xiaotanlan@126.com).

Three-phase four-leg inverters can be employed to interface the EVs with the grid. Compared with conventional three-phase three-wire or three-phase four-wire inverters, the fourth leg allows the neutral point voltage to be actively modified, and then enables the inverter to achieve high utilization of DC bus voltage and feed unbalanced loads, and so on. [7-10]. V2G converters not only are used to charge the EVs from the grid, but also can compensate unbalanced voltages on demand. Hence the four-leg topology is needed in V2G applications at costs of additional switches. It is a must to develop appropriate current control schemes for inverters to feed-in high quality currents in V2G applications. It is well known that the 3rd-order LCL filter enable the inverters to achieve much better high frequency current harmonics attenuation than 1st order L filter [11]. However, it might significantly increase the complexity of the analysis and synthesis of the current control methods for inverters[12]. Neglecting the high frequency filtering capacitor C, the 3rd-order system could be approximated to be a 1st-order system with the sum inductance of two inductors [13]. Hence, a very simple deadbeat (DB) control scheme can be developed for the inverters with the approximated L filter. However, such DB controlled inverters might not be able to feed high-quality current into the grid and has poor damping capability of resonance due to the omission of high frequency response of LCL filter [14]. Instead of ignoring the capacitor C, when a weighted average current value of the two inductors is employed as the feedback in the control loop[15], the 3rd order LCL filter is found to be equivalent to a 1st order L filter [16]. Therefore the weighted average inductor current (WAIC) based DB control scheme can be developed for inverters with LCL filter [17-19]. The WAIC based DB control scheme will significantly simplify the synthesis of the inverter current controller without any system performance and stability degradation. Since the WAIC based DB controller is based on accurate mathematical model, the DB control scheme cannot well remove periodic feed-in current error and harmonics under various uncertainties, also it might encounter instability caused by unmodelled time delay[14, 20].

This paper proposed a WAIC based DB control strategy combined with plug-in repetitive controller (RC) for V2G three-phase four-leg inverter with LCL filter. The stability of

Qihong Chen is a Professor with School of Automation, Wuhan University of Technology, Wuhan 430070, China (e-mail: chenqh@whut.edu.cn).

Keliang Zhou is a Senior Lecturer with James Watt School of Engineering at the University of Glasgow, Glasgow, G12 8QQ, United Kingdom (e-mail: keliang.zhou@glasgow.ac.uk).

Liyan Zhang is a Professor with School of Automation, Wuhan University of Technology, Wuhan 430070, China (e-mail: zlywhut@whut.edu.cn).

the DB controlled inverter with the impact of unmodelled system time delay is investigated to facilitate the control synthesis. The WAIC based DB control has fast dynamic response to the reference changes, but it can't track the reference accurately and can't suppress the harmonic effectively. As we know, the internal model principle (IMP) based RC [21, 22] can exactly track periodic reference signal or eliminate periodic disturbances. In order to eliminate the residual harmonic distortion and periodic tracking error from the fed-in current in the presence of parameter uncertainties, a plug-in phase-lead compensation RC is added to reinforce the DB controller. The highlights are as following: 1) WAIC based DB control strategy is applied to three-phase four-leg grid-tied inverter for V2G application, which can simplify the third-order of the system to be an equivalent first-order system. 2) the current control performance of the V2G system can be improved significantly in terms of easy implementation, high accuracy, low THD and good robustness. Simulations and experiments on a test rig of 10kW grid-tied inverter are executed to prove the high-performance of proposed strategy.

The remaining parts of the paper are arranged as follows: a mathematical model of V2G three-phase four-leg inverter

with LCL filter is established in Section II. The analysis and synthesis of the current control strategy is shown in Section III. Section IV gives simulation and experiment results of the proposed strategy. Section V provides the conclusion.

II. MODEL OF THE INVERTER

The topology of the grid-connected three-phase four-leg inverter with LCL filter is shown in Fig.2. The four legs (a, b, c, n) comprise of 8 IGBTs (Insulated Gate Bipolar Transistor) power electronic switches named as $Q_1 \sim Q_8$ in the topology. v_{ga} , v_{gb} and v_{gc} are grid voltages of three-phase, respectively. DC bus voltage is denoted as V_{dc} . i_{1j} , i_{2j} ($j=a, b, c$) are currents of the two inductances of corresponding phase, respectively. The voltages between point a, b, c, n, and the DC ground are denoted as v_a , v_b , v_c , v_n , respectively. The capacitor voltages of the three phases LCL filter are denoted as v_{ca} , v_{cb} , v_{cc} , respectively.

The proposed scheme comprises of a WAIC based DB controller and a paralleled plug-in RC for three-phase four-leg inverter. A 3D-SVM is used to convert the control outputs of the proposed controller into PWM signals for driving the IGBTs[23].

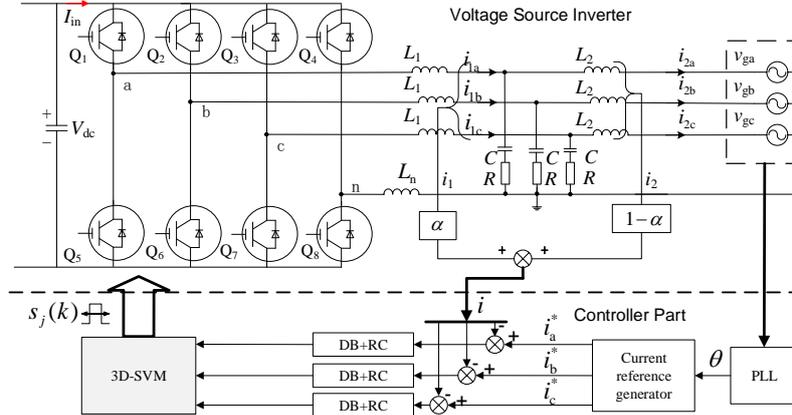


Fig. 2 Topology of four-leg VSI for V2G interface

A. Modelling of the Inverter

The mathematical model of the three-phase four-leg inverter shown in Fig. 2 can be obtained as

$$\begin{cases} L_1 \begin{bmatrix} \dot{i}_{1a} \\ \dot{i}_{1b} \\ \dot{i}_{1c} \end{bmatrix} + RC \begin{bmatrix} \dot{v}_{ca} \\ \dot{v}_{cb} \\ \dot{v}_{cc} \end{bmatrix} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \\ C \begin{bmatrix} \dot{v}_{ca} \\ \dot{v}_{cb} \\ \dot{v}_{cc} \end{bmatrix} = \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \end{bmatrix} - \begin{bmatrix} i_{2a} \\ i_{2b} \\ i_{2c} \end{bmatrix} \\ RC \begin{bmatrix} \dot{v}_{ca} \\ \dot{v}_{cb} \\ \dot{v}_{cc} \end{bmatrix} - L_2 \begin{bmatrix} \dot{i}_{2a} \\ \dot{i}_{2b} \\ \dot{i}_{2c} \end{bmatrix} = \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} - \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \end{cases} \quad (1)$$

Eq. (1) indicates that the three-phase four-leg inverter is decoupled into three separated single-phase inverter circuits [24].

B. Weighted Average Inductor Current Scheme

As shown in Fig. 3, the WAIC scheme is developed for each phase LCL filter to simplify the synthesis of the current controller, where $V_{gj}(s)$ and $V_i(s)$ are voltages of grid-side and inverter output side, respectively, the resistor R is used to damp the resonance, and the capacitor C is used to remove high frequency current.

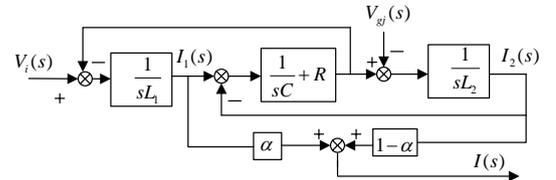


Fig. 3. Block diagram of each phase WAIC scheme.

The transfer functions from the inductor currents of the LCL filter to the inverter output voltage can be derived as

$$\begin{cases} \frac{I_1(s)}{V_i(s)} = \frac{Z_2 + Z_c}{Z_1 Z_2 + Z_1 Z_c + Z_2 Z_c} \\ \frac{I_2(s)}{V_i(s)} = \frac{Z_c}{Z_1 Z_2 + Z_1 Z_c + Z_2 Z_c} \end{cases} \quad (2)$$

where

$$\begin{cases} Z_1 = sL_1 \\ Z_2 = sL_2 \\ Z_c = 1/sC + R \end{cases} \quad (3)$$

Define $L = L_1 + L_2$ and the weighting factor $\alpha = L_1/L$, Eq. (2) can be rewritten into two 3rd order transfer functions as below

$$\begin{cases} \frac{I_1(s)}{V_i(s)} = \frac{(1-\alpha)LCs^2 + RCs + 1}{\alpha(1-\alpha)L^2Cs^3 + RCLs^2 + sL} \\ \frac{I_2(s)}{V_i(s)} = \frac{RCs + 1}{\alpha(1-\alpha)L^2Cs^3 + RCLs^2 + sL} \end{cases} \quad (4)$$

Let us define a weighted average inductor current as

$$I(s) = \alpha I_1(s) + (1-\alpha)I_2(s) \quad (5)$$

Substitute Eq. (4) into (5), we can get a first-order control plant $G_p(s)$ as below

$$G_p(s) = \frac{I(s)}{V_i(s)} = \frac{1}{sL} \quad (6)$$

Therefore, the third-order system would be simplified to be an equivalent first-order L filter by using the WAIC scheme.

III. PROPOSED CURRENT CONTROL STRATEGY

This paper develops a high-performance current control scheme for the grid-tied three-phase four-leg inverter. It comprises of a simple WAIC based DB and a paralleled plug-in RC as shown in Fig.4.

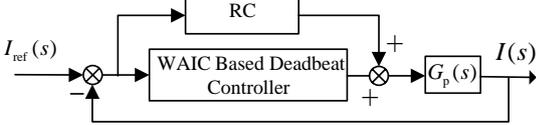


Fig. 4. Block diagram of the strategy

A. WAIC Based Deadbeat Control

The WAIC based 1st-order L filter is described as

$$v_j = L \frac{di_j}{dt} + v_{gj} \quad (7)$$

where v_j and v_{gj} is the voltage of invert output side and grid side, respectively. i_j is the weighted average inductor current of the LCL filter, with $j=a, b, c$ indicates the phase.

In discrete time domain with the sampling interval T_s , equation (7) could be

$$i_j(k+1) = i_j(k) + \frac{T_s[v_j(k) - v_{gj}(k)]}{L} \quad (8)$$

If the current is tracked in one period, namely $i_j(k+1) = i_j^*(k)$, where $i_j^*(k)$ is reference current, DB current control is obtained as the Eq.(9) by replacing $i_j(k+1)$ with $i_j^*(k)$ in Eq. (8)

$$v_j(k) = \frac{L}{T_s}[i_j^*(k) - i_j(k)] + v_{gj}(k) \quad (9)$$

According to Eq. (9), we can draw out the block diagram as shown in Fig. 5

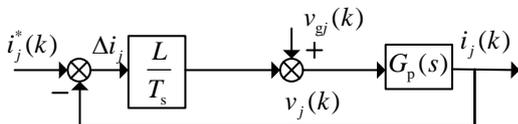


Fig. 5. Block diagram of DB controlled current loop.

DB control can force the output to track the reference with one sampling step delay, which means that DB can provide fast dynamic response [10]. However, DB control is sensitive to system uncertainties in practice, especially unmodelled time delay, e.g. computation delay, system control delay, etc. The unmodelled time delay not only will degrade the performance of the DB control system [25, 26], but also have significant impact on the system stability.

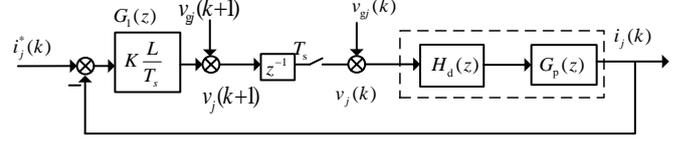


Fig. 6. Block diagram of DB control with system time delays.

The block diagram of DB controlled inverter with system time delays is shown in Fig. 6, where the computation delay is represented as one sampling time delay z^{-1} , and other unmodelled time delay is given as $H_d(s) = e^{-sT_d}$ with T_d being the time length of unmodelled delay [25, 20]. $H_d(z)$ shown in Fig. 6 is the discretization of $H_d(s)$. The coefficient K is used to replace unit coefficient of the inductance L . $G_p(z)$ is the discretization of $G_p(s)$ using zero-order holder (ZOH) $G_h(s) = (1 - e^{-sT_s}) / s$:

$$G_p(z) = \mathcal{Z}[G_h(s) \cdot G_p(s)] = \frac{T_s}{L} \cdot \frac{1}{z-1} \quad (10)$$

Using the first order Taylor expansion, the delay function $H_d(s) = e^{-sT_d}$ can be written as:

$$e^{-sT_d} = 1 - sT_d + \frac{(-sT_d)^2}{2!} + \dots \approx 1 - sT_d \quad (11)$$

If the delay time T_d is approximately treated as $T_d \approx m \cdot T_s$, where m is integer times of the sampling period T_s . Using the Tustin transfer, the delay function of $H_d(s)$ could be discretized as:

$$H_d(z) = 1 - 2m \cdot \frac{z-1}{z+1} \quad (12)$$

Hence the open-loop transfer function of Fig.6 can be expressed as

$$G_{op} = G_1(z)z^{-1}H_d(z)G_p(z) = \frac{K[(1-2m)z + 2m + 1]}{z^3 - z} \quad (13)$$

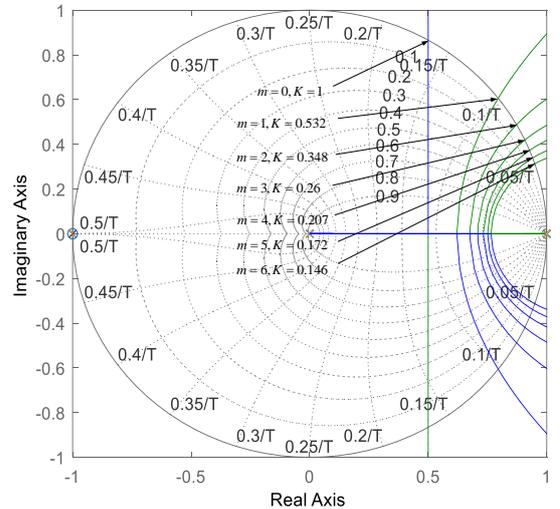


Fig. 7. Root locus of DB controller with delays in z-plane

The root locus shown in Fig.7 presents the influence of time delay steps ($m=0\sim 6$) on DB controller in z -plane. To ensure the stability of control system, the value of K should be within a certain limit range to ensure the root locus inside the unit circle. When $T_d=mT_s$ is increased from 0 to $6T_s$, the stability range of K is decreased from $K\in(0,1)$ to $K\in(0,0.146)$. It indicates that the unmodelled delay may significantly degrade the stability of the DB control system. Fig. 7 indicates that the increase of delay time T_d will decrease stability range of K . In other words, the DB controller is not immune to these unmodelled system delays [20].

Furthermore, the DB controllers highly depend on the accurate system model. But we can hardly get accurate models of grid-connected inverters with various disturbances and uncertainties in practice. The DB controller cannot eliminate periodic current harmonics distortions. To ensure exact current tracking and harmonic attenuation, an IMP based RC is plugged to reinforce the DB controller.

B. Plug-in Repetitive Controller

In practice, since the WAIC based DB controller cannot eliminate periodic current harmonic distortion [27]. In order to remove the residual harmonic distortion from the feed-in current [21], a plug-in phase-lead compensation RC shows in Eq. (14) is added to reinforce the WAIC based DB controller.

$$G_{rc}(z) = k_{rc} \frac{z^{-N+p} Q(z)}{1 - z^{-N} Q(z)} \quad (14)$$

where $N = f_s / f_0$ with f_s and f_0 being the sampling frequency and grid frequency, the low-pass filter $Q(z) = a_0 z + a_1 + a_0 z^{-1}$ with $2a_0 + a_1 = 1$ and $|Q(z)| \leq 1$ is usually used to achieve a trade-off between the system robustness and tracking accuracy. The k_{rc} is the control gain for tuning the convergence rate of RC, and z^p provides linear phase lead compensation. The implementation of the RC in Eq. (14) is shown in Fig. 8, and $p=3$, $a_0=0.25$, $a_1=0.5$ are employed in the following simulations and experiments.

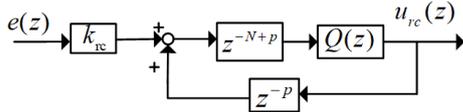


Fig. 8. The general RC with phase-lead compensation

C. Closed-loop Current Loop Stability Analysis

When the WAIC based DB controller plus the plug-in RC is applied to the three-phase four-leg inverter controller system, the transfer function of the closed-loop current control without considering delay can be written as:

$$\begin{aligned} \phi(z) &= \frac{I_j(z)}{I_j^*(z)} = \frac{[G_1(z) + G_{rc}(z)]G_p(z)}{1 + [G_1(z) + G_{rc}(z)]G_p(z)} \\ &= 1 - \frac{(1 - z^{-N}Q(z)) \cdot [1 + G_1(z)G_p(z)]^{-1}}{1 - [1 - k_{rc}z^p G_s(z)] \cdot z^{-N}Q(z)} \end{aligned} \quad (15)$$

$$\text{where } G_s(z) = \frac{G_p(z)}{1 + G_1(z)G_p(z)}$$

The following conditions should be held to ensure the above system to be stable:

- 1) The DB control system without the RC is inherently stable, that is to say, the poles of $G_s(z)$ should locate in the unit circle.

- 2) All the roots of $1 - [1 - k_{rc}z^p G_s(z)]z^{-N}Q(z) = 0$ should locate in the unit circle, i.e.

$$|1 - k_{rc}z^p G_s(z)| < 1/|Q(z)| \quad (16)$$

where $z = e^{j\omega T_s}$, with $\omega < \pi/T_s$.

Eq. (16) clearly indicates that $Q(z)$ with $|Q(z)| \leq 1$ will reinforce the system stability.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A test rig of 10kW grid-tied three-phase four-leg inverter has been configured to validate the proposed control strategy via simulations and experiments. TABLE I. list out the inverter parameters.

TABLE I. INVERTER PARAMETERS

Parameters	Value	Unit
DC-link voltage V_{dc}	700	V
Inductor L_1	3	mH
Inductor L_2	1	mH
Capacitor filter C	5	uF
Damping resistance R	24	Ω
Sampling frequency	20	kHz
Grid frequency	50	Hz
Rated RMS voltage	220	V
Rated currents	15	A
Rated power	10	kVA

A. Simulation Results

The output currents of i_1 , i_2 and the feed-in grid current output error percentage at rated power are shown in Fig.9.

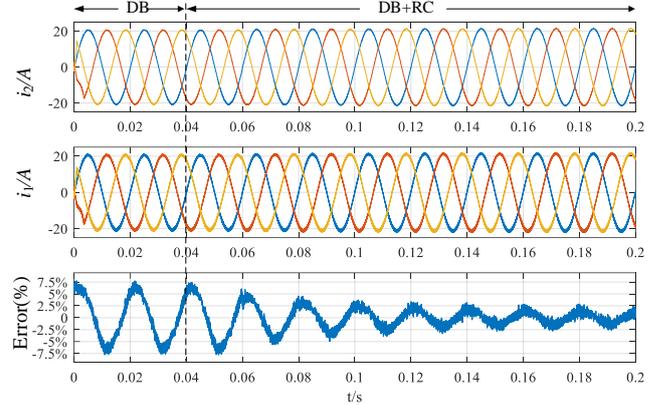


Fig.9. Plug-in RC is added onto the WAIC based DB controlled inverter at the time $t=0.04s$.

It can be seen from Fig. 9 that, the peak of current control error under the WAIC based DB control strategy is about $\pm 7.5\%$ of the reference peak current of 21.2A before the RC is plugged in at the time $t=0.04s$; and the peak of current control error is reduced from $\pm 7.5\%$ to about $\pm 2.5\%$ within 0.1s after the RC is plugged in at the time $t=0.04s$. Simulation results show that the proposed DB with plug-in RC current control scheme is of fast response and high control accuracy.

Dynamic responses of feed-in current with proposed current control scheme are shown in Fig. 10. It shows that feed-in currents can rapidly track their references within 1ms under step changes of references between 15A and 10A.

Simulation results indicate that the proposed DB plus plug-in RC is of fast response and robust to sudden reference changes.

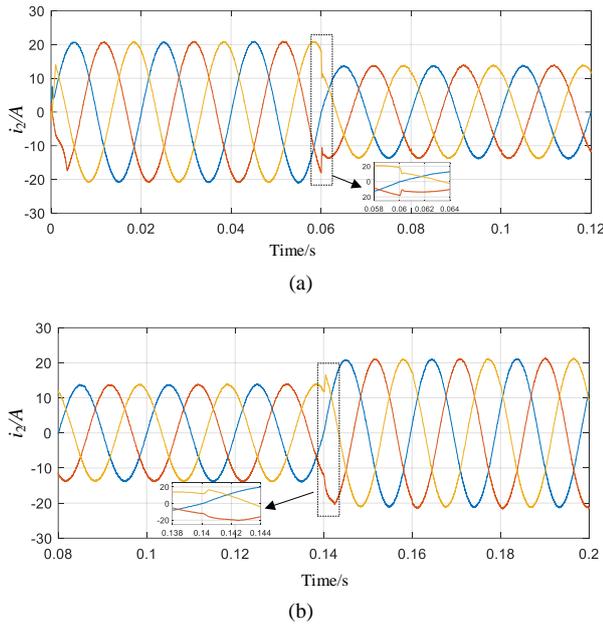


Fig. 10. Dynamic responses of feed-in grid current with the proposed strategy. (a) reference current steps from 15A to 10A (b) reference current steps from 10A to 15A

B. Experiment Results

Figure 11 shows the experiment platform of a 10kW DSP controlled three-phase four-leg grid-connected inverter for V2G application interface. Note that, as one system disturbance, the THD of the grid voltage is 2.96% in the following experiments.

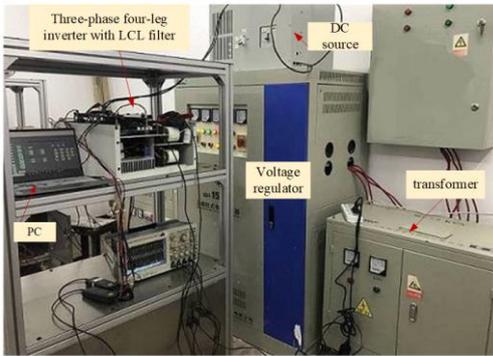


Fig. 11. The test rig of 10kW four-leg Inverter.

The steady-state feed-in grid currents at rated power and their harmonic spectrum with WAIC based DB current control strategy is shown in Fig. 12. We can see that the THD of the feed-in currents is up to 7.82%, which is not satisfied the standard of 5% specified in IEEE std. 1547. The experiment results show that WAIC based DB current control cannot well eliminate periodic current harmonic distortions in practice.

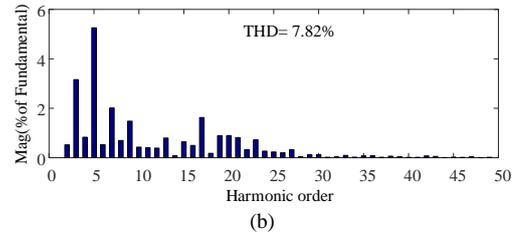
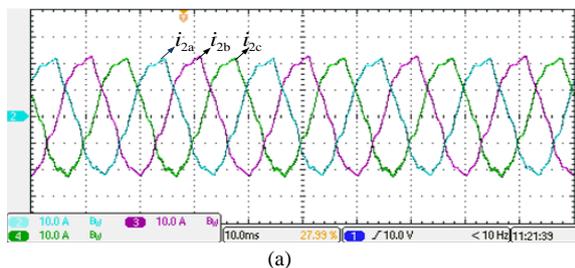


Fig. 12. Current responses with WAIC based DB controller at rated power. (a) feed-in grid currents (b) harmonic spectrum

To remove harmonic distortion from the feed-in current, a plug-in RC is added to reinforce the DB controller. Fig. 13 shows the output current at rated reference current of 15A RMS with the proposed control strategy. We can see that the THD of fed-in current is decreased remarkably to 2.06%, with the feed-in current and grid voltage in the same phase. The output current tracking error is only about $\pm 0.2A$ in the presence of the THD=2.96% of the grid voltages. Experiment results show that the proposed DB plus plug-in RC could achieve accurate current tracking and eliminate the harmonics distortion even under the condition of grid voltage distortions.

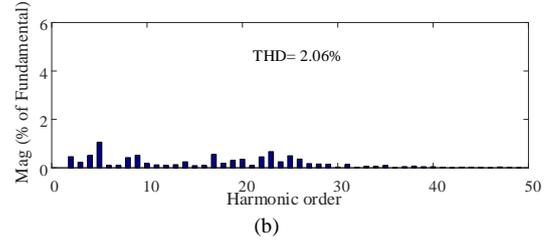
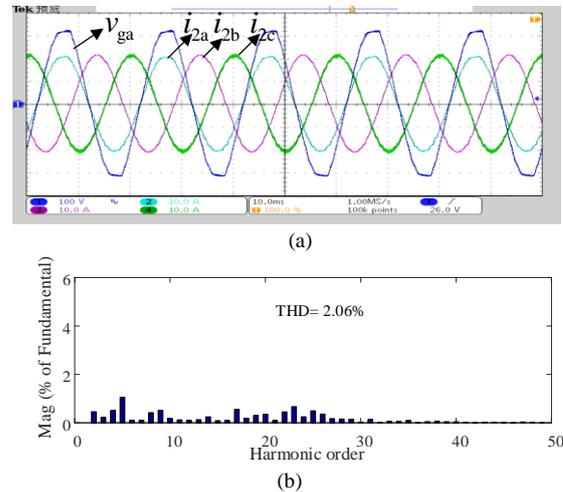


Fig. 13. Current output with proposed DB plus plug-in RC at rated power. (a) feed-in grid current (b) harmonic spectrum

Fig. 14 shows the dynamic feed-in current responses under step reference changes between 15A and 10A. The feed-in currents can track their reference rapidly within 4ms when references change. Experiment results show that the proposed DB plus plug-in RC strategy is of fast response and robust to sudden reference changes.

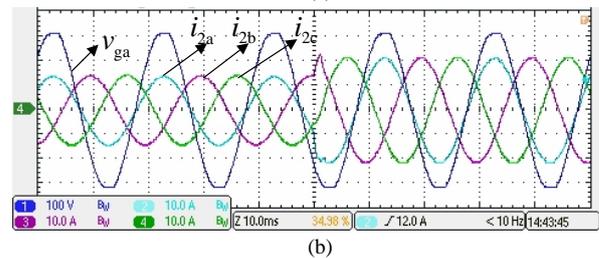
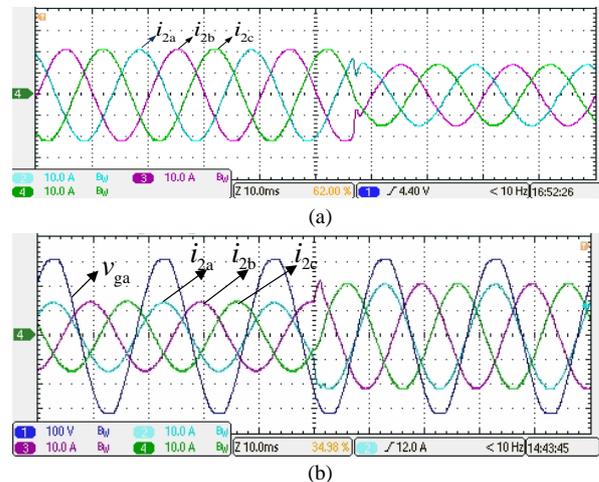


Fig. 14. Dynamic responses of the feed-in grid currents with proposed DB plus plug-in RC. (a) from 15A to 10A. (b) from 10A to 15A

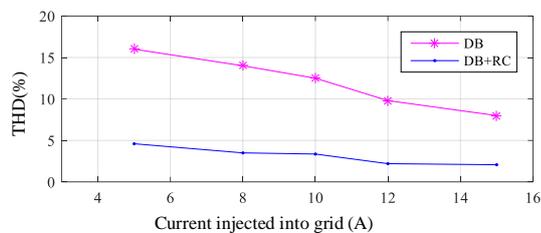


Fig. 15. THD of feed-in currents

The IEEE std. 1547 has specified the maximum THD of feed-in current should not exceed 5% at rated current capacity. Fig.15 shows that the THD of feed-in currents with the proposed scheme is always below the threshold of 5% in the range of 5A to 15A, while the THD of feed-in currents with WAIC based DB controller is always above 5%. That is to say, the V2G inverter with proposed DB plus plug-in RC can offer good quality feed-in current in the range of 30% to 100% of rated power.

All the experiment results show that the proposed current control strategy provides a simple high-performance solution to the three-phase four-leg V2G inverters with LCL filter.

V. CONCLUSION

This paper proposed a simple high performance current control scheme for V2G three-phase four-leg inverters with LCL filter, which comprises of a WAIC-based deadbeat (DB) controller and a plug-in repetitive controller (RC). Using the WAIC, the third-order LCL filter can be simplified to be an equivalent 1st order L filter, which subsequently simplify the design and analysis of the current control scheme. Based on the equivalent 1st order L filter, a simple DB controller is developed for the three-phase four-leg inverter. The DB controller is of very fast response and easy implementation, but is not immune to system time delay and various uncertainties. The stability analysis of the DB controlled inverter is conducted to investigate the impact of the unmodelled system time delay. To overcome the disadvantages of the DB controller, a plug-in RC is added to reinforce the DB controller to remove harmonic distortion from the feed-in current. The results of both simulations and experiments on a 10kW grid-connected three-phase four-leg inverter with LCL filter show that the proposed current control scheme offers a very simple high performance control solution to V2G interface inverters, which is of high accuracy, fast response and good robustness and easy implementation in the presence of various uncertainties.

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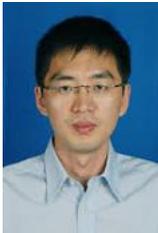
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Cuilan Tan received the B.S. and M.S. degree in School of Automation, Wuhan University of Technology, Wuhan, China, in 2002 and 2009 respectively, where she is currently pursuing the Ph.D. degree. Since 2009, she has been a faculty member at Jiangnan University, Wuhan, China, her research interests include power electronics and electric drives, current control for grid-tied inverters



Qihong Chen (M'08) received the Ph.D. degree in control science and engineering from Southeast University, Nanjing, China, in 2003. He is currently a Professor with the Wuhan University of Technology, Wuhan, China. His current research interests include grid tied inverters and predictive control.



Keliang Zhou (M'04-SM'08) received the B.Sc. degree from the Huazhong University of Science and Technology, Wuhan, China, the M.Eng. degree from Wuhan Transportation University (now the Wuhan University of Technology), Wuhan, and the Ph.D. degree in Electrical Engineering from Nanyang Technological University, Singapore, in 1992, 1995, and 2002, respectively. He is currently a Senior Lecturer with James Watt School of Engineering at the University of Glasgow, Glasgow in U.K. since 2014.

He has authored or co-authored one monograph on "Periodic Control of Power Electronic Converters", more than 100 technical papers and several granted patents in relevant areas. His teaching and research interests include power electronics and electric drives, renewable sources assessment and integration, general PID control and applications.



Liyan Zhang received the Ph.D. degree in control science and engineering from Zhejiang University, Hangzhou, China, in 2004. He is currently a Professor with the Wuhan University of Technology, Wuhan, China. His current research interests include predictive control, and modeling and control of hybrid electric vehicles.