Quantum Interference in Silicon 1D Junctionless Nanowire Field Effect Transistors:
Supplementary Information

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FABRICATION

The devices were fabricated from 55 nm silicon-on-insulator (SOI) wafers from SOITEC with a 145 nm buried oxide. The SOI layers were implanted with P at 15 keV with doses of $4 \times 10^{14}$ cm$^{-2}$ and $5 \times 10^{15}$ cm$^{-2}$ before being annealed at 950 °C for 90 seconds. The activated dopant densities of the wafers were determined in Hall-bar measurements to be $4 \times 10^{19}$ cm$^{-3}$ and $2 \times 10^{20}$ cm$^{-3}$ for the low and high implantation dose respectively[1]. Next the top Si was etched to reduce the thickness before a Vistec VB6 electron beam lithography tool was used to pattern an etch mask for the nanowire with hydrogen silsesquioxane (HSQ). The pattern was transferred to the silicon in a low damage SF$_6$ / C$_4$F$_8$ inductivity coupled plasma etch [2] before the resist was stripped and a thermal oxide was grown at 950 °C. The electrical contacts were defined using optical lithography and metalized with 20 nm of Ni and 50 nm of Pt after the oxide had been stripped with HF. The samples were annealed in forming gas at 380 °C for 15 minutes to alloy the contacts and produce a NiSi Ohmic contact to the silicon channel with a specific contact resistance of 0.8 Ω-mm. This anneal also reduced the interface trap density $D_{it}$ between the oxide and the channel as shown for similar devices in Fig. 1. Finally electron beam lithography was used with 400 nm of PMMA resist to lift-off the Al gate.

![Graph](image)

**FIG. 1.** Density of interface traps $D_{it}$ as a function of frequency $f$ before the forming gas anneal (red) and after forming gas anneal (blue).

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IMAGING

Cross-sectional samples of nanowires were fabricated using an FEI Nova Dualbeam Focused Ion Beam (FIB) Scanning Electron Microscope (SEM) instrument using standard "lift-out" and polishing protocols. A thin protective Pt layer was deposited prior to milling using electron beam induced deposition, which also led to the vacuum gap beneath the wire being filled with Pt, which is just visible in Fig. 1b of the manuscript. Transmission Electron Microscopy (TEM) and Scanning TEM (STEM) were then performed on a JEOL ARM200cF instrument that was operated at 200 kV. A Gatan Quantum spectrometer and Bruker XFlash spectrometer were used for electron energy loss spectroscopy (EELS) and energy dispersive xray spectroscopy (EDS), respectively, using the latter to map Pt. Elemental mapping was performed using a "spectrum imaging" methodology, using background-subtracted Si-K (1839 eV energy loss), Al-K (1560 eV), O-K (532 eV) and C-K (284 eV) EELS edges, and the Pt - Lα peak in EDS. Acquisition and data processing were conducted using routines within Gatan’s Digital Micrograph software.

FERMI WAVELENGTH

One dimensional transport in a nanowire structure requires a Fermi-wavelength on the order or larger than the nanowire diameter. To estimate the Fermi-wavelength we require the activated dopant density $n$:

$$\lambda_F = \frac{g_sg_v}{n^{1/3}}$$  \hspace{1cm} (1)

where $g_s = 2$ and $g_v = 2$ are the valley- and spin-degeneracies in a confined silicon system. For the activated dopant concentrations measured in the wafers, $n = 4 \times 10^{19} \text{ cm}^{-3}$ and $n = 2 \times 10^{20} \text{ cm}^{-3}$, this yields 11.7 nm and 6.8 nm. Since additional dopant deactivation due to e.g. dielectric effects will lower the activated dopant concentration and thus increase the Fermi wavelength, these numbers are a lower boundary[3]. We therefore conclude, that 1D confinement effects are indeed relevant in our nanowires in agreement with previous results from Mirza et.al[4]. For quantum interference along the nanowire axis, we require a wavelength of an electron travelling in parallel to the nanowire axis on the order of the mean free path or lower. This is not the same wavelength as the Fermi-wavelength discussed in the previous paragraph, where we the entire electron energy is used to calculate the wavelength. For the wavelength of an electron travelling along the nanowire axis, the confinement energy needs to be taken into account. We cannot accurately calculate this wavelength given the uncertainties in confinement potential and the activated dopant density at a given gate voltage. We can, however, get a rough estimate from the data in the Fig. 3 of the main text and carry out a sanity check: The nanowire is starting to be conductive (at the lowest temperature) at 1.2 V in gate voltage and the first oscillations in conductance are observed at 2.7 V. Assuming a lever arm of around $\alpha = 0.1$ this corresponds to an electrostatic energy addition of 150 meV and, assuming only the first subband is occupied, we can calculate the associated wavelength via:

$$\lambda_{||} = \frac{2\pi\hbar}{2m^*E} = 7.2 \text{ nm}$$  \hspace{1cm} (2)

where $m^* = 0.19m_e$ is the effective electron mass and $m_e$ is the electron mass. This is on the order of the mean free path that was found and therefore supports the interpretation of the data.

COULOMB BLOCKADE IN LARGE GATE RANGE

The range of gate voltage in which the Coulomb blockade persists in device A is much larger than the one shown in the main text. In Fig. 2 of this Supplementary Information we show a measurement over 6 V in gate voltage with over 500 equally spaced Coulomb-peaks. Figure 3 shows a close up of two regions on both ends of the gate voltage range. The autocorrelation in the main text is taken from the entire data set. Figure 4 shows a histogram of the Coulomb peak spacing as an alternative to the autocorrelation in the main text.

COULOMB BLOCKADE IN DEVICE B

Device B shows signatures of Coulomb blockade in the low gate region. In contrast to a single quantum dot, however, the spacing of the peaks is not constant and the stability diagram (shown here in Fig. 5) contains many diamonds that do not close all the way. This behaviour is indicative for transport through a channel that breaks up into one or multiple islands depending on the gate voltage. A similar behaviour is suggested by the low gate region in device C for $V_g < -6 \text{ V}$ (see Fig. 6).
FIG. 2. Current $I$ as a function of gate voltage $V_g$ in the entire gate voltage range from the measurement in Fig. 2 of the main text.

FIG. 3. Current $I$ as a function of gate voltage $V_g$ at the top end and the low end of the gate voltage window in Fig. 2 of this Supplementary Information.

CIRCULAR CAPACITOR MODEL

The capacitance of the devices can be estimated from a circular capacitor model (coaxial capacitor). We extract the geometrical parameters from TEM and SEM pictures[1] including the radius of the nanowire $a=4$ nm, the
FIG. 4. Histogram of the Coulomb peak spacing as a function of gate voltage.

FIG. 5. Conductance $G$ as a function of gate voltage $V_g$ and bias voltage $V_b$ in the low gate voltage region of device B.

distance to the gate $b=34$ nm and the length of the nanowire $L=150$ nm:

$$C_g = \frac{2\pi\epsilon_\epsilon_0}{\ln (b/a)} L = 15.2 \text{ aF}$$

(3)

Here $\epsilon_0$ is the vacuum permitivity and $\epsilon_r = 3.9$ is the relative permitivity of the oxide.
FIG. 6. Transconductance $dG/dV_g$ as a function of gate voltage $V_g$ and bias voltage $V_b$ in device B. Green arrows indicate the expected pattern for quantum interference features as discussed in the main text.

**DEVICE C**

Fig. 6 shows the transconductance $dG/dV_g$ as a function of bias voltage $V_b$ and gate voltage $V_g$ for device C at 4 K. The green arrows point to the non-zero bias plateaus discussed in the main text.

**TEMPERATURE DEPENDENCE AND BACKGROUND**

Figure 3 of the main text shows the differential conductance at zero-bias measured with an SR830 lock-in amplifier for only 4 out of 82 temperatures. Here we show the entire data set in Fig. 7 for temperatures from 30 mK to 28 K. For some temperatures there is an artefact in the measured conductance at high gate voltages which likely stems from the limitations of the amplifier - we have removed those traces in the following analysis. The gate traces were fitted with a forth degree polynomial function to capture the background well, but not fit the fluctuations on a smaller scale. The selection of this fit function was done very carefully to avoid residual effects in the following. After subtracting these fits from the data we have isolated the fluctuations (see Fig. 8) and taken the
FIG. 7. Differential conductance $G$ as a function of gate voltage $V_g$ at temperatures from 30 mK to 28 K.

root mean square over the gate-traces to obtain the data in the inset of Fig. 3 in the main text.
FIG. 8. Differential conductance $G$ as a function of gate voltage $V_g$ at temperatures from 30 mK to 28 K after removing the background with a forth degree polynomial fit for every temperature trace.

TEMPERATURE DEPENDENCE OF $\Delta G$

The constant regime in the inset of Fig. 3 of the main text corresponds to a case where the Universal Conductance Fluctuations are not reduced by thermal averaging or a decreasing coherence length $l_\phi$ and the associated averaging over multiple independently fluctuating parts of the nanowire. In the regime above 1.9 K two mechanisms are causing the decrease in $\Delta G$ with temperature: A reducing coherence length following Nyquist dephasing due to electron-electron interactions in one dimension[5] and thermal broadening characterized by the thermal length $l_T$. In this section we describe the temperature dependence in the cases where one mechanism dominates over the other as well as in the case where both mechanisms are contributing.

The coherence length is associated to a coherence time via

$$l_\phi = \sqrt{D\tau_\phi}$$

as well as an energy scale

$$E_c = \frac{\hbar D}{l_\phi^2}$$

analogous to the thermal energy

$$E_T = \frac{\hbar D}{l_T^2} = k_B T$$
According to Ref. 3 the dephasing time is proportional to \( T^{-2/3} \) for Nyquist dephasing in 1D. The coherence length therefore scales according to:

\[ l_{\phi} \propto T^{-1/3} \quad (7) \]

The thermal length scales according to Eq. 6:

\[ l_{T} \propto T^{-1/2} \quad (8) \]

In case the Nyquist dephasing dominates over thermal broadening \( E_{c} >> E_{T} \) \((l_{\phi} << l_{T})\) temperature effects can be neglected and \( \Delta G \) follows\[6, 7\]:

\[ \Delta G \propto l_{\phi}^{3/2} \propto T^{-1/2} \quad (9) \]

In case the thermal broadening dominates \( E_{c} << E_{T} \) \((l_{\phi} >> l_{T})\)[6, 7]:

\[ \Delta G \propto l_{\phi}^{1/2} l_{T} \propto T^{-2/3} \quad (10) \]

In the intermediate regime Beenakker and van Houten have calculated a interpolation formula for \( E_{c} \sim E_{th} \) \((l_{\phi} \sim l_{T})\)[7]:

\[ \Delta G = C \left( \frac{l_{\phi}}{L} \right)^{3/2} \left( 1 + \frac{9}{2\pi} \left( \frac{l_{\phi}}{l_{T}} \right)^{2} \right)^{-1/2} \quad (11) \]

where \( C \) is a constant. The temperature dependence of this expression is more complicated than a simple power law and approaches the limiting cases mentioned above for \( l_{\phi} << l_{T} \) and \( l_{\phi} >> l_{T} \)