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Power Management Using Photovoltaic Cells for Implantable Devices

KAUNG OO HTET, (Student Member, IEEE), RAMI GHANNAM, (Member, IEEE), QAMMER H. ABBASI, (Senior Member, IEEE), AND HADI HEIDARI, (Senior Member, IEEE)

School of Engineering, University of Glasgow, Glasgow G12 8QQ, U.K.

Corresponding author: Hadi Heidari (hadi.heidari@glasgow.ac.uk)

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ABSTRACT This paper presents a novel inductor-less switched capacitor (SC) DC–DC converter, which generates simultaneous dual-output voltages for implantable electronic devices. Present dual output converters are limited to fixed ratio gain, which degrade conversion efficiency when the input voltage changes. The proposed power converter offers both step-up and step-down conversion with 4-phase reconfigurable logic. With an input voltage of 1 V provided by photovoltaic (PV) cells, the proposed converter achieves step-up, step-down, and synchronised voltage conversions in four gain modes. These are 1.5 and 0.5 V for normal mode, 2 and 1 V for high mode, 2 V for double boost mode, as well as 3 and 2 V for super boost mode with the ripple variation of 14–59 mV. The converter circuit has been simulated in standard 0.18-μm CMOS technology and the results agree with the state-of-the-art SC converters. However, our proposed monolithically integrated PV powered circuit achieves a conversion efficiency of 85.26% and provides an extra flexibility in terms of gain, which is advantageous for future implantable applications that have a range of inputs. This research is, therefore, an important step in achieving truly autonomous implantable electronic devices.

INDEX TERMS Implantable electronics, solar power, switched capacitor, DC-DC converter, simultaneous outputs, single-input-dual-outputs (SIDO).

I. INTRODUCTION

Implantable electronic devices are now becoming widely used in healthcare, entertainment, tracking and security applications [1]–[4]. Advancements in CMOS fabrication processes is further miniaturising these devices [5]–[8]. Wearable or implantable electronic devices can be grouped into a number of important building blocks. This research focuses on the energy supply block, which will be powered by solar cells. Solar cells have previously been used in wearable electronic devices, such as the artificial iris demonstrated in [9] and [10]. However, energy harvesting systems that rely on solar energy need to have rectifying circuits to maintain high energy efficiency. This is due to the intermittency and variability of incoming solar radiation [11].

Photovoltaic cells convert light into electricity. These cells range from expensive high-efficiency multi-junction devices to lower cost non-crystalline devices. This paper presents an innovative solution to convert the unregulated output voltage of PV cells to a regulated DC voltage, which can be used by implanted sensors and circuits under skin, as shown in Fig. 1. Ultimately, reliable and efficient DC-DC conversion offers steady and regulated DC output voltage from an unregulated source to attain longer and more efficient system run-time.

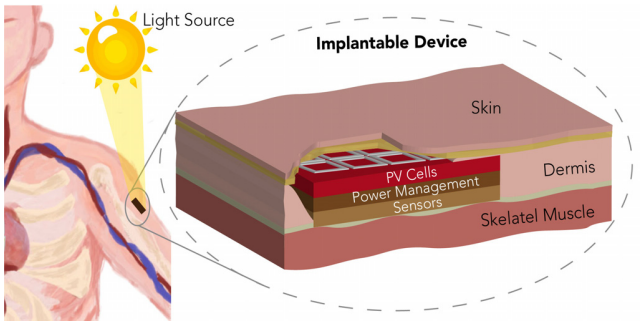

FIGURE 1. Envisaged Implantable device with integrated Photovoltaic cells.

System-on-chip implantable devices have a range of functionalities and electronic components. Each of which may contain circuits and sensors that operate at different voltages for the required power. Such a system is powered by a single input source, which requires an energy conversion unit.

TABLE 1. Integrated power management designs.

Ref	Configuration	C_{fly} (F)	Mode	Input (V)	Output (V)	Gain	Max-Efficiency (%)	Power (W)
[14]	Dickson	40p×4	Boost	0.55-0.7	1.1-3.4	4-stage	66	0.1-32µ
[18]	Cross-coupled	630p×6	Boost	1.2	4.8	3-stage	80.2	479µ
[19]	Dickson+Cross	20p×9	Boost	0.45-0.60	4	6-stage	51.7	-
[20]	Series-parallel	1µ×4	Buck	1.6-3.3	0.5-3	Multiple	91	250m
[21]	Series-Parallel	1µ×3	Boost	1.4-3	4.8	Multiple	82	2.4-48m

In this regard, the DC-DC converters can perform either step-up or step-down conversions to provide the required voltage at the load. Current energy harvesting mechanisms are limited in size and low generated power, such as the PV system shown in [12], the high motion dependent Piezoelectric system in [13], the thermoelectric system in [14], the electrostatic system in [15] and the electromagnetic system in [16]. The degrading factors such as temperature, light, and motion reduce the nominal output power, which will be fed back into the power management unit. Therefore, the conversion efficiency of a converter with a fixed ratio gain will decrease over time since the gain ratio relative to the input value changes.

The integrated monolithic chip converter or power management system is based on the charge pump designs described in Table 1. Examples include the Dickson charge pump [14], [17] and cross-coupled design [18] for step-up conversion purposes, or use of the hybrid charge pump together with energy harvester [19]. However, only the integer gains can be configured in charge pump design, which makes them inconvenient for applications with varying inputs. This is because whenever there is a change in input voltage, the circuit may need to be re-adjusted to keep up with the high conversion ratios. Therefore, series-parallel converters [20] that can configure non-integer gain values as well as reconfigure gains [21], [22] are becoming more popular.

Current Series-parallel converters are reconfigurable. Sometimes a certain load operating at the highest voltage requires both maximum powers from the converter and for a long period of time. Thus, the converter ends up driving at its optimum gain almost all the time to provide the sufficient voltage to all the present loads connected to a single output line. Moreover, since all the loads are connected to a single output line, small loads with low operating voltages require further drop down using additional Linear Drop Out (LDO) circuits. This leads to power losses across additional components. To overcome these issues, researchers have used SIMO configuration with either fixed or a limited number of conversion ratios [23]–[26]. In our case, we have implemented a system with a more diverse range of conversion ratios due to the range of input voltages that are obtained from our PV energy harvesting source.

The rest of paper is organised as follows, section II of the paper, details of the converter methodology are specified. The design and implementation are provided in Section III. Similarly, the simulation results are presented in Section IV. Finally, the conclusions and future work are provided in Section V.

II. POWER MANAGEMENT METHODOLOGY

This paper introduces a miniaturised power management DC-DC converter design, which will be an integrated on-chip power system for implantable devices. An inductor-less, switched-capacitor, DC-DC converter design is used to remove the involvement of bulky inductors. Moreover, power management is obtained using series-parallel connections of flying capacitors via MOSFET power switches. These are all digitally controlled using digital modules, as shown in Fig. 2. The PV cell and its energy storage device (battery) are employed for the primary energy inputs. Depending on the load requirements of the power conversion unit, it performs both step-up and step-down voltage conversions at the same time by using the novel 4-phases rotation scheme with 4 flying capacitors. The appropriate gain pairs are chosen accordingly to produce a different gain of step-up conversion simultaneously. These different set of gain pairs can be categorised into four different modes (Normal, High, Double Boost and Super Boost). This novel topology, which uses single-input-dual-output (SIDO) design, is inspired by the single-input-single-output (SISO) 3-phases rotation topology presented in [27], whereby one idle capacitor in every charging phase is always present. To achieve the same objective, two outputs need to be produced independently. This will require either doubling the SISO converters twice [28] (which can only generate one gain at a time), or stack the capacitors as a capacitor bank [29].

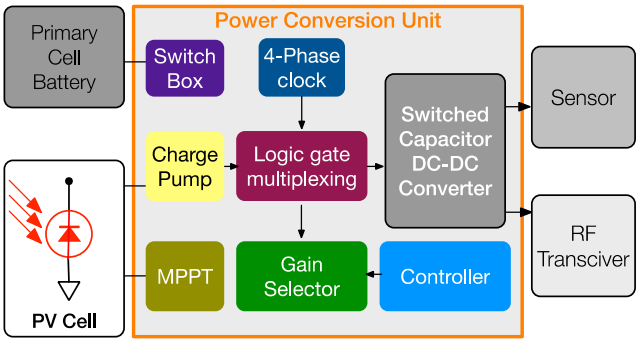

FIGURE 2. Block Diagram of a power conversion for energy harvesting using photovoltaic cells in Implantable applications.

This converter has achieved the reconfigurable dual outputs (V_{out1}, V_{out2}), which can produce regulated voltage

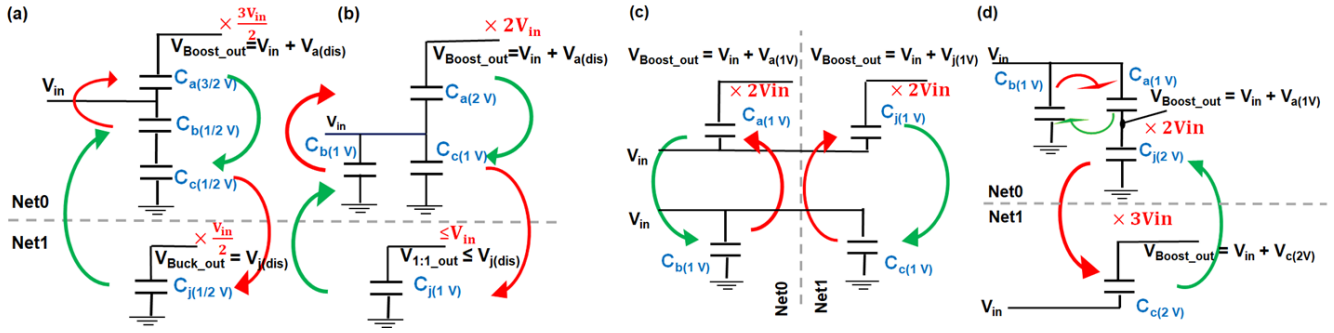

FIGURE 3. Proposed Methodology different modes with arrows indicating charging (green) and discharging (red) directions.

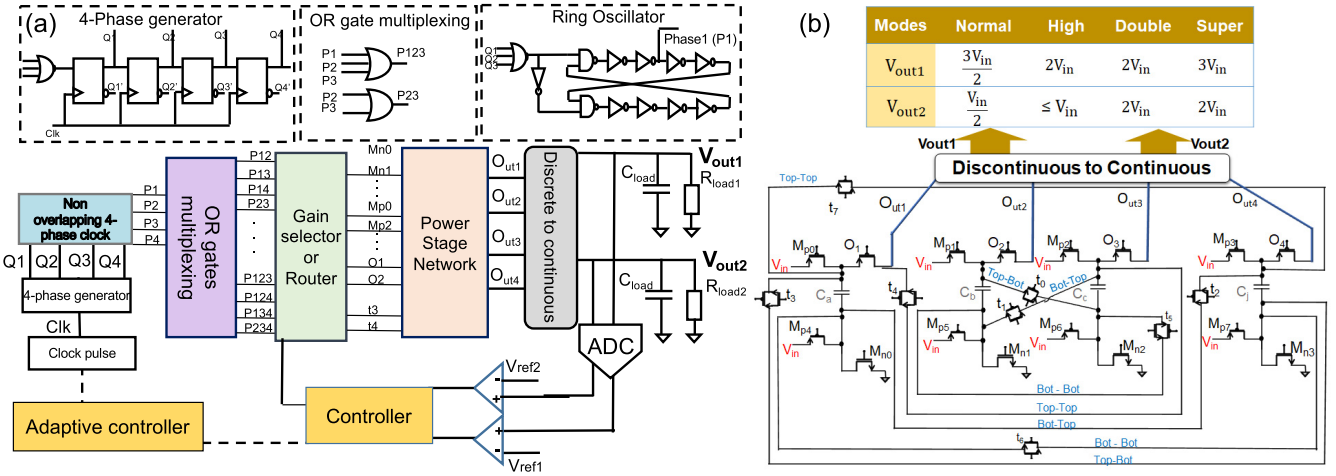

FIGURE 4. (a) Overall schematic diagram of proposed converter which highlighted the crucial blocks. (b) Circuit level diagram of the power stage network which the operation is digitally controlled by a non-overlapping 4-phases clock.

pairs of both boosting or boost and buck at the same time. There are four different gain modes, representing each set of voltage gains generated from two conceptual internal networks (Net0, Net1) illustrated in Fig. 3. In each network, a different set of gains or modes are configured by constructing series-parallel configurations of capacitors and switches, as suggested by methodology. Since the positions of each capacitor are followed by its operation changes in every phase, the corresponding internal outputs (O_{ut1}-O_{ut4}) in Fig. 4 also change accordingly. Henceforth, these internal outputs shall name it as discontinuous outputs. Similarly, since the two external outputs of converters produce continuous four set of two different voltages, the external outputs can be addressed as continuous outputs. Therefore, discontinuous-to-continuous switches can be employed to correspond the connection of internal outputs (O_{ut1}-O_{ut4}) to external loads (V_{out1} and V_{out2}) at different phases.

A. NORMAL, HIGH, DOUBLE BOOST AND SUPER BOOST OPERATIONS

The operations of all four modes can be realised by following the arrow rotations described in Fig. 3. In Normal mode, two equal capacitors (C_b and C_c) are being charged in series with input source and hence stored $V_{in}/2$. Assuming a present set up in the diagram is in steady state, a step-up gain of Net0 output is obtained $3V_{in}$ /2 by discharging capacitor C_a in series with the input source. Meanwhile, a capacitor C_j is independently discharged to output at Net1 with the step-down gain of $V_{in}/2$. In the next phase, two charged capacitors are swapped with two discharged capacitors, as shown in Fig. 3(a). Since this proposed converter not only provides fixed gain outputs, rearranging series-parallel connections of power stage network can configure higher gains than Normal mode, as shown in Fig. 3(b). Instead of constructing two charging capacitors in series, parallel connections are made so that each capacitor is charged to V_{in} values, thus the output of Net1 achieves up to V_{in} gain.

The reconfigurable dual-output SC converter with the two flying capacitors was presented in [23], whereas two different step-up gain pairs are discretely output to loads in two different phases. These configurations are further enhanced in this proposed rotation scheme, interleaved with a 4-phase clocks topology as shown in Fig. 3(c) and Fig. 3(d) to enable no idle charging time for all phases. As a result, continuous outputs of $2V_{in}$ are obtained for Double Boost, as well as $3V_{in}$ and $2V_{in}$ for Super Boost in every cycle.

B. OUTPUT VOLTAGES AND POWER LOSSES

The derivation of output voltages for Normal and High modes has been described in [30]. By taking the total amount of charge for steady-state charging and discharging voltage-time ΔQ_{Mode} for Normal mode, High mode, Double Boost, and Super Boost are $\frac{I_0}{2f_s}$, $\frac{I_0}{3f_s}$, $\frac{I_0}{4f_s}$ and $\frac{I_0}{2f_s}$ respectively. The gain ratio multiplier (k) for different modes correspond to table in Fig. 4 and output voltage for individual modes can be generalised as

$$V_{boost,buck\_Mode} = kV_{in} - \frac{\Delta Q_{Mode}}{\alpha f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (1)$$

whereas t_d represents discharging time and t_c for the charging time, RC time constant (T_d and T_c) are subjected to on-resistance along the path of charging-discharging R_{on}, α is the charge multiplier varies over different modes and flying capacitor C_p which has the most dominant capacitance in power stage. The conduction power loss can be expressed from the second term of (1) multiply with the output current I_o gives (2):

$$P_{conduct\_Mode} = \frac{I^2_{o\_boost,buck}}{\alpha f_s C_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (2)$$

$$P_{sw\_Mode} = f_s \sum_i C_{gsi} V^2_{gsi} \cong f_s C_{OX} \sum_i W_i L_i V^2_{gsi} \quad (3)$$

Equation (3) represents switching power loss (P_{sw}), which is influenced by charge-discharge mechanisms of a gate-source parasitic capacitance of MOSFET transistors (C_{gs}), the frequency of switching (f_s) and the gate-source voltages (V_{gs}) of individual switches along the path [31]. The other variables are the width (W_i) and length (L_i) of individual transistors along the path of operations and the transistor gate-oxide capacitor (C_{ox}) which has the approximate value of 8.31 fF/μm^2 for 0.18 μm technology. For a steady state, due to symmetric nature of output waveforms in every mode, redistribution loss is considered by taking KQL of one phase operation. Whereas present phase discharge capacitor (C_d), switching time (T_s) and the number of parallel connections with C_d (n) are described in (4):

$$P_{redis\_Mode} = \frac{I^2_{o\_boost,buck} T_s}{4C_d} + \frac{I^2_{o\_boost,buck} T_s}{8(nC_d + C_{load1,2})} \quad (4)$$

III. DESIGN AND IMPLEMENTATION

This design is implemented in a standard 0.18 μm CMOS technology and Fig. 4 represents the system diagram of the proposed converter controlled by digital modules. In generating the 90-degree phase shift four-phase clock in every rising edge of the input clock, a series of four D-flip flops are employed. The ring oscillator circuits, by taking phase generator outputs, are used to construct 0.1 ns non-overlapped region to benefit full charge settling and prevent reversion loss. To accommodate all the combination of 4-phase pairs as clock signal inputs in the next router module, OR gate-multiplexing is used. Depending on the topology selection, the same transistor can be active for all 4-phases.

In the proposed design, there are four sets of gain pairs. Each can provide the different set of voltage gains, such that boost-buck or boost-boost to the output are simultaneously obtained. The wide range of gain selection greatly benefit applications with a wide range of input to maintain high efficiency. By monitoring the load condition via ADC, the comparator compares the output voltage with a reference voltage to provide the flag information to choose the appropriate gain mode in digital router module programmed in Verilog-A. All the transistor addresses for four different phases logics are registered and automatically reconfigure the power stage network in accordance with the proposed methodology when a selection of gain modes changes. Currently, a gain selection is made via a simple controller program with the predetermined voltage references and simulating through parametric fixed loads. Thus, it is still acting as the open loop circuit. Therefore, our next step is to upgrade the controller and feedback loop to enhance autonomous error minimising and close the loop. Similarly, adaptive pulse unit can be further improved by introducing an advanced algorithm, instead of manually selecting predetermined optimum operating frequencies for each mode.

The power circuit network is comprised of 20 switches to configure four integrated 1 nF capacitors from analog library in series-parallel positions. However, only a few switches are required to configure the selection of mode as shown in Fig. 5(a-d). To charge and discharge the capacitors the switches have been implemented by PMOS and NMOS transistors. The transmission gates are employed due to its bi-directional charge transfer, switching on-off fast transitions, small turn-on resistance to minimise conduction power loss and to avoid charge injection or clock feedthrough on both capacitors connected in the series arrangement. The circuit level configuration of the High mode is illustrated in Fig. 5(b) as an example and the all the active switches to configure all four modes in 4-phases are described in Table 2. In High mode, the two capacitors are charged in parallel by V_{in} through (M_{p0}, M_{n0}, M_{p1}, M_{n1}) to capacitors (C_a, C_b) for the phase1 and (M_{p2}, M_{n2}, M_{p3}, M_{n3}) are employed to charge capacitors (C_c, C_j) in the phase4. Meanwhile, in the phase1 Net0, capacitor C_c is discharged in series with the input voltage to get $2V_{in}$ at O_{ut3} through (M_{p6}, O_3) and capacitor Cj is independently discharged at Net1 to the gain of V_{in} at O_{ut4} through (M_{n3}, O_4). Likewise, in phase 4, the Net0 output with the gain $2V_{in}$ is received at O_{ut2} via (M_{p5}, O_2) and Net1 output with the gain of V_{in} is achieved at O_{ut1} via (M_{n0}, O_1). In the next phase, both discharged capacitors are swapped with two charged capacitors as suggested in topology. Thanks to the symmetry of the design, phase 2 and phase 3 can be described in a similar manner. By keeping the minimum length for all transistors, the width of PMOSs is 60 μm and 20 μm for NMOSs is used.

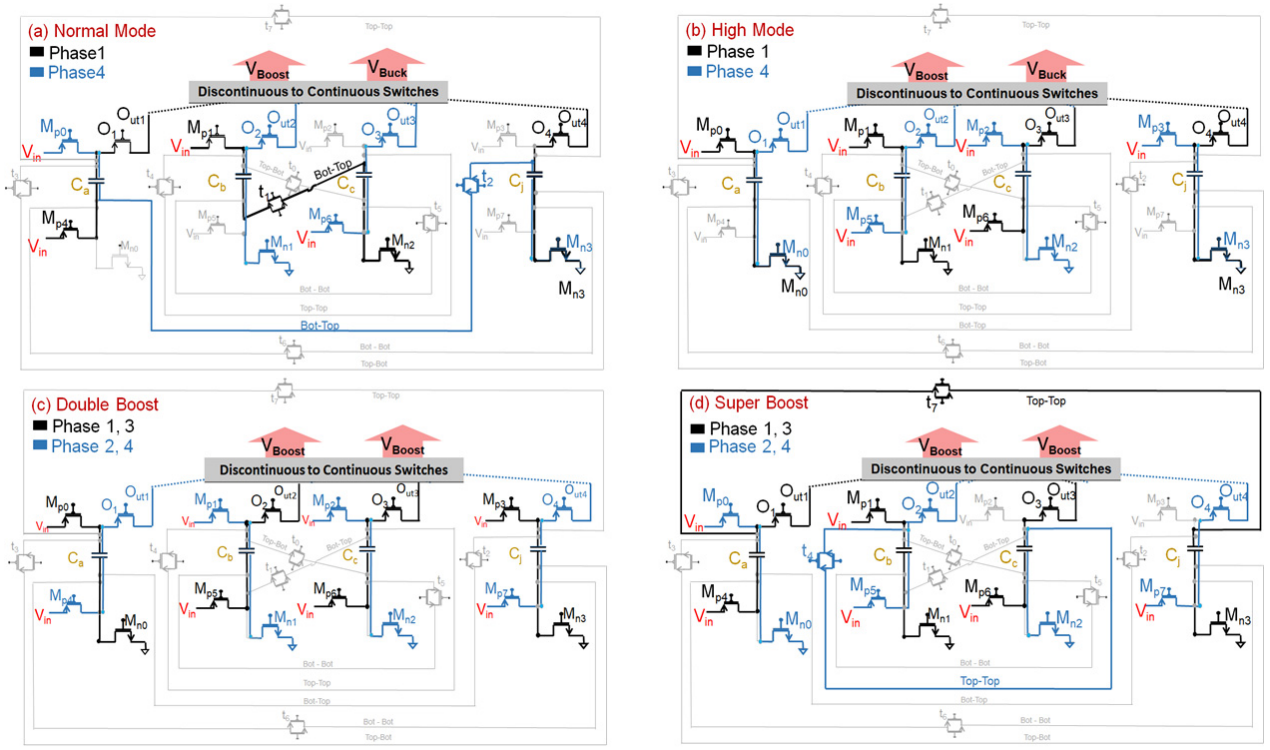

FIGURE 5. Operation phases of Power Stage network at 4 different modes: (a) Normal Mode; (b) High Mode; (c) Double Boost; (d) Super Boost.

TABLE 2. Active switches for all four modes in 4-phases(P1-P4). Switches in green area are used for charging and red area are for discharging.

Phase	Net0						Net1			
Normal Mode										
P1		Mp1	t1	Mn2	Mp4	O1			Mn3	O4
P2		Mp3	t3	Mn0	Mp5	O2			Mn2	O3
P3		Mp2	t0	Mn1	Mp7	O4			Mn0	O1
P4		Mp0	t2	Mn3	Mp6	O3			Mn1	O2
High Mode										
P1	Mp0	Mn0	Mp1	Mn1	Mp6	O3			Mn3	O4
P2	Mp2	Mn2	Mp3	Mn3	Mp4	O1			Mn1	O2
P3	Mp0	Mn0	Mp1	Mn1	Mp7	O4			Mn2	O3
P4	Mp2	Mn2	Mp3	Mn3	Mp5	O2			Mn0	O1
Double Boost Mode										
P1		Mp0	Mn0		Mp5	O2	Mp3	Mn3	Mp6	O3
P2		Mp1	Mn1		Mp4	O1	Mp2	Mn2	Mp7	O4
P3		Mp0	Mn0		Mp5	O2	Mp3	Mn3	Mp6	O3
P4		Mp1	Mn1		Mp4	O1	Mp2	Mn2	Mp7	O4
Super Boost Mode										
P1	Mp1	Mn1	t7	Mn3	Mp4	O1			Mp6	O3
P2	Mp0	Mn0	t4	Mn2	Mp5	O2			Mp7	O4
P3	Mp0	Mn0	t4	Mn2	Mp5	O2			Mp7	O4
P4	Mp1	Mn1	t7	Mn3	Mp4	O1			Mp6	O3

In all gain modes at 4-phases, the power switches protocols are designed to retain the optimum symmetric nature of same on resistances R_{on} value for consistency of outputs level. This is because different pathing for the same logic can lead to small variation in ΔV at internal outputs of power stage (O_{ut1}-O_{ut4}). For instance, Super Boost phase 1,4 O_{ut1} and phase 2,3 O_{ut1}, configurations not only provide the same output value but also share the same R_{on} values. It is to note that transistors (t_5, t_0, t_6, t_3) are reserved for the future purpose. The voltage regulation can be further improved by introducing adaptive pulsing unit in between gain selector and power stage network since fast switching energy delivery for low and high loads can vary. Therefore, 5.8823 kHz for Normal, 666.66 kHz for High, 1.1 MHz for Double Boost and 2 MHz for Super Boost are chosen respectively, as operation frequencies.

IV. SIMULATION RESULTS

The results of our simulations are shown in Fig. 6(a-d). These are simulated for a 1 V input at a temperature of 27°C, while the loads are varied from 50-100 kΩ. We show that a voltage conversion efficiency of 98% can be achieved. At best, the average boost output mode produces 1.49 V (at 29.45 μA) and the buck being 0.467 V (at 9.36 μA) Normal mode. Likewise, for the High mode, the average boost output produces 1.905 V (at 39.2 μA) and 0.98 V (at 19.6 μA) for the buck output. Similarly, Double Boost produces 1.97 V (at 39.4 μA), and Super Boost yields 2.85 V (at 57.1 μA) and 1.89V (at 37.8 μA) average outputs. The output ripples are recorded between 14-59 mV. The line transient indicates that the converter takes approximately 1-3.3 μs to get the first

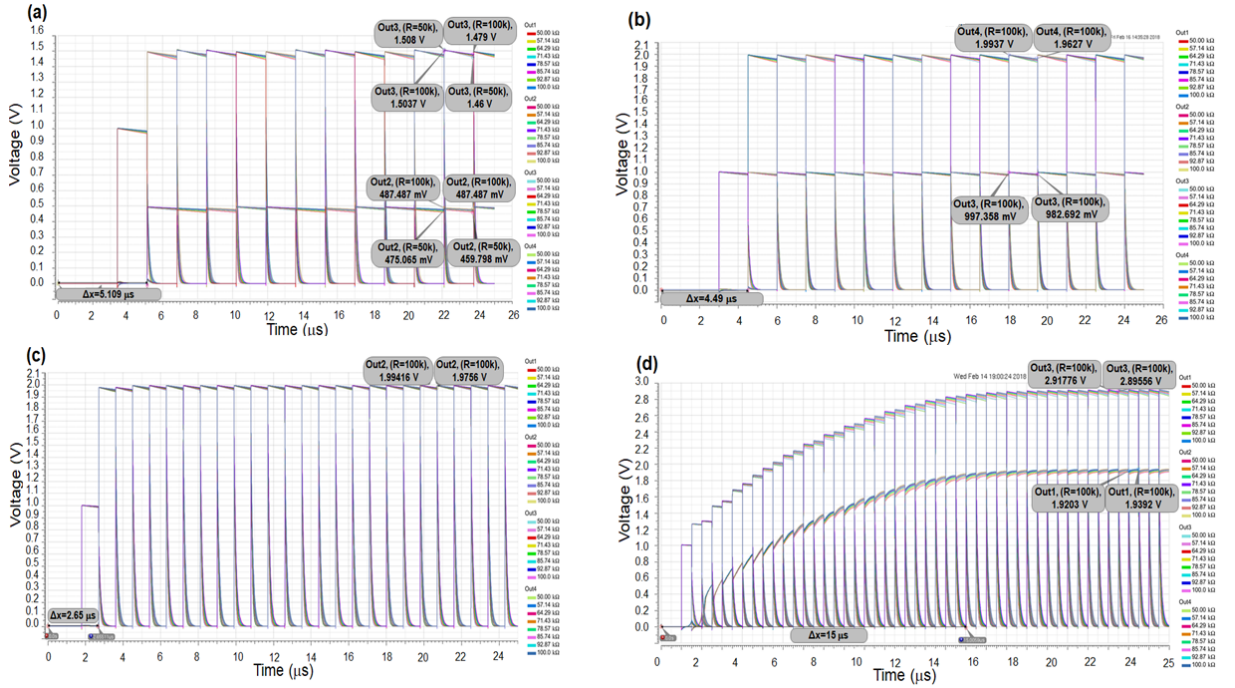

FIGURE 6. The simulated voltage output of (a) Normal Mode (b) High Mode (c) Double Mode (d) Super Boost over different loads 50-100 kΩ.

signal and 2.65-15 μs load transient time to reach saturation, depending on the selection of modes and the loads.

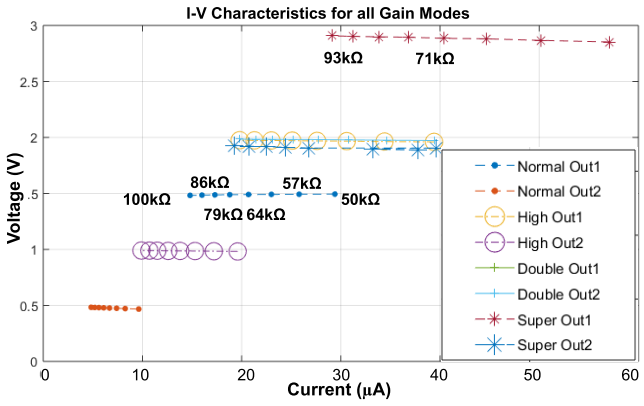

FIGURE 7. Current Vs Voltage characteristic at 50-100 kΩ for four different modes.

To analyse the output power of the proposed system, output voltages and currents values of all gain modes tested with various resistance loads 50-100 kΩ are recorded from the simulation. These values are then plotted in Fig. 7. When the loads increase, the voltage at the output increases and the current dropped as expected from Ohms law characteristic. Each mode has different gradient change due to its different in internal resistance R_{on} of the current paths. The diagram illustrates that although out_1 of High, $out_{1,2}$ of Double Boost and out_2 of Super Boost modes, which altogether share the same gain of ($2V_{in}$) are configured differently with different switches, out_1 of High and $out_{1,2}$ of Double Boost modes provides the same I-V characteristic, since they overlapped, and closely match with Super's out_2 line. The output current from 5.19-50.7 μ A can be expected from the converter.

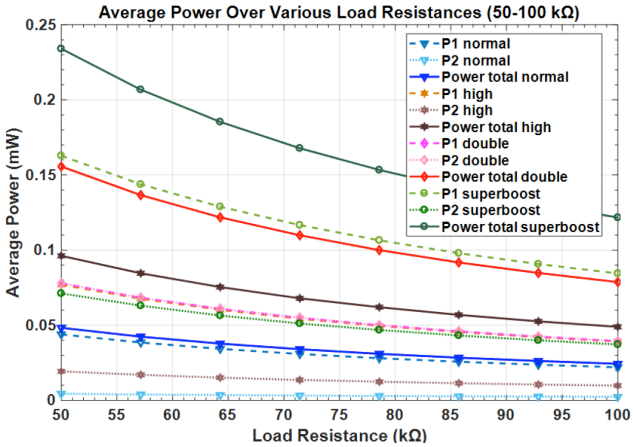

FIGURE 8. Average output power for varying loads tested with 50-100 kΩ.

The converter average output power varies across the different load of 50-100 kΩ as shown in Fig. 8. It demonstrates the average low power output range from 0.0023-0.23 mW. Therefore, this power system is also suitable for the implantable system. Due to target output values are the same ($\times$2 gain) for P1 double, P2 double and P1 high, it is observed that there are some overlapping performance lines as shown in Fig. 8. These overlapping lines suggest that the proposed

TABLE 3. Comparison of proposed work with state-of-the-art.

Specification	This work 180 nm Simulated	[26] 40nm Integrated	[24] 45nm Simulated	[25] 90nm Integrated	[23] 350nm Integrated
Input (V)	1	3.7	1	1.2	1.1-1.8
Output (V)	1.49, 0.47	1.8, 0.8	0.66, 0.33,1	0.76, 0.32	2, 3
	1.91, 0.98	-	-	-	
	1.97, 1.97	-	-	-	
	2.85, 1.88	-	-	-	
I_{load} (mA)	0.04, 0.06, 0.08, 0.1	0.4, - 1	-	0.4, 0.9	12
Conversion Ratios	3/2, 1/2 or 2, 1 or 2, 2 or 3, 2	1/2, 1/4	2/3, 1/3, 1	1/2, 2/3	3, 2 or 2, 2
P_{out_max}(mW)	0.23	1.3	1.3	1	60
Ripple (mV)	14-59	60	9.6	19.5-40.6	
Max Efficiency (%)	85.26	70	90	68	90
Capacitor (F)	1n ×4	2.24n × (≥2)	3.7n × (≥4)	5n×2 6n×2	4.7µ ×2

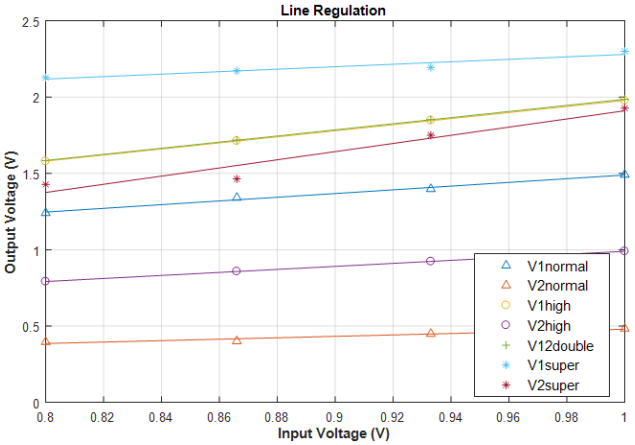

FIGURE 9. Line regulation tested with the charging input of 1-0.8 V at 100 kΩ.

converter maintains the stable performances for the different configurations and the different switches of the same output. Assuming input integrated battery degrades over time or supplied PV cell power degrades at night time, line regulation with varying inputs of 1-0.8 V, simulated with a fixed load of 100 kΩ and the results shown in Fig. 9. Although the output voltages reduce from targeted values due to input changes, the linear line indicates that the converter still maintains correct gain operation relative to a given input.

The conduction power losses are calculated by inserting simulated result values into the (2); has resulted in 0.759 μW and 0.077 μW respectively for $P_{conduct\_Norm(boost,buck)}$, and 0.9239 μW and 0.231 μWn for $P_{conduct\_High(boost,buck)}$. Similarly, 1.216 μWn for $P_{conduct\_DoubleBoost}$ and, 1.14 μWn and 0.5013 μWn for $P_{conduct(out1,out2)SuperBoost}$ respectively. Also, the switching power losses are calculated using (3) produces 4.3411×10^{-19} W for P_{sw_Norm}, 6.714×10^{-19} W for P_{sw_High}, 1.25×10^{-18} W for $P_{sw\_DoubleBoost}$, and 4.89×10^{-18} W for $P_{sw\_SuperBoost}$. Redistribution losses in (4) for all modes is 2.413 μW, 4.317 μWnn, 2.094 μWn and 2.929 μWnn respectively. Simulated input power for all modes are 485.7 μW, 104 μWn, 107.1 μWn and 316.6 μWn respectively. Likewise, simulated power consumption at digital modules are 80.82 μW, 27.99 μW, 0.184 mW and 0.6189 mW respectively. Observed that for Super and Double modes digital modules consume huge power from high frequencies operations. The efficiency of the converter is simulated from output power divided input power for all four modes yields 85.257%, 72.884%, 53.6% and 47.85% respectively.

The recent state-of-the-art SIDO SC designs can only produce fixed gain ratios as summarised in Table 3. Apart from [24], which produces spontaneous three fixed different voltages (SIMO), the rest of the designs in comparisons are SIDO designs.

Depending on the application and required output power and availability of chip area, most of the designs use Nano Farad size capacitors and typically employed 4 flying capacitors for dual output designs. In achieving multioutput integrated battery-powered system-on-chip SC converter, in [26] the conversion efficiency significantly dropped due to cascading 2:1 converter twice to get 1/2 and subsequent 1/4 outputs. However, for a huge input range, this fixed ratio configuration can be highly inefficient in contrary to this proposed design. Same can be said for the SC converters in [24] and [25] which have the fixed output gain setting. This proposed design and [23] are not only accessible for simultaneous step-up and step-down conversions whilst most of SIDO converters are only enable simultaneous down conversions, but also allow converter to reconfigure into different gains.

However, the converter has [23] some idle time for every 180-degree phase shift due to it going back to the charging phase and our proposed topology can simultaneous outputs the different gains at the same time. Moreover, our proposed work has by far the highest reconfigurability for SIDO design since it can configure 4 different gain pairs. Lastly, the efficiency values agree with the state-of-the-art SIMO and SIDO converters.

V. CONCLUSION AND FUTURE WORK

This paper describes the novel topology of switched-capacitor approach for 4-phases rotation scheme to yield simultaneous dual outputs conversions for multi-functional implantable applications with internally integrated electronic modules. This topology has fulfilled the gap of reconfigurability in SIDO converters, fast response time and offers an ability to reconfigure the converter into a step up or down gain ratios for simultaneous outputs. This prevents efficiency degrading in wide input range since the large range of gain pairs are accessible.

Moreover, the efficiency degrading in higher conversions such as double and super boost modes are from leakage current in between the phase-changes transitions, govern by the higher frequency switching. This can be minimised by having a phase controller to readjusting the non-overlapping dead time region. Once the proper controllers are introduced, the efficiency of the converter will improve significantly, and dual outputs design will lead to self-power the system, whilst powering to the load.

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KAUNG OO HTET was born in Yangon, Burma. received the B.Eng. degree (Hons.) in electronic engineering from the University of Birmingham, the M.Sc. degree (Hons.) in automation and control from Newcastle University in 2013, and the M.Phil. degree in autonomous power system for bio device from Newcastle University in 2016. He is currently pursuing the Ph.D. degree with the Microelectronics Lab (meLAB), University of Glasgow, under the supervision of Dr. H. Heidari. He also achieved his BITE Award (Distinctions) and HND Foundation (Merits) from the Wigan and Leigh College in 2008–2009.

His research interest is integrated power management system for wearable and implantable devices. He was also awarded excellence First Prize Poster Award in 17th Annual Research Conference, Newcastle University, and the IEEE ISCAS 2018 Conference Travel Grant. He was a liaison representative for IEEE community and hosted a few IEEE conferences and seminars in Newcastle University, which brought students, industry, and the IEEE community together.

RAMI GHANNAM received the B.Eng. degree (Hons.) from King's College, and the DIC and M.Sc. degrees from Imperial College London. He is currently a Lecturer in electronic and electrical engineering with research interests in the broad field of photonics. Following his Ph.D. from Cambridge University in 2007, he has spent the past 10 years in the field of photovoltaics. He has held previous industrial appointments at Nortel Networks, IBM Research GmbH, and Starkon S.A.E. He is also a member of the Microelectronics Laboratory, where he is investigating the use of PV cells for energy harvesting applications in wearable and implantable electronic devices.

QAMMER H. ABBASI (SM'16) received the B.Sc. and M.Sc. degrees (Hons.) in electronics and telecommunication engineering from the University of Engineering and Technology (UET), Lahore, Pakistan, and the Ph.D. degree in electronic and electrical engineering from the Queen Mary University of London(QMUL), U.K., in 2012. In 2012, he was a Post-Doctoral Research Assistant with the Antenna and Electromagnetics Group, QMUL. From 2012 to 2013, he was international young Scientist under the National Science Foundation China, and an Assistant Professor with UET, KSK, Lahore. From 2013 to 2017, he was with the Centre for Remote Healthcare Technology and Wireless Research Group, Department of Electrical and Computer Engineering, Texas A&M University (TAMUQ) initially as an Assistant Research Scientist and later was promoted to an Associate Research Scientist and a Visiting Lecturer, where he was leading multiple Qatar national research foundation grants (worth 3 million). He is currently a Lecturer (Assistant Professor) with the School of Engineering, University of Glasgow, U.K., in addition, he is also a Visiting Research Fellow with QMUL and a Visiting Associate Research Scientist with TAMUQ. He has been mentoring several undergraduate, graduate students, and post-docs. He has contributed to a patent, over 150 leading international technical journal, peer reviewed conference papers, and five books. He has also received several recognitions for his research including the University Research Excellence Award from TAMUQ in two consecutive years, the Reward for Exellence from the University of Glasgow, exceptional talent endorsement (awarded to early career world-leading innovators and scientists) by the Royal Academy of Engineering, and most downloaded paper in the IEEE Terahertz Transaction. Media coverage by Analog IC tips, Microwaves & RF Newsletters, Vertical News. His research interests include compact antenna design, RF design and radio propagation, nano communication, biomedical applications of terahertz communication, antenna interaction with human body, implants, body centric wireless communication issues, wireless body sensor networks, non-invasive health care solutions, cognitive and cooperative network, and multiple-input-multiple-output systems. He has been a member of the technical program committees of several IEEE flagship conferences. He is an Associate Editor for the IEEE Access journal, the IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology and acted as a guest editor for numerous special issues in top notch journals. He has been a technical reviewer for several IEEE and top-notch journals. He contributed in organizing several IEEE conferences, workshop, and special sessions in addition to European school of antenna course.

HADI HEIDARI (M'15–SM'17) received the Ph.D. degree in microelectronics from the University of Pavia, Italy, in 2015, where he was involved in integrated CMOS sensory microsystems. He is currently a Lecturer (Assistant Professor) with the School of Engineering and the Lead of the Microelectronics Lab, University of Glasgow, U.K. He has authored over 60 articles in peer reviewed journals (e.g., the IEEE Solid-State Circuits Journal, Transactions on Circuits and Systems I, and the IEEE Transactions on Electron Devices) and in international conferences. He is a member of the IEEE Circuits and Systems Society Board of Governors, the IEEE Sensors Council, and the IEEE Solid-State Circuits Society Administrative Committee. He has received several best paper awards from the IEEE international conferences including ISCAS'14, PRIME'14, ISSCC'16, and travel scholarship from IEEE NGCAS'17. He has been a recipient of the Gold Leaf award from the IEEE PRIME 2014 Conference and the Silk Road Award from the International Solid-State Circuits Conference 2016. He has organised several conferences, workshops, and special sessions, e.g., he was a member of organising committee of SENSORS 2017–2018 and BioCAS 2018, and a General Chair of U.K.-China Emerging Technology 2017. He is an Editor for the Elsevier *Microelectronics Journal* and a Lead Guest Editor for four journal special issues. He has grant portfolio of č1 million funded by major research councils and funding organizations including European Commission, U.K.'s Royal Society, and Scottish Funding Council.