Performance enhancement of Al_2O_3/H-diamond MOSFETs utilizing vacuum annealing and V_2O_5 as a surface electron acceptor

David A. Macdonald, Kevin G. Crawford, Alexandre Tallaire, Riadh Issaoui and David A.J. Moran

***Abstract*— We report on the performance enhancement of 250 nm gate-length H-diamond FETs through thermal treatment of devices at 400°C and the incorporation of V_2O_5 as a surface electron acceptor layer. Encapsulation of the H-diamond surface with V_2O_5 is found to increase the transfer doping efficiency and reduce device access resistance. A reduction in ohmic contact resistance and channel resistance beneath the gate after thermal treatment at 400°C was found to further reduce device on-resistance and increase the maximum drain current and peak transconductance. These devices demonstrate the highest drain current (375 mA/mm) and transconductance (98 mS/mm) yet reported for H-diamond FETs of this gate length that incorporate an electron acceptor oxide layer.**

***Index Terms*—Diamond, FETs, Transfer Doping, V_2O_5**

I. Introduction

DIAMOND possesses many unique properties that make it attractive for the production of high performance semiconductor devices [1]. A large bandgap of 5.5 eV, high thermal conductivity of up to 20 $Wcm^{-1}K^{-1}$ and high carrier saturation velocity of 2×10^7 cm^{-1} for electrons and 0.8×10^7 cm^{-1} for holes make diamond of particular interest for the production of robust, high power and high frequency field effect transistors. Despite diamond's electronic potential, development of a mature electronic device technology has been limited by the immaturity of existing doping processes used to introduce mobile charge into its naturally insulating crystal structure. 'Transfer doping' of hydrogen-terminated diamond (H-diamond) presents a potential solution to this challenge which has allowed for the production of high performance FETs in terms of both high power [2] and high frequency operation [3]. Transfer doping of H-diamond has traditionally relied on the adventitious adsorption of air-borne electron-acceptor species onto the diamond surface when exposed to atmosphere however [4], and thus suffers from acute environmental and temperature sensitivity and associated instability [5]. Recent work by various groups has demonstrated significant advancements in the efficiency and stability of transfer-doped H-diamond by replacing the adsorbed surface atmospheric species with high electron affinity **electron-acceptor oxide (EAO)** materials such as MoO_3 [6][7], V_2O_5 [8][9], WO_3[9][10], Nb_2O_5[9] and ReO_3[10]. Though encouraging progress has recently been reported for FET devices that incorporate some of these EAO materials [11-13], the challenges associated with their integration into a diamond FET architecture and associated process flow have thus far limited their full potential to enhance both device performance and stability of operation. Furthermore, it was recently demonstrated that treatment of the H-diamond surface with a 400°C anneal prior to deposition of EAOs MoO_3 and V_2O_5 is required to ensure stability of doping with time [5], thus placing additional thermal constraints on the processing required to integrate these materials into real devices. Although some work has already investigated the impact of exposure of more traditional H-diamond FET devices to temperatures up to 400°C e.g. [14,15], little has as-yet been reported on the impact of such high temperature processing on devices that incorporate an EAO layer.

We report on a new fabrication strategy for the production of H-diamond FETs that incorporate V_2O_5 as an EAO layer following a 400°C anneal stage. These devices demonstrate the highest drain current and transconductance yet reported for EAO-enhanced diamond FETs with a gate length of 250 nm and a substantial performance increase in comparison with their "atmospheric-doped" counterparts.

II. Experimental

4.5 × 4.5 mm monocrystalline (001) substrates procured from Element Six were used for this work. Substrates were cleaned in a boiling acid solution of H_2SO_4:HNO_3 for 1 hour then treated with hydrogen plasma at a power of 2.6 kW and substrate temperature of 650°C for 45 minutes as discussed in [16]. Roughness of the H-diamond surface was measured by AFM to be 0.5 nm RMS. The processing steps utilized for the fabrication of FETs are summarized as follows: 1) An 80 nm thick Au layer was evaporated by electron beam across the H-diamond surface. 2) Electrical isolation of devices was performed using photolithography, etching of the Au layer in the resultant unmasked regions using KI etch solution and then

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treatment of the exposed H-diamond surface to oxygen plasma. 3) Removal of the gold from the active regions of test structures such as TLMs and VDPs was performed using photolithography and KI etch solution, forming the ohmic contacts for these structures from the remaining Au layer. 4) 250 nm long gate contacts were defined for devices with a width of 50 µm by electron beam lithography and the source and drain Au ohmic contacts formed at a separation of 2.5 µm by KI wet etch. 5) 10 nm Al_2O_3 / 20 nm Al / 20 nm Pt / 40 nm Au was deposited by electron beam evaporation and lifted off to form the gate stack. A cross section showing the device structure at this stage is presented in Fig. 1a. 6) The substrate was annealed at 400°C for 45 minutes *in-situ* at a vacuum of 1 × 10^{-6} mbar and left to cool to 50°C under vacuum before 10 nm of V_2O_5 was thermally evaporated across the surface. A cross section of the final device architecture is presented in Fig. 1b.

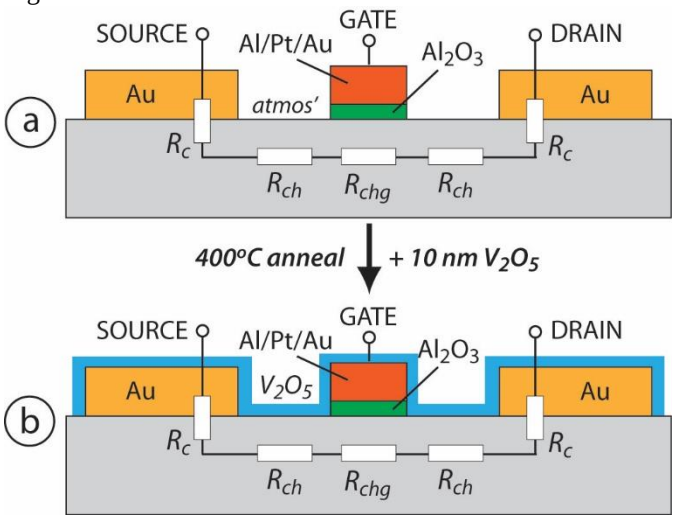

Fig. 1. Cross section schematic of FET devices with (a) the access region exposed to atmosphere ("Atmos-FET") and (b) the access region encapsulated with 10nm V_2O_5 ("V_2O_5-FET").

III. Results

DC characterization of the same devices was performed before and after the 400°C anneal and V_2O_5 deposition stage. This allowed for comparison between FETs with the access regions exposed to atmosphere (henceforth referred to as "Atmos-FETs"), shown in Fig. 1a, with exactly the same devices after a 400°C anneal and encapsulation with 10 nm V_2O_5 (henceforth referred to as "V_2O_5-FETs"), shown in Fig. 1b. Typical output (I_d,I_g:V_{ds}) and transfer characteristics (I_d,g_m:V_{gs}) for an Atmos-FET are presented in Figs. 2 and 3 respectively. The output and transfer characteristics for the same device (V_2O_5-FET) following the 400°C anneal and encapsulation with 10 nm V_2O_5 are then presented in Figs. 4 and 5 respectively.

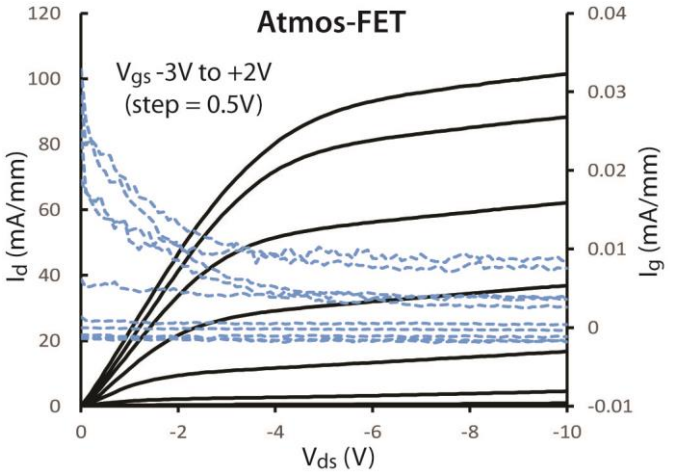

Fig. 2. Output characteristics for an Atmos-FET device (Fig. 1a) showing drain current, I_d (continuous line) and gate current, I_g (broken line) vs. source-drain voltage, V_{ds} for gate voltage, V_{gs} from -3V to +2V.

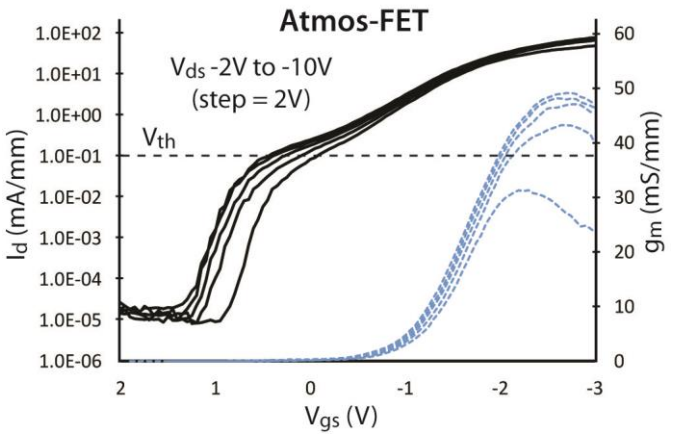

Fig. 3. Transfer characteristics for an Atmos-FET device (Fig. 1a) showing drain current, I_d (continuous line) and transconductance, g_m (broken line) vs. gate-source voltage, V_{gs} for source-drain voltage, V_{ds} from -2V to -10V.

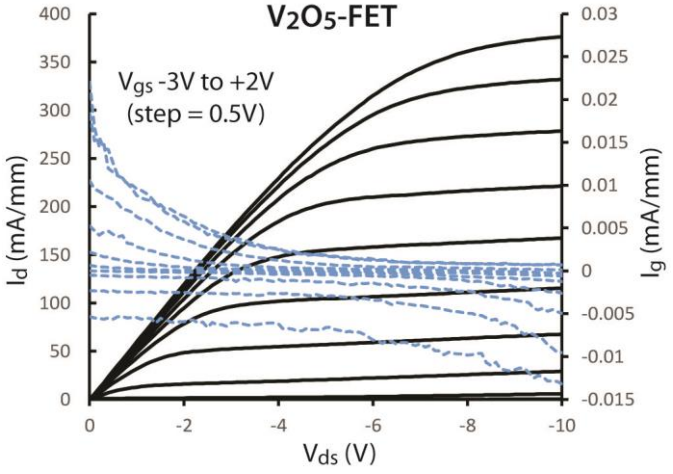

Fig. 4. Output characteristics for a V_2O_5-FET device (Fig. 1b) showing drain current, I_d (continuous line) and gate current, I_g (broken line) vs. source-drain voltage, V_{ds} for gate voltage, V_{gs} from -3V to +2V.

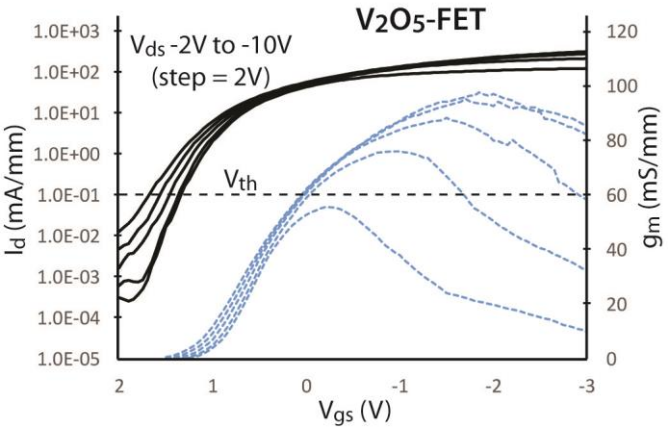

Fig. 5. Transfer characteristics for a V_2O_5-FET device (Fig. 1b) showing drain current, I_d (continuous line) and transconductance, g_m (broken line) vs. gate-source voltage, V_{gs} for source-drain voltage, V_{ds} from -2V to -10V.

A summary of device parameters and performance metrics as extracted from DC characterisation as well as TLM and VDP test structures is provided in Table I.

Table I
Comparison of extracted FET parameters

FET parameter	**Atmos-FET**	**V_2O_5-FET**
R_{on} (Ω.mm)	43.9	16.8
R_c (Ω.mm)	9.0	3.0
R_{ch} (Ω.mm)	7.9	4.2
R_{ch} (Ω/□)	7000	3700
R_{chg} (Ω.mm)	10.1	2.5
$I_{d\text{-}max}$ (mA/mm)	~ 100	~ 375
$I_{g\text{-}max}$ (mA/mm)	0.033	0.022
Peak $g_{m\text{-}ext}$ (mS/mm)	49	98
Peak $g_{m\text{-}int}$ (mS/mm)	287	325
V_{th} (V)	0.45	1.7

Where R_c, R_{ch} and R_{chg} represent the contact resistance, lateral channel resistance between the ohmic contacts and gate, and channel resistance beneath the gate contact respectively (as denoted in Fig. 1).

Extraction of the resistance figures presented in Table I. relied on two assumptions: 1. the contact resistance values for the source and drain ohmic contacts (R_c) are equal and 2. the source-gate and gate-drain channel resistances (R_{ch}) are also equal due to the symmetric positioning of the gate between the ohmic contacts. The device on-resistance (R_{on}), which is extracted from the linear region of the device output characteristics, may therefore be expressed as:

$$R_{on} = 2R_c + 2R_{ch} + R_{chg} \quad (1)$$

where R_{chg} is the channel resistance beneath the gate. The intrinsic transconductance values ($g_{m\text{-}int}$) were then extracted using the following expression [17]:

$$g_{m-int} = \frac{g_{m-ext}}{1 - (R_c + R_{ch})\, g_{m-ext}} \quad (2)$$

where $g_{m\text{-}ext}$ is the measured, extrinsic device transconductance and R_c and R_{ch} were extracted from TLM and VDP measurements.

IV. Discussion

Good transistor action is realized with both the Atmos-FET and V_2O_5-FET devices, with low and similar gate leakage achieved for both across the inspected bias range. A substantial increase in performance is observed following the anneal and V_2O_5 deposition however, including an increase in maximum drain current, $I_{d\text{-}max}$, from 100 to 375 mA/mm, an increase in extrinsic transconductance, $g_{m\text{-}ext}$, from 49 to 98 mS/mm and a reduction in on-resistance, R_{on}, from 43.9 to 16.8 Ω.mm. Although this is the highest drain current and transconductance yet reported for an EAO-enhanced H-diamond FET, the use of a relatively small gate length in these devices (in comparison with other reported technologies [11–13]) may further contribute to this enhanced performance. The performance enhancement observed between the Atmos-FET and V_2O_5-FET however may in part be attributed to the higher doping efficiency and associated reduction in sheet resistance (from 7000 to 3700 Ω/□ as verified by VDP measurement) in the V_2O_5-encapsulated access regions (R_{ch} in Fig. 1). This is complemented by a reduction in ohmic contact resistance (R_c) from 9 to 3 Ω.mm that is also observed following the 400°C anneal and deposition of V_2O_5. The mechanism for this reduction in contact resistance is at present not well understood and requires deeper investigation beyond the scope of this work. Further inspection of the series components of the device on-resistance, R_{on}, (as shown in (1)), also indicate a reduction in the equivalent channel resistance beneath the gate (R_{chg}) following the anneal and deposition of V_2O_5. This is likely attributed to thermally induced modification of the Al_2O_3/H-diamond interface by the 400°C anneal. The shift in threshold voltage (extracted at I_d = 0.1 mA/mm and V_{ds} = -10 V) from 0.45 to 1.7 V and increase in intrinsic transconductance from 287 to 325 mS/mm (extracted utilizing equation (2)) also strongly suggest modification to the intrinsic gate contact, most likely resulting from the 400°C anneal. Although a model to describe the formation of the 2D hole channel at the H-diamond/Al_2O_3 interface has recently been proposed for ALD-deposited Al_2O_3 [18], this mechanism may not apply to electron-beam evaporated Al_2O_3 as used in this work. The role of potential residual atmospheric adsorbates between the diamond and Al_2O_3 may also play an important role in these devices and warrants further investigation. Deeper investigation into thermal modification to the H-diamond interface with both the Au ohmic contact metal and Al_2O_3 gate dielectric layer is therefore required to better understand and exploit these mechanisms to further enhance H-diamond FET performance. These results however demonstrate a promising new approach for the integration of EAO materials into H-diamond FET technology for enhanced device performance.

V. Conclusion

H-diamond FETs incorporating an Al_2O_3 gate dielectric layer were realized and characterized before and after treatment with a 400°C thermal anneal and encapsulation with a thin film of V_2O_5. On-resistance of devices was reduced due

to a combination of reduced access resistance attributed to the V_2O_5 layer, and lowered ohmic contact and channel resistances most likely associated with the 400°C anneal. This led to a substantial increase in both device transconductance and maximum drain current. These results demonstrate a new strategy for the integration of EAO materials such as V_2O_5 into H-diamond FET technology to substantially enhance performance. Further work is now required to better understand the operation of the H-diamond interfaces in these devices and their role in device operation and reliability.

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