Impact of stress in ICP-CVD SiN$_x$ passivation films on the leakage current in AlGaN/GaN HEMTs

S.-J. Cho, X. Li, I. Guiney, K. Floros, D. Hemakumara, D.J. Wallis, C. Humphreys and I.G. Thayne

The impact of the stress in room temperature inductively coupled plasma chemical vapour deposited (ICP-CVD) SiN$_x$ surface passivation layers on off-state drain ($I_{DS-off}$) and gate leakage currents ($I_{GS}$) in AlGaN/GaN high electron mobility transistors (HEMTs) is reported. $I_{DS-off}$ and $I_{GS}$ in 2 μm gate length devices were reduced by up to four orders of magnitude to ~10 pA/mm using a compressively stressed bilayer SiN$_x$ passivation scheme. In addition, $L_{sat}/I_{DS}$ of ~10$^4$ and sub-threshold slope of 68 mV/dec were obtained using this strain engineered surface passivation approach.

Introduction: AlGaN/GaN HEMTs are a promising candidate for power and RF electronics due to the high breakdown voltage, high electron saturation velocity and good thermal stability of the GaN-based material system [1, 2]. Off-state drain to source ($I_{DS-off}$) and gate leakage ($I_{GS}$) currents must be minimised in devices to improve the efficiency of their power switching. To reduce leakage currents, Al$_2$O$_3$ passivation deposited by atomic layer deposition, wet chemical or plasma surface treatment before passivation and annealing after gate metal deposition have been reported [3–6]. SiN$_x$ has been widely used for surface passivation between the transistor gate and drain and shown to be effective in reducing current collapse and DC-TO RF dispersion arising from the large density of surface states and trapped surface charge [7]. Optimisation of the properties of the SiN$_x$ passivation film has been reported, including the impact of stress in the SiN$_x$ film on the properties of an AlGaN/GaN HEMT by Gregusová et al. [8]. Fehlberg et al. [9] used Hall Bars to investigate the impact of stress in SiN$_x$ deposited films on the electrical transport properties of AlGaN/GaN heterostructures. To date, all reports on the impact of stressed SiN$_x$ films have been restricted to passivation layers deposited by plasma enhanced chemical vapour deposition (PECVD) techniques with a maximum compressive stress of 150 MPa. Moreover, the use of SiN$_x$ by PECVD as a surface passivant can result in increased $I_{DS-off}$ and $I_{GS}$ [10]. To mitigate these effects, in this Letter, we compare the impact of both tensile and compressive stress in the range of -1622 to +440 MPa in room temperature deposited ICP-CVD SiN$_x$ surface passivation films on AlGaN/GaN HEMTs. A significant reduction in $I_{DS-off}$ and $I_{GS}$ was observed for the optimally stressed films.

Fabrication process: The AlGaN/GaN heterostructure epi-layers of this study were grown on a silicon substrate by metal organic chemical vapour deposition. From the substrate, the layer structure comprised a 0.25 μm AlN nucleation layer; a 27 nm Al$_{0.27}$Ga$_{0.73}$N barrier and a 2 nm GaN cap layer. Transistors were fabricated by first depositing 70 nm SiN$_x$ films using process (I) in Table 1 followed by the higher stress films (II to V) of Table 1. A ‘typical bilayer’ films are shown in Figs. 1b and 2b.

Table 1: Stress conditions and type of SiN$_x$

<table>
<thead>
<tr>
<th>Ref</th>
<th>ICP power, W</th>
<th>Platen power, W</th>
<th>Chamber pressure, mT</th>
<th>Stress, MPa</th>
<th>Refractive index</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I)</td>
<td>200</td>
<td>0</td>
<td>5</td>
<td>-280 (compressive)</td>
<td>2.01</td>
</tr>
<tr>
<td>(II)</td>
<td>200</td>
<td>4</td>
<td>5</td>
<td>-616 (compressive)</td>
<td>1.99</td>
</tr>
<tr>
<td>(III)</td>
<td>300</td>
<td>4</td>
<td>5</td>
<td>-1163 (compressive)</td>
<td>1.93</td>
</tr>
<tr>
<td>(IV)</td>
<td>300</td>
<td>8</td>
<td>5</td>
<td>-1622 (compressive)</td>
<td>1.89</td>
</tr>
<tr>
<td>(V)</td>
<td>300</td>
<td>0</td>
<td>7</td>
<td>+440 (tensile)</td>
<td>1.72</td>
</tr>
</tbody>
</table>

Fig. 1 Cross-section of surface passivation
- ‘High’ stressed single layer surface passivation
- ‘High/conventional’ stressed bilayer surface passivation

Measurement results and discussion: Fig. 3 shows room temperature electron mobility ($\mu_x$) and carrier concentration ($n_x$) as a function of various stress of SiN$_x$, bilayer as determined by Van der Pauw test structure measurement. Electron mobility is increased and carrier concentration is decreased as a consequence of highly compressive stress of SiN$_x$. This suggests either highly compressive stress of SiN$_x$ passivation schemes have reduction of net positive charge effect at the GaN surface and/or the presence of fixed positive charge in the SiN$_x$ films [12].

Fig. 2 SEM image of surface passivation
- ‘High’ stressed single layer surface passivation
- ‘High/conventional’ stressed bilayer surface passivation

Fig. 3 Room temperature Van der Pauw evaluation
- Stress-electron mobility by various passivation schemes
- Stress-carrier concentration by various passivation schemes

Fig. 4a shows semi-log scale $I_{GS}$–$V_{GS}$ and $I_{DS}$–$V_{DS}$ characteristics for the single and bilayer passivation schemes and are compared with unpassivated devices. The incorporation of passivation (I)+(II) and (I)+(V) result in three orders of magnitude increase in $I_{DS-off}$ and $I_{GS}$, when compared to unpassivated devices which have leakage currents of order 10 nA/mm. In contrast, devices with passivation (I)+(IV) have around four orders of magnitude reduction in $I_{DS-off}$ and $I_{GS}$, when compared to unpassivated devices. Devices with passivation (I)+(IV) demonstrated $L_{sat}/I_{DS}$ ratio of ~10$^4$ and sub-threshold slope of 68 mV/dec. Fig. 4b shows reverse Schottky gate leakage comparison...
of unpassivated and various stressed SiN$_x$ surface passivation schemes. The rank of Schottky reverse bias leakage is same as $I_{GS}$ leakage of Fig. 4a. Figs. 5a and b, respectively, show the $I_{DS}$-$V_{GS}$ three terminal off-state leakage current and $I_{GS}$-$V_{DS}$ lateral isolated leakage current ($I_{lateral}$) characteristics for the various passivation schemes. These clearly show the bilayer passivation (I) + (IV) is optimal in reducing these contributors to device leakage current.

**Fig. 4** Semi-log scale off-state and gate leakage comparison of unpassivated and various stressed SiN$_x$ surface passivation schemes

- a $I_{GS}$-$V_{GS}$ and $I_{DS}$-$V_{DS}$ comparison ($W_{C}=100$ μm, $L_{C}=2$ μm, $L_{D}=2$ μm, $L_{X}=7$ μm)
- b Reverse Schottky gate leakage comparison

**Fig. 5** Semi-log scale off-state and lateral isolated leakage comparison of unpassivated and various stressed SiN$_x$ surface passivation schemes

- a $I_{DS}$-$V_{GS}$ and $I_{GS}$-$V_{DS}$ off-state leakage current characteristics ($W_{C}=100$ μm, $L_{C}=2$ μm, $L_{D}=2$ μm, $L_{X}=7$ μm)
- b Lateral isolated leakage current characteristics

**Conclusion:** In this Letter, the impact of stress in ICP-CVD SiN$_x$ surface passivation layers deposited at room temperature on $I_{DS,off}$ and $I_{GS}$ in AlGaN/GaN HEMTs is assessed. The use of a bilayer SiN$_x$ passivation scheme comprising 70 nm 280 MPa compressively strained film followed by a 150 nm 1.6 GPa compressively strained layer resulted in $I_{DS,off}$ and $I_{GS}$ reduction by up to four orders of magnitude when compared to unpassivated devices and up to seven orders of magnitude in comparison with devices with a single 70 nm 280 MPa compressively strained passivation layer. $I_{DS,off}$ and $I_{GS}$ of ~10 pA/mm, $I_{lateral}$ of $\sim 10^{-12}$ and subthreshold slope of 68 mV/dec are obtained using the optimal process.

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One or more of the Figures in this Letter are available in colour online.

S.-J. Cho, X. Li, K. Floros, D. Hemakumara and I.G. Thayne (School of Engineering, University of Glasgow, Glasgow G12 8LT, United Kingdom)

✉ E-mail: Sung-Jin.Cho@glasgow.ac.uk

I. Guiney, D.J. Wallis and C. Humphreys (Department of Materials Science & Metallurgy, University of Cambridge, Cambridge CB3 0FS, United Kingdom)

References