A review of the Z^2-FET 1T-DRAM memory: Operation mechanisms and key parameters

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Abstract

The band-modulation and sharp-switching mechanisms in Z^2-FET device operated as a capacitorless 1T-DRAM memory are reviewed. The main parameters that govern the memory performance are discussed based on detailed experiments and simulations. This 1T-DRAM memory does not suffer from super-coupling effect and can be integrated in sub-10 nm thick SOI films. It offers low leakage current, high current margin, long retention, low operating voltage especially for programming, and high speed. The Z^2-FET is suitable for embedded memory applications.

Introduction

The DRAM (Dynamic Random Access Memory) cell, composed of a MOSFET and a charge-storage capacitor, needs to be billion-times cloned, which implies aggressive scaling. While the transistor miniaturization is still going on, the size of the capacitor cannot be easily shrunk further without adversely affecting the amount of stored charge required to discriminate the memory states '0' and '1'. An ineluctable paradigm shift consists in simply suppressing the capacitor. Devices with isolated body (such as planar SOI MOSFET, FinFET on SOI, nanowires, etc) are attractive in this respect: the charge is stored within the floating body of the transistor which is also used to read the memory state.

The concept of single-transistor DRAM (1T-DRAM) came out more than 20 years ago [1] and many enthusiastic variants have since been proposed [2-24]. In general, 1T-DRAMs take advantage of the floating-body effects that were usually regarded as parasitic and detrimental. In '1' state, excess majority carriers (holes) are stored in the body and increase the potential, lower the threshold voltage and yield high current. State '0' features lower current achieved by removing the holes from the body.

However, 1T-DRAMs have not yet reached the market for two main reasons:

- Conventional DRAMs were pacing successfully and there was no emergency for replacement.
- None of the 1T-DRAM versions was entirely convincing. Either the writing mechanisms were too demanding in power/voltage/reliability or the device compatibility with standard FDSOI process was limited.

After a first round of selection, we have retained and compared three promising variants: MSDRAM, A2RAM and Z^2-FET. The MSDRAM is based on the Meta-Stable Dip (MSD) hysteresis effect [14]. The back channel of a regular FDSOI N-MOSFET is biased in moderate inversion and the front gate V_{GF} is swept from strong to moderate accumulation. For high negative V_{GF}, band-to-band tunneling (BTBT) rapidly supplies holes in the front channel. Since the memory is at equilibrium, a high current flows at the back channel (state '1'). In state '0', V_{GF} is pulsed from depletion to moderate accumulation; since there is no source to generate holes fast enough, the body potential drops in deep depletion, temporarily suppressing the back-channel current. Relatively thick MSDRAMs feature wide memory window (hysteresis), high memory margin I_1/I_0 and seconds-long retention. The fatal issue is film thinning used in advanced FDSOI technology [15]. Below 10 nm, the super-coupling effect denies the co-existence of electron and hole channels facing each-other [25-27]. The MSD effect vanishes because the electron channel is needed to read the memory state, while the hole channel serves for charge storage.

The A2RAM is similar to the MSDRAM except that the back electron channel has 'physical' doping (N^+ bridge synthesized by ion-implantation or epitaxial growth) instead of 'electrostatic' doping induced by the back gate [19-20]. When holes are stored in the body, the bridge connects the source and drain and the current I_1 is high. If no holes are available for $V_{GF} < 0$, the body and the bridge are fully depleted and the current I_0 is interrupted. Experimental results indicate

promising performance but again the film thinning looks as a show-stopper. The fabrication and variability of the bridge in films with sub-10 nm overall thickness are challenging.

For these reasons, we have finally decided to focus on the Z^2-FET memory [22-24]. The Z^2-FET is a PIN diode with large gate underlap (Fig. 1), similar to a TFET but operated in forward-bias mode. Electrostatic barriers are formed, via gate disposition and biasing, to prevent electron/hole injection into the channel until the gate or drain bias reaches a turn-on value. The front and back gates induce electrostatic doping in the undoped body so the device looks like a N^+PNP^+ thyristor, although the mechanisms of operation differ [28]. The gate action leads to band modulation along the channel that blocks the current flow. A positive feedback mechanism between the electron and hole injection barriers causes the device to abruptly switch (< 1 mV/decade) from OFF state with low leakage current to ON state with high drive current. The output I-V characteristics (Fig. 2) exhibit a large hysteresis useful for single-transistor memory (1T-DRAM). Other band-modulation devices have recently been proposed for sharp switching, ESD protection, and memory applications [21, 29-32].

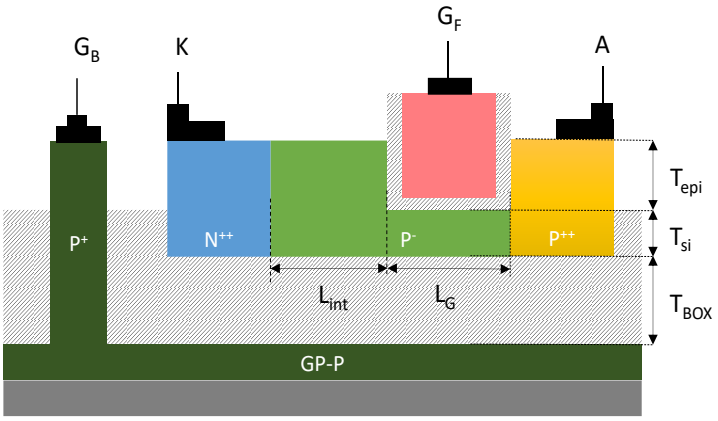

Fig. 1. Schematics of Z^2-FET fabricated with 28 nm FDSOI technology.

In section 2, the difference between the various modes of operation (steady-state, transient and memory) will be outlined. We present experimental results and discuss in detail the device physics, architecture, and processing steps of the Z^2-FET. The memory performance is investigated by systematic measurements revealing the roles of gate/anode bias, program and read pulses, temperature and geometrical parameters. The memory mechanism is rather subtle. It is clarified in section 3 with numerical simulations that illustrate step-by-step the change in energy barriers and carrier concentration during the memory cycling. These simulations offer guidelines for developing physics and compact models needed in device optimization.

2. Experimental results

2.1. Device fabrication

The Z^2-FET is a partially gated P-I-N diode illustrated in Fig. 1. The cathode (N^+ doped source) is grounded and the anode (P^+ doped drain) is positively biased. In 28 nm FDSOI [33] technology, the Z^2-FET features undoped ultrathin silicon film (t_{SI} = 7 nm), thin buried oxide (t_{BOX} = 25 nm) and raised epitaxial layer (t_{epi} = 15 nm) in the drain, source and ungated regions

to reduce the series resistance [34]. The front-gate ($V_{GF} > 0$) and back-gate (ground-plane, $V_{GB} < 0$) are biased to form a virtual NPNP structure, blocking the electron injection from cathode and the hole injection from anode.

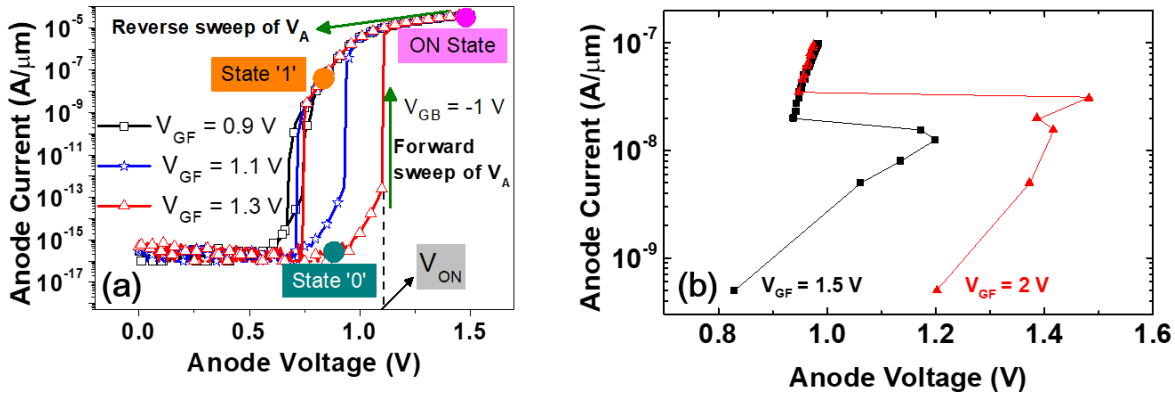

Fig. 2. Experimental I_A-V_A curves for different gate voltages in quasi steady-state (DC mode). Measurements were performed by setting the gate biases for several seconds, then (a) slowly scanning the anode voltage to reveal the hysteresis or (b) forcing the anode current to reach the S-shaped curve. $L_G = L_{int} = 200$ nm.

2.2. Operation in DC mode

Fig. 2a shows typical hysteresis in I_A-V_A characteristics measured by scanning the anode bias (with a voltage source). The hysteresis originates from an S-shaped I-V characteristic that can actually be measured by imposing the anode current with a current source (Fig. 2b). For low anode voltage, the barriers created by the gates maintain the device in OFF state ('0'). When the turn-on voltage V_{ON} is reached, the feedback mechanism makes the injection barriers to collapse and the current reaches the normal value of a PIN diode (‘1’ state). The switching mechanism is strongly dependent on the modification of the minority carrier concentrations (electrons in the ungated P-region and holes in the gated N-region). The quasi-Fermi levels evolve significantly during the memory cycle. In the hysteresis window, for the same value of V_A, two different currents are observed which can be used as state ‘1’ and state ‘0’ for a static memory (1T-SRAM). We will see that the 1T-DRAM is more complex being governed by non-equilibrium conditions which shift the memory window, V_{ON} and reading voltage to higher V_A.

The band-modulation effect results in sharp transition from low to high current, with an I_{ON}/I_{OFF} ratio of 8 decades (Fig. 2). The turn-on voltage and the hysteresis window are enlarged by increasing the barrier heights via $V_{FG,BG}$. For reverse V_{GF} scan, the device remains in ON state until it reaches a point (~ 0.7 V) at which it turns OFF. The two equilibrium states, ‘0’ and ‘1’, are shown in Fig. 2a. As the hysteresis is achieved with V_A and V_{GF} of about 1 V, the Z^2-FET is attractive for low-power embedded memory applications.

The schematic description above, using the feedback between energy barriers and carrier injection, does not capture the full complexity of the operation mechanisms in Z^2-FET. A detailed physics-based model has been derived by Taur [28]. The leading idea is the continuity of the total current for each of the three P-N junctions: at anode, at cathode and in the center of the body. The model includes the generation-recombination (GR) and diffusion currents for electrons and holes and accounts for the rapid variation of the quasi-Fermi levels with bias. MOS equations define the concentrations of electrons N^* and holes P^* ('electrostatic' doping) in the gated and ungated regions, respectively. 5 equations are sufficient to reproduce the hysteresis and S-shape of DC characteristics. Each step of this continuous model was backed by exhaustive numerical simulations.

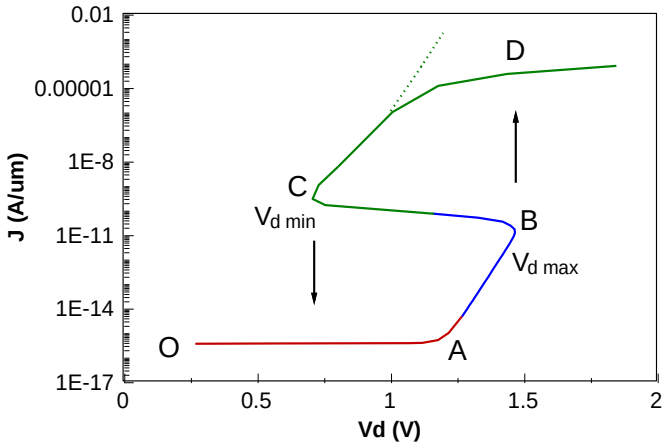

Fig. 3. Computed I_A-V_A curve with Taur's model [28], showing the transitions between different modes of operation.

Fig. 3 shows simulated curves that convincingly match the experiment of Fig. 2b. Several distinct regions of operation are underlined:

From O to A: The device is in OFF state. The voltage drop on the side junctions being negligible, any increase in V_A results in stronger reverse-biasing of the center junction. The corresponding GR current defines the device leakage and is very low. Since the effective gate bias ($V_{FG} - V_A$) decreases, the concentration of electrons N^* tends to vanish.

From A to B: Once the reverse bias on the central junction reaches a maximum, the anode junction starts being forward biased. Injected holes flow towards the cathode and recombine with electrons released by the cathode. The hole diffusion current dominates which explains the slope of 60 mV/decade. As more holes collect in the gated section and more electrons in the ungated section, the central junction becomes less reverse-biased.

From B to C (snapback region): When the central junction is turned on (point B), the anode voltage shared by 3 forward-biased junctions is unnecessarily large. This implies that the current increases even if V_A is reduced, leading to a negative-resistance region.

From C to D: The energy barriers are collapsed and the device behaves as a PIN diode with large forward current. At very high injection level, the series resistance limits the effective voltage on the diode.

Based on the same physical principles and simulations set, a compact model has been formulated by Martinie et al [35]. The various regions of Fig. 3 are modeled independently and linked by interpolation functions. Implemented in Verilog A, the model is used to further optimize the device performance and size.

It is finally noted that Z^2-FET is free of super-coupling and operates successfully even in sub-10 nm thick films. The super-coupling has been experimentally confirmed using a 4-gate transistor (G^4-FET) [36]. This device features a pair of N+ contact and, in the perpendicular direction, a pair of P^+ contacts that enable monitoring the electron and hole currents. Both currents can co-exist in relatively thick body. But, in ultrathin FDSOI, the hole channel, activated by one gate, disappears as soon as an electron channel is induced by the opposite gate, and vice-versa [27]. In Z^2-FET, the populations of electrons are separated *laterally* (in the gated and ungated regions respectively), not *vertically* as in other 1T-DRAMs.

2.3. Transient operation

In transient or pulsed modes of operation, where the electron/hole concentrations do not reach the steady-state, the I_A–V_A characteristics are modified. For example, when the gate is pulsed from 0 V to a positive voltage, electrons are expected to fill the gated region. But, there is no source of electrons other than the generation process or junction and gate leakage. Since electrons cannot be supplied promptly enough, the body potential is in non-equilibrium condition, similar to the well-known deep depletion in MOS capacitors [37,38]. As a result, the energy barrier opposing the injection of holes from anode is temporarily higher than in DC mode and the turn-on voltage V_{ON} is increased. The shorter the pulse, the higher the V_{ON}.

A similar mechanism raises the electron injection barrier at the cathode after switching on the back gate. Finally, applying a positive V_A pulse should reduce the electron concentration under the gate. Again, this modification takes a relatively long time needed for electrons to recombine.

It is clear that carrier generation dominates the off region whereas recombination affects the turn-on and high-current regions. The carrier lifetime is of uppermost importance for the sharp-switching capability and also for memory performance. A detailed analysis is proposed by Parihar et al [39].

2.3. Memory operation

Figure 4 shows the bias pattern used for Z^2-FET memory operation and the corresponding anode current.

- ***Write '0' (W0)***: Electrons are evacuated from the gated region by dropping the gate voltage to 0V.

- ***Hold '0' (H0)***: When V_{GF} returns to 1.2 V, there are no electrons available to compose the inversion layer and the device experiences a non-equilibrium state (deep-depletion) [40]. The sudden change in potential makes the hole injection barrier very steep.

- ***Read '0' (R0)***: Memory reading is achieved with a pulse on the anode. V_A is selected to be in-between the V_{ON} values measured in DC and transient modes. Therefore, the diode is not switched on and the current I_0 is negligible. State '0' requires refresh as parasitic electron-hole generation tends to repopulate the gate region and lower the energy barrier and V_{ON}.

- ***Write '1' (W1)***: The gate voltage is set to 0V to eliminate the barrier. A V_A pulse enables the forward-biased PIN diode to inject electrons and holes into the body.

- ***Hold '1' (H1)***: As soon as V_{GF} returns to 1.2 V, there are sufficient electrons to store under the gate. The diode is at equilibrium, the barriers are lower than for *Hold '0'*, and V_{ON} decreases.

- ***Read '1' (R1)***: The pulse on the anode is now able to turn on the diode, hence the current I_1 is high. Not only are the barriers lower for $V_A > V_{ON}$ but also the discharge current of stored electrons contributes to the sharp switch. Remark that state '1' is self-refreshing and permanent: the electrons forming the anode current are recollected under the gate when the memory returns in *Hold '1'* mode.

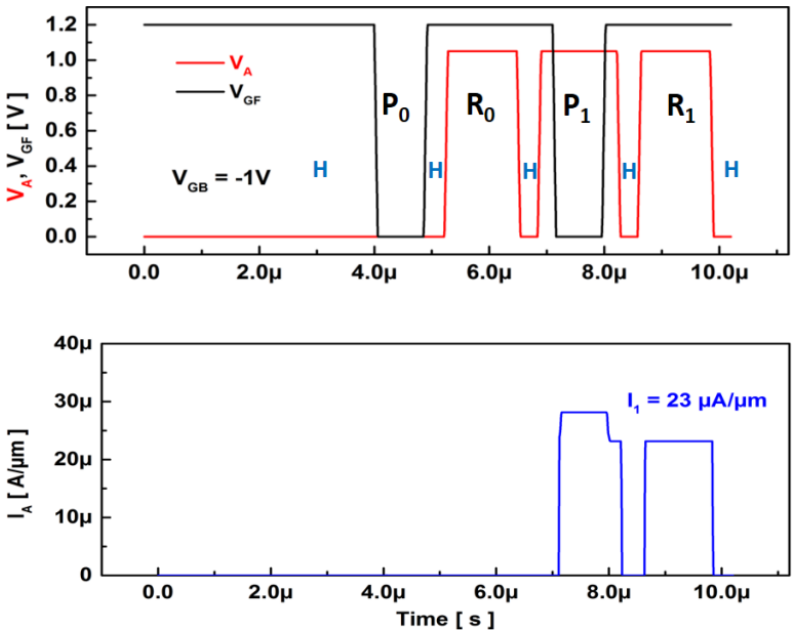

Fig. 4. Bias sequence used for Z^2-FET memory operation and corresponding anode current. V_{GF} = 1.2 V, V_A = 1.05 V, and V_{GB} = -1 V; $L_G = L_{int}$ = 200 nm.

2.4. Memory performance

Programming – Writing state '0' does not depend on voltage (as $V_A = V_{FG}$ = 0 V) and has no impact on power dissipation. A crucial aspect for power reduction is the possibility to reduce

the anode voltage needed to program '1' state below 0.5 V. Even in low-injection condition, the PIN diode is still able to supply enough electrons at the gate for programming logic '1'. For V_A = 0.5 V (Fig. 5), the write current and corresponding power consumption are negligible, massively reduced compared with the nominal case of V_A = 1.05 V (Fig. 4). Another relevant feature is that the read current is rather insensitive to the programming voltage and remains high even for 0.5 V (Figs. 4 and 5). Such a low-voltage capability is unrivalled by any other emerging memory such as resistive, phase change or spin.

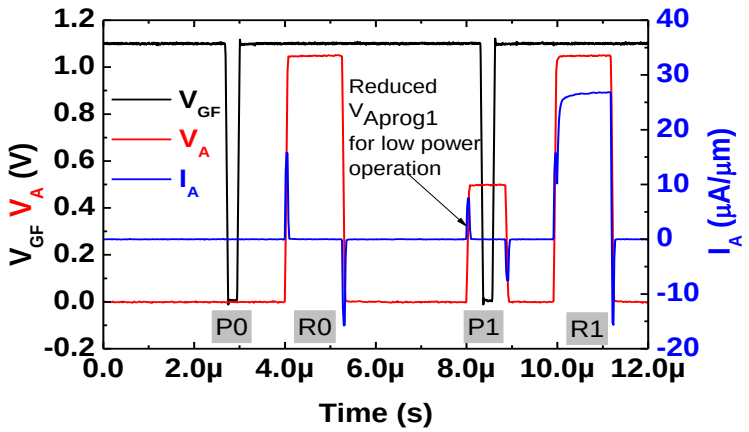

Fig. 5. Bias pattern for Write '1' with very low anode voltage (V_A = 0.5 V). The current spikes are artefacts due to the limitations of the experimental set-up. Other parameters as in Fig. 4.

Reading –The selection of V_A is critical for proper memory operation. If V_A is higher than the transient V_{ON}, the device always turns on, erasing the difference between states '0' and '1'. Similarly, there is no memory effect when V_A is far smaller than the DC V_{ON} because the device is unable to turn on. The correct choice of V_A is between V_{ON} values in DC and transient modes, when the device turns on for state '1' and remains blocked for state '0'. Figure 6 shows that in '1' state the current I_1 depends essentially on anode reading voltage. The diode is in double injection mode, where ultimately $I_1 \sim V^2$. The selection of V_A implies a trade-off between high current margin and low operating voltage. By comparison, the gate bias has a minor effect on I_1 current, as illustrated in Figs. 6. It is in the 'Hold' phase that the choice of V_{GF} bias becomes important because it sets the barrier height in the gated region which controls the hole injection from anode. Figure 7 shows that a too low V_{GF} voltage compromises state '0'. Logic '0' current is ideally negligible (I_0 < nA/μm) unless the injection barriers are not high enough. The remedy is to reinforce the anode barrier by increasing the gate voltage ($V_{FG} \geq$ 1.3 V in Fig. 7b). Reasonable current margins ($I_1 - I_0$ > 20 μA/μm) are obtained for ~1V operation.

Power – During the memory cycle, there are several phases (W0, R0, H0 and H1), where the device is blocked and basically does not dissipate power. Power consumption occurs only when the cell is turned on for programming and reading state '1'. If the same anode bias (~ 1 V) is used for W1 and R1, the drain currents are similar (Fig. 4), leading to equivalent power dissipation in these two phases. However, the program voltage can be reduced to 0.5 V (Fig. 5)

which renders insignificant the W1 current and power. As a result, the total power dissipation of the memory cell is reduced by a factor of two.

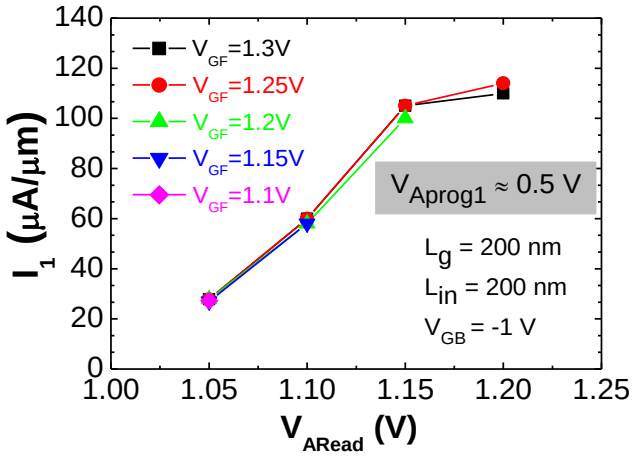

Fig. 6. Logic '1' current versus read anode voltage for different V_{GF} values.

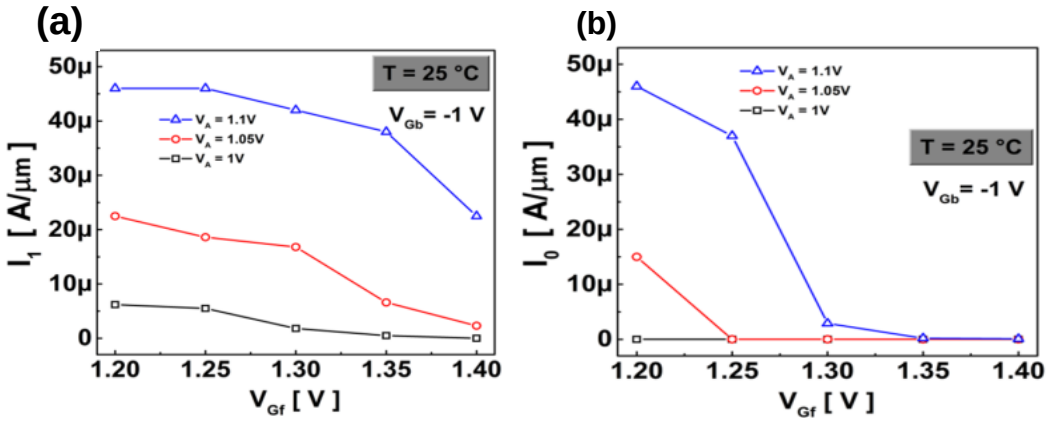

Fig. 7. Logic '1' (a) and '0' (b) read currents versus front-gate voltage V_{GF} for variable anode voltage V_A.

Retention – State '1' is stable and does not require refresh. The read current I_1, composed of electrons and holes, is high. Some of the available electrons are blocked under the gate when the device returns to Hold '1'. The memory retention is defined by the time needed for electrons to repopulate the gate region during '0' state. Carrier generation corrupts logic '0' in logic '1'. Frequent or continuous reading of logic '0' highly improves the retention time simply because the parasitic electrons, that tend to accumulate under the gate, are swept away by the read pulse; the barrier height is restored after each read '0'. Retention time beyond 500 ms has been measured at room temperature and even at 85°C [41]. Voltage tuning is essential for long retention. Also the simple bias sequence shown in Fig. 4a can be revisited by using higher V_{GF} during hold (i.e., stronger barrier) and/or negative V_{GF} for write '0' (i.e., enhanced non-equilibrium condition).

Speed – The Z^2-FET memory is suitable for high-speed 1T-DRAM because the overall performance is improved for fast access time. Sharp switching V_{GF} pulse during programing makes the hole injection barrier higher. For reading, fast rising V_A pulse increases the current and enables lowering the operation voltage. An extreme case is illustrated in Fig. 8: V_A is slightly smaller than the DC V_{ON}, hence a relatively long pulse for read '1' cannot unblock the device. However, for very fast pulse, the device turns on, being triggered by the gate discharge current $\Delta Q_G/\Delta t$. Shorter pulse duration also reduces the time the device is in ON state and dissipates power. Our measurements with 320 ns pulse (equipment limitation) show energy saving by 2 orders of magnitude compared with 120 µs pulse, without any degradation in memory performance. Simulations anticipate successful operation at 1ns access time. The memory keeps working even at 0.1 ns at the expense of degraded current margin (higher I_0 current).

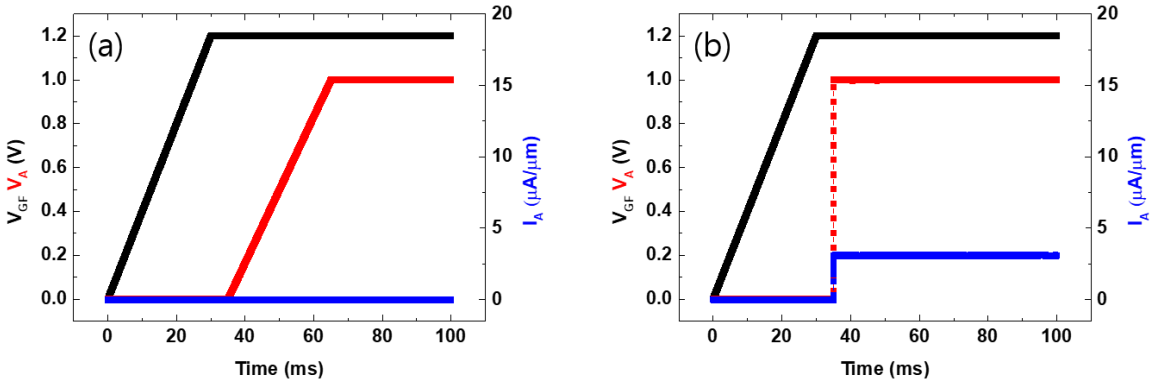

Fig. 8. Influence of anode pulse duration on read logic '1' current. (a) For long V_A pulse, the current I_1 is modest. (b) A short pulse increases I_1 by an order of magnitude.

High temperature operation – The memory is fully functional at 85°C and 125°C. At high temperature, not only are the barriers are weaker but also the carriers gain energy. The current I_1 measured at 85 is 50% higher than at room temperature, which implies that the memory can be operated with lower anode voltage. Since the off current I_0 also tends to increase at high temperature, the solution for maintaining a respectable sensing margin is to adjust V_{GF} to a slightly higher value [34].

The following is a brief summary of the roles played by the main parameters of the memory.

- Anode voltage determines I_1 current.
- V_{GF} defines the hole injection barrier and I_0.
- V_{GB} controls the electron injection barrier. A lower V_{GB} reinforces the front-gate action. The doping of the ground-plane can be adjusted such as to operate the memory with $V_{GB} = 0$ and facilitate peripheral circuitry [42].
- Gate oxide and BOX should be as thin as possible in order to reduce the gate bias.

- Length defines the barrier width and blocking capability; scaling leads to weaker barriers (narrower and shorter) but is possible at least down to 30 nm [9,43].
- Shorter lifetime increases V_{ON} but negatively affects the retention. Conversely, for long lifetime, the Z^2-FET operates as a diode without sharp switch. In practice, the carrier lifetime is technology-related and cannot be easily engineered in ultrathin FDSOI films. It follows that semiconductors with high lifetime may not be suitable.
- Higher carrier mobility increases ON current and carrier diffusion length.
- Short pulses with fast ramping time are beneficial.

3. Insights from memory simulation

With the help of numerical simulations, we can follow the evolution of the injection barriers and carrier populations during the critical steps of the memory cycling. The simulations have been performed with a given set of parameters (length, thickness, carrier lifetime and mobility). Modification of these parameters does not change the qualitative behavior of the Z^2-FET. The numbers in Fig. 9 indicate the biasing points that are further elaborated in Figs. 10-21. Each figure shows the barrier heights (left panel), the electron concentration (center) and the hole concentration (right).

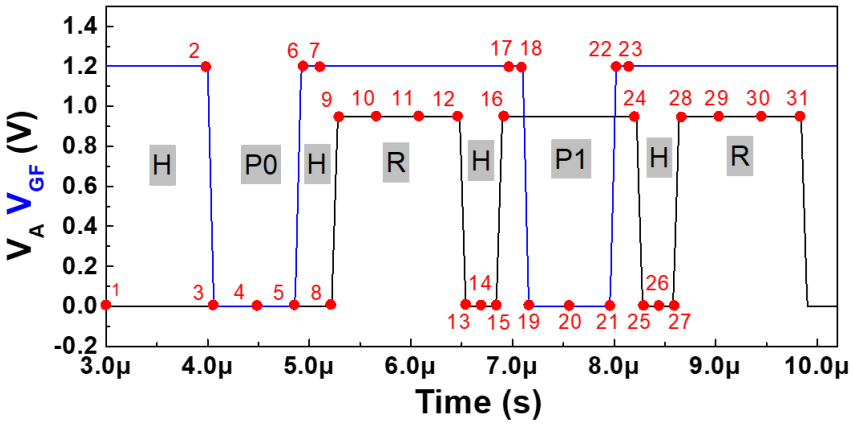

Fig. 9. Chronogram of memory operation indicating the steps elucidated in the following figures. V_{GF} = 1.2 V, V_A = 1.05 V, and V_{GB} = -1 V; L_G = L_{int} = 200 nm.

Pre-programming (Fig. 10) – The two barriers are high and the central junction absorbs ~1 V. The wells are filled with electrons (gated region) and with holes (ungated region). In general, the hole injection barrier is controlled by the difference between anode and gate voltage whereas the electron injection barrier is rather constant.

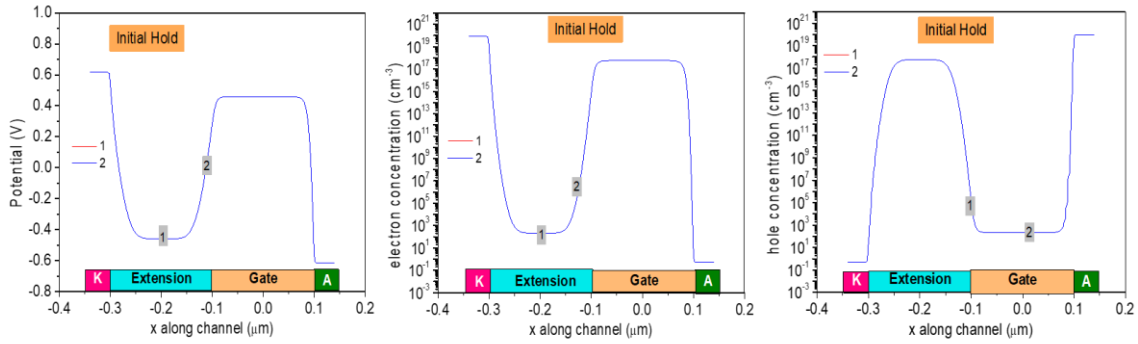

Fig. 10. Quasi-DC initial state. Potential barriers and electron/hole concentrations along the device.

Pre-Write '0' (Fig. 11) – As V_{GF} decreases, the hole injection barrier is strongly reduced which also lowers the voltage drop in the central junction to 150-200 mV. The reason is the clear increase in minority carrier concentrations: electrons near cathode and holes near anode. The electron concentration at 1 nm under the gate decreases by 10-20 %. For fast fall time (1 ns, not shown) of V_{GF} signal, the electrons are actually displaced from the top surface to the bottom interface (film-BOX). A longer fall signal (60 ns) enables most electrons to be evacuated from the back surface.

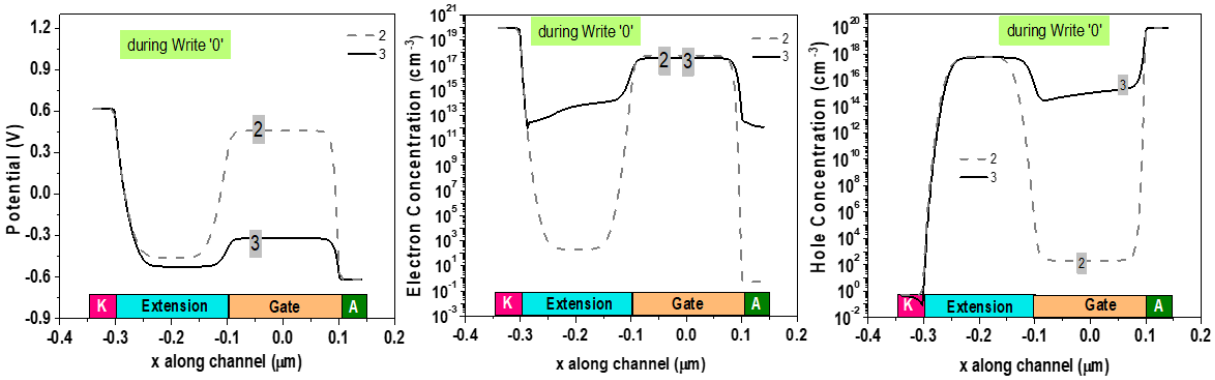

Fig. 11. Evolution during the gate voltage drop before writing '0'.

Write '0' (Fig. 12) – The gate voltage being maintained at 0 V, the electron concentration under the gate decreases by more than 10 orders of magnitude, which is actually the purpose of Write '0'. The hole concentration decreases slightly in the gated region which explains the little higher injection barrier.

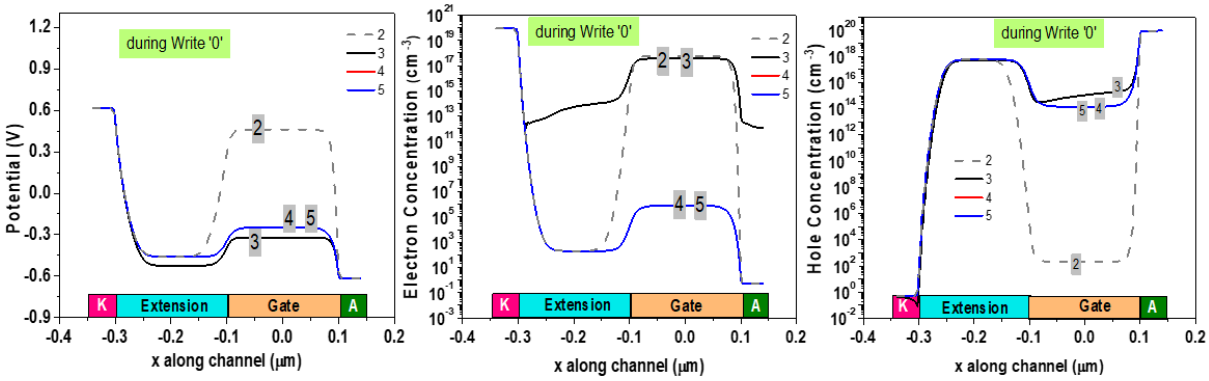

Fig. 12. Write ‘0’ stage.

Hold ‘W0’ (Fig. 13) – Once the gate returns to a high voltage, the electron concentration tends to increase but is still insignificant (10^{12} cm^{-3}) and triggers non-equilibrium condition. The hole injection barrier is higher (1.6 V) than in DC state (~1 V in Fig. 10). The holes are evacuated from the gated region.

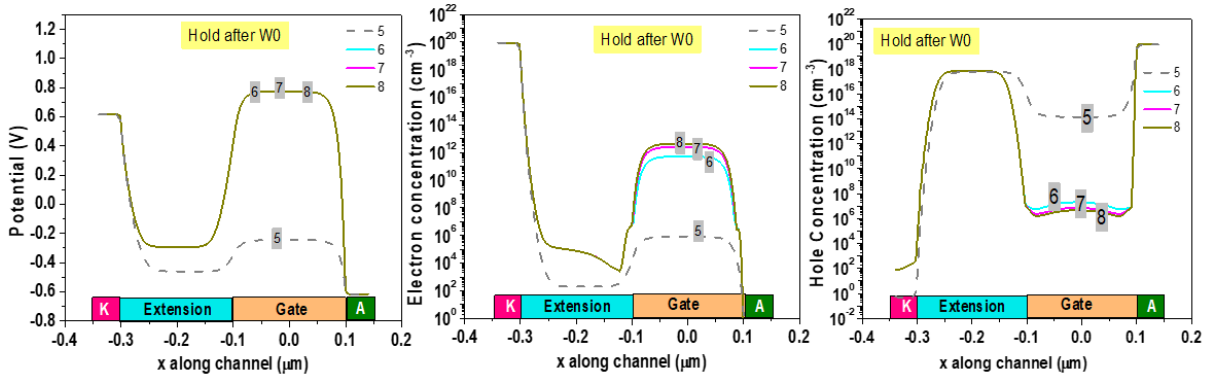

Fig. 13. Evolution during Hold ‘0’.

Pre-Read ‘0’ (Fig. 14) – The V_D pulse lowers the hole injection barrier without being able to collapse it.

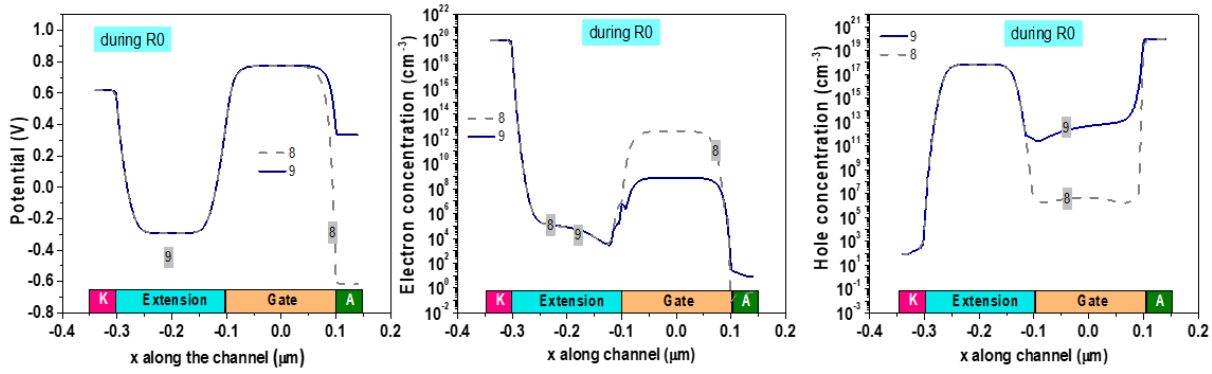

Fig. 14. Evolution during the rise of anode voltage in preparation of reading ‘0’.

Read '0' (Fig. 15) – During the period when V_D is high, the electron injection barrier at cathode decreases by 0.4 V which reduces the voltage drop on the central junction. Although the electron concentration under the gate tends to increase, the hole injection barrier remains constant. Despite marginal changes in carrier concentrations, the device remains blocked with negligible I_0 current.

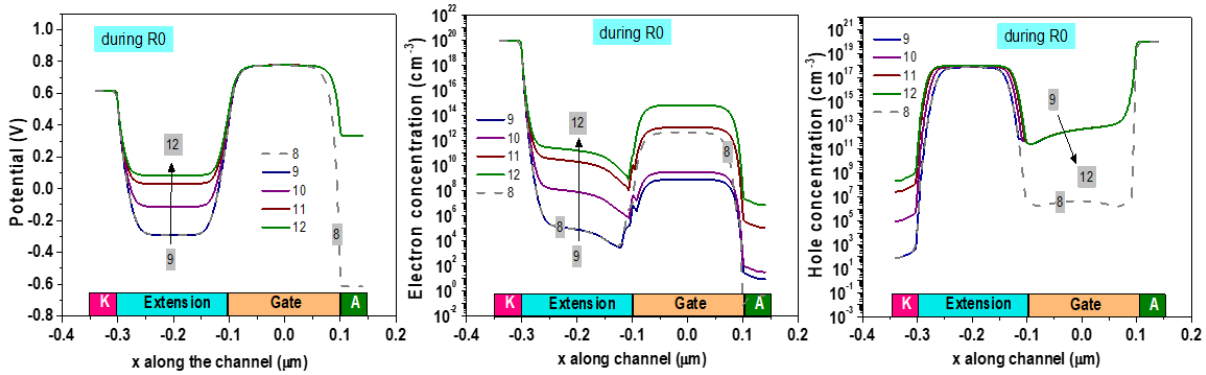

Fig. 15. Read '0' state.

Hold 'R0' (Fig. 16) – The main effect of suppressing the anode voltage is to restore a high barrier against hole injection. The electron concentration under the gate continues to attempt increasing.

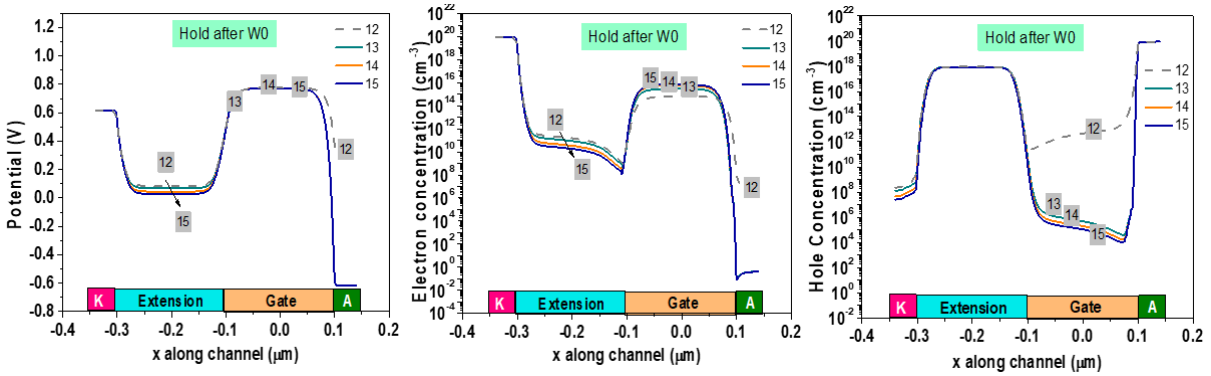

Fig. 16. Hold stage after reading '0'.

Pre-Write '1' (Fig. 17) – As V_A increases again, the hole barrier is immediately reduced. In the gated region, the electron concentration decreases because the gate bias is less effective ($V_{FG} - V_A$), and more holes arrive.

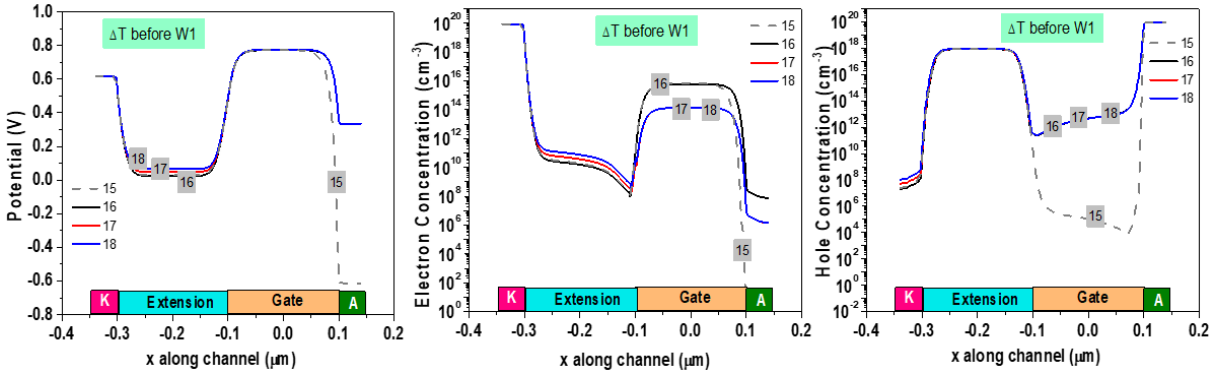

Fig. 17. Evolution during V_A rise in preparation of writing '1' state.

Write '1' (Fig. 18) – As soon as V_{GF} is brought to 0 V, both barriers collapse and the central junction becomes forward biased. The PIN diode is ON and the concentrations of electrons and holes are high and comparable everywhere in the body.

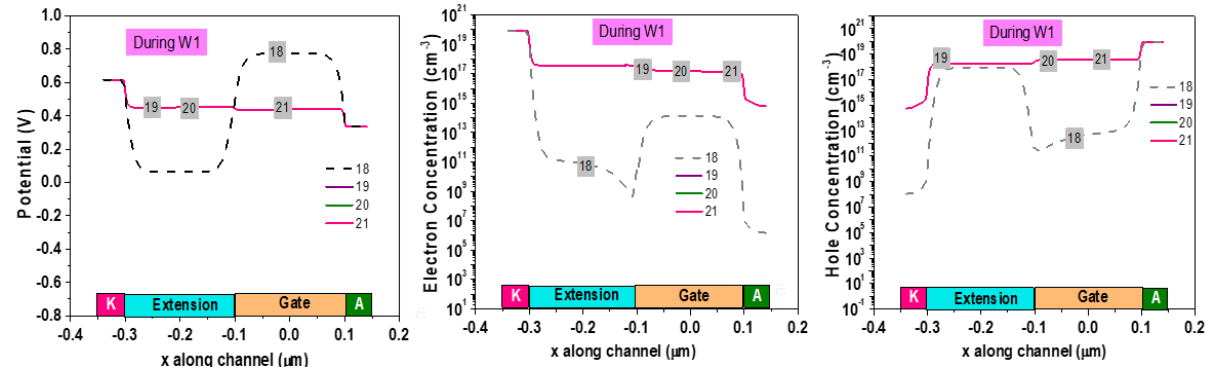

Fig. 18. Write '1' with the diode turned ON.

Post-Write '1' (Fig. 19) – Even if V_{GF} returns to high level (1.2 V), the diode is still in ON state.

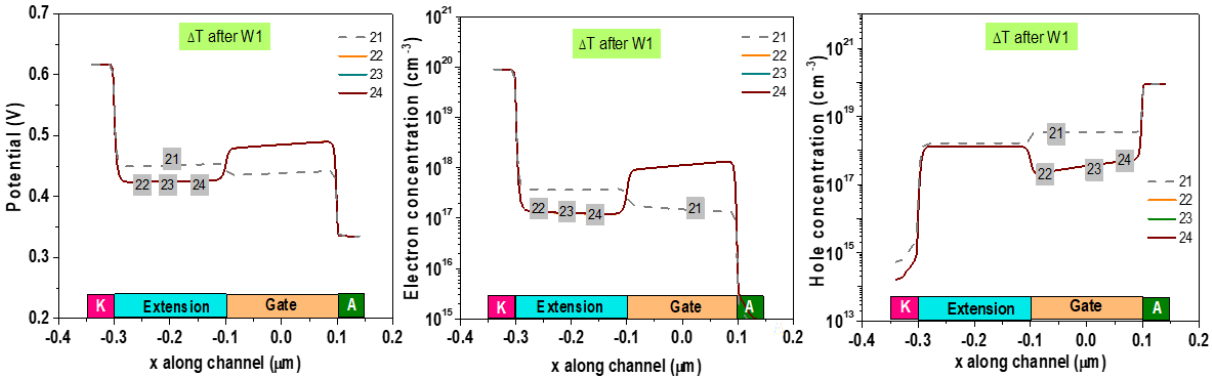

Fig. 19. Change in diode behavior when gate bias is switched from 0 V to high voltage, in preparation of Hold ‘1’.

Hold ‘W1’ (Fig. 20) – Only after V_A is pulsed to 0 V are the barriers reconstructed. The electron concentration is far higher than in Hold ‘0’ situation (Fig. 13) which enables discriminating ‘1’ and ‘0’ states.

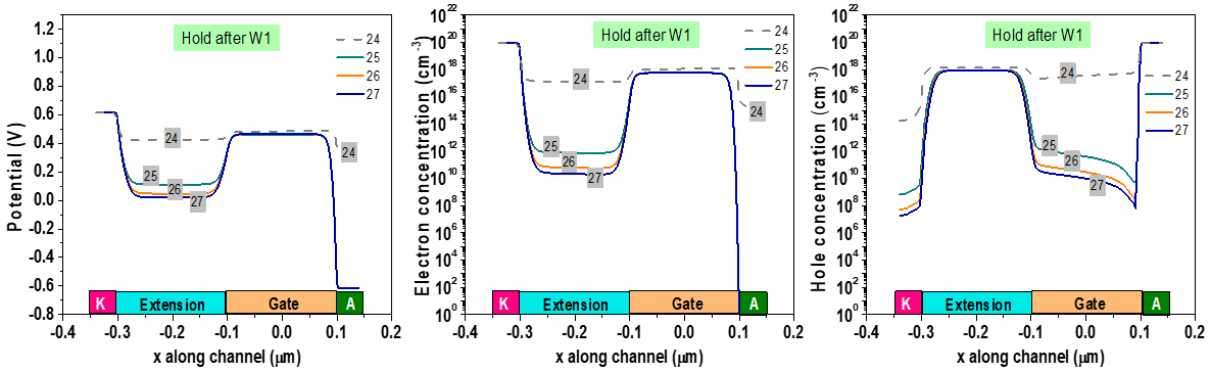

Fig. 20. Hold ‘1’ where the diode returns to OFF mode.

Read ‘1’ (Fig. 21) – The V_A pulse is now able to collapse both barriers bringing the diode in ON state with high current and electron/hole concentrations.

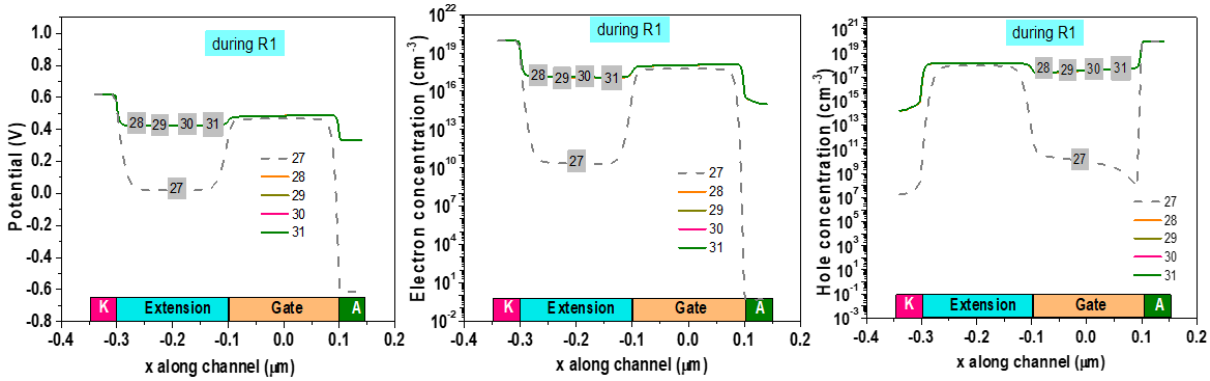

Fig. 21. Read ‘1’ turns the diode on.

Conclusion

The rationale for developing Z^2-FET 1T-DRAMs has been documented by referring to the limitations of other types of floating-body memories. The Z^2-FET sharp switch and its application as 1T-DRAM have been described by revealing the detailed mechanisms that occur

in DC, transient and memory operation. Additional information is available in a series of papers dedicated to Z^2-FET [41-45]. The experiments and simulations have been focused on the device fabricated with 28nm FDSOI technology (Fig. 1). Other implementations are under investigation: thinner body, gate oxide and BOX as considered for 14 nm FDSOI node, dual ground planes that control respectively the gated and ungated sections of the body [44], intentional N-type doping in the ungated region to suppress the need for back bias [42], and gateless Z^3-FET where the barriers are set by independent ground planes [32].

The Z^2-FET memory is unrivalled in terms of retention time, low-power consumption, memory margin and non-destructive reading. Another practical advantage is the full compatibility with the FDSOI process, without any additional technology module needed. We have experimentally demonstrated low-voltage operation with ~1 V read bias and program bias as low as 0.4–0.5 V. These assets make the Z^2-FET very attractive as high-speed, low-power embedded memory.

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