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Simulation Study of Junctionless Silicon Nanoribbon FET for High-Performance Printable Electronics

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***Abstract*— High-performance electronics on flexible substrates along with low-cost fabrication by printing has gained interest recently. For this purpose, the printing of inorganic semiconductors based micro/nanostructures such as nanowires etc. are being explored. However, due to thermal budget, the controlled selective source/drain doping needed to obtain transistors from such structure remains a bottleneck post transfer printing. This paper presents an attractive solution to address this challenge. The solution is based on junctionless FETs (JLFET), which do not require selective doping. Unlike conventional JLFETs, which use nanowires, the devices presented here are based on nanoribbons as this enable larger channel width and hence high drive current. Studied through simulation, the JLFETs presented here show high-performance with current high enough to drive micro-LED. The TCAD simulation has been carried out to study the effect of single and dual metal gate (top and bottom side) of JLFETs as well as that of doping and nanoribbon thickness on the electrical characteristics. The simulation results indicate that the proposed devices will be suitable for high performance printable electronics applications.**

Keywords— Junctionless FET; TCAD simulation; Dual Gate Transistor; Flexible Electronics, Printable Electronics

I. INTRODUCTION

The large area flexible electronics has become an area of intense research as it enables a range of new applications which are not possible with conventional electronics [1]. Traditionally, organic semiconductors and amorphous silicon have been explored for large area electronics as they can be printed or coated over large areas. However, the slow response of the devices from these materials, owing to their low charge carrier mobility, renders them suitable only for low-end applications such as displays and photovoltaics where fast transistor switching is not a strict requirement [2]. With the fast communication and computation needed in the emerging applications such as wearable systems and internet of things etc., the high-performance (i.e. faster response, robust, uniformity of response, low-power etc.) of flexible electronics is gaining prominence [3]. The high-performance flexible electronic and photonic devices are also needed in applications such as opto-genetics, next-generation flexible portable displays, health sensors, oximeters, electronic skin etc. [1, 4]. A range of alternative solutions are being explored for high-performance flexible electronics. For example, the two-dimensional (2D) materials such as graphene, which have very high mobility, are being explored as channel materials for FET [5]. However, the zero bandgap and difficulties with synthesis and transfer of graphene over large flexible areas pose a huge challenge [5]. Although there is some progress in this direction, the technology is still not at a stage where one can think of large scale integration. In this regard, micro/nanostructures such as thin membranes, ribbons, nanowires etc. from single crystal silicon and compound semiconductors can offer better solutions as they exhibit high charge-carrier mobility and the technology for devices based on these materials is mature [6, 7]. Further, recent advances such as printing of silicon and compound semiconductor micro/nanostructures on flexible substrates make them attractive alternative for high-performance flexible electronics [8-11]. However, due to thermal budget related issues it is difficult to attain controlled doping of micro/nanostructures after they have been printed on flexible substrates. Controlled doping at defined locations is critical to obtain transistors. Some attempts have been made to overcome this issue through alternative means such as using Si/Ge heterostructures [12, 13]. However, with this approach it is not possible to develop CMOS circuitry as they lead to only p-MOS devices. This highlights the need to further explore the alternative solution. The junctionless FETs (JLFET) or gated resistors reported recently could be one route as in this case entire micro/nanostructures should be doped, which could be achieved before these structures are transferred or printed on to flexible substrates [14]. Further, this solves the traditional issue related to precise registration/printing of source drain contacts at defined location. This paper explores this interesting direction with simulation studies of nanoribbon based junctionless FETs.

This paper is organized as follows. The structure of the nanoribbon based JLFET is presented in the section II. This section also explains the difference of device presented here with respect to the conventional nanowire based JLFETs. This is followed by discussion related to simulation results in Section III. The Technology Computer Aided Design (TCAD) based simulation is used to optimize the device. The effect of doping, thickness, etc. on the performance of the nanoribbon based JLFET are also presented in Section III. Finally, the key results are summarized in the concluding Section IV.

II. STRUCTURE AND WORKING OF PROPOSED JLFET

The two prerequisites for JLFETs are: (1) Thin semiconductor layer to enable full depletion of the channel in its off state; and (2) Highly doped semiconductor to allow for realistic current drive in its ON-state as well as provide ohmic source and drain contacts [14, 15]. In addition, normally off operation is required for JLFETs to be used in conventional CMOS applications. To achieve the normally off condition, a high work function material such as n^+ polysilicon is used as the

gate material for p+ channel (or p^+ polysilicon gate for n+ channel) in the junctionless nanowire FETs [15-17]. The JLFETs we propose in this work meets the above conditions, but instead of using nanowires, we have used nanoribbons as this allows devices with higher ON current. The higher channel width in nanoribbons allows higher current in comparison with nanowires based JLFETs. Devices with higher ON current typically are needed to drive Light Emitting Diodes (LEDs) used for large area displays. They are also needed to drive micro LEDs that are typically used in optogenetic application. The drive current for micro LEDs for such applications is typically ~2-5 mA [18]. Further the nanoribbon based JLFETs presented here have metal gate electrodes instead of polysilicon as this leads to lower gate resistance and prevents gate depletion. Further, the metal gate can be deposited at low temperature, which is critical for flexible electronics applications.

The structure of the device presented here has been designed considering that the transfer printing based processing technology will be used to realize them on flexible substrates such as polyimide [9, 19, 20]. Fig. 1(a) shows the 3D structure of the simulated JLFET on a polyimide. An equivalent 2D structure corresponding to the vertical cross-section (Fig. 1(a)), is shown in Fig. 1(b). The 2D structure was also simulated as the 3D simulation often requires intensive computing and longer time to converge. The horizontal and the vertical axis in Fig. 1b are not of same scale. The device comprises of 50-nm thick Si nanoribbon on the top of polyimide. A doping concentration of $1x10^{18}$ cm^{-3} is considered throughout the nanoribbon without any junction. A metal gate forming a channel length of 20 µm with a work function of 5.15 eV (corresponding to Ni) is used to realize a gate all-around transistor structure. This is also a differentiating factor compared to the conventional nanowires based JLFET where the channel length is in nanoscale [15]. In the case of 2D, the top and bottom gate is considered as a common gate in the simulation. A common mode gate voltage is applied during simulation to mimic the wrapped gate, around the nanoribbon. The metal gate is isolated from the active region of the device by a 30-nm thick Al_2O_3 (κ~ 9.3) dielectric wrapping around the nanoribbon. In the case of 2D, this equivalent to the 30-nm thick Al_2O_3 dielectric between the nanoribbon and commonly connected top and bottom gates. This resembles a double gate structure. A gap of 2.5 µm was considered between source and the gate region. The models used for the simulation studies include concentration dependent mobility, field dependent mobility, Fermi-Dirac statistics, auger recombination, quantum effects [21, 22].

III. Simulations and Results

Simulating and studying the device behavior is needed to cost-effectively analyze various structure and the effects of electrical parameters on device performance before fabrication. The effect of single Vs. double gate (2D equivalent), nanoribbon thickness, doping etc. are presented in this paper. In this paper the simulation were carried out with Silvaco ATLAS 3D and 2D packages [21, 22].

A. 3D Vs 2D Simulation of JLFET

A comparative study was carried out to evaluate the difference between 2D and 3D structures. For 2D simulation, a common gate voltage was applied to both the top and bottom terminal with the drain current from both the simulation normalized to unit channel width. The results of the 2D and 3D structure simulations are shown in Fig. 2. A difference of <2.2% was observed between the transfer characteristics of the 3D and 2D simulation at 1.5 V. Since the difference is not high, the rest of the simulation study presented in this paper is based on the 2D structure. This is also keeping in view that the 3D simulation is computational intensive and requires longer time to converge. For the following discussion, the current at V_{GS} = 1.5V is termed as I_{D+} and at V_{GS} = -1.5V is termed as I_{D-}. Later considering a normally off operation, we have discussed on-to-off ratio.

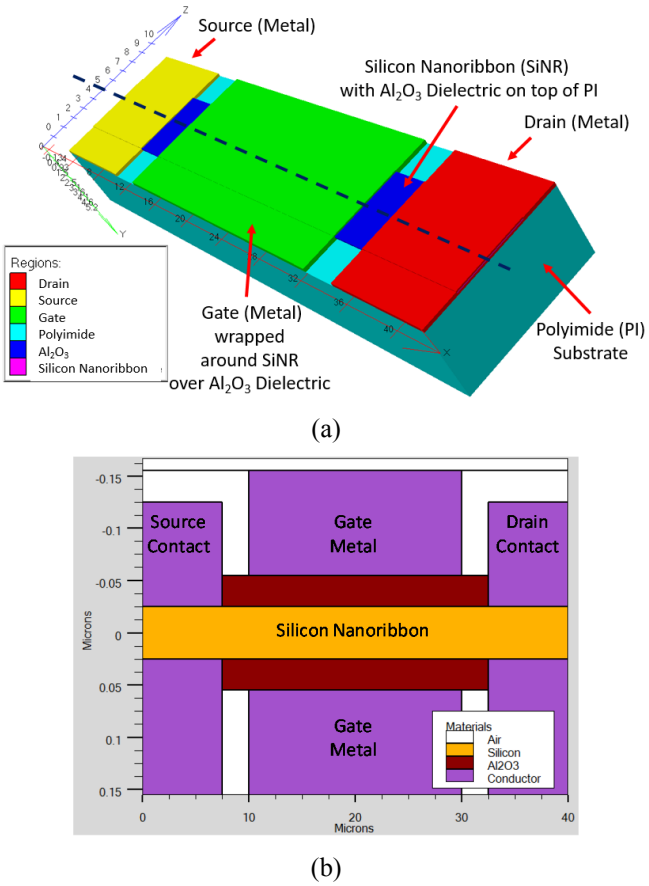


Fig. 1: (a) 3D structure of JLFET and its equivalent (b) 2D structure, a vertical cross sectional representation of JLFET (Horizontal and vertical axis are of different scale in 2D)

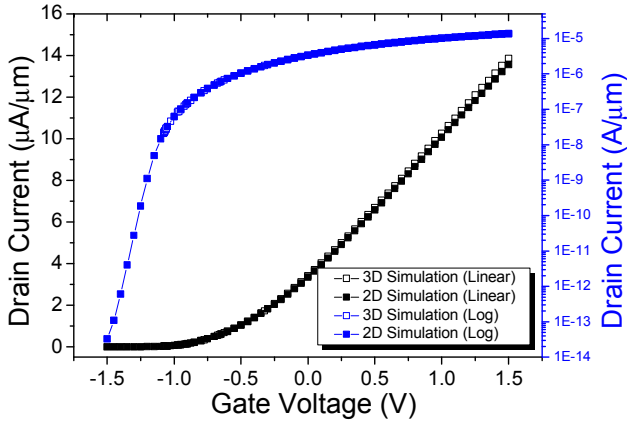


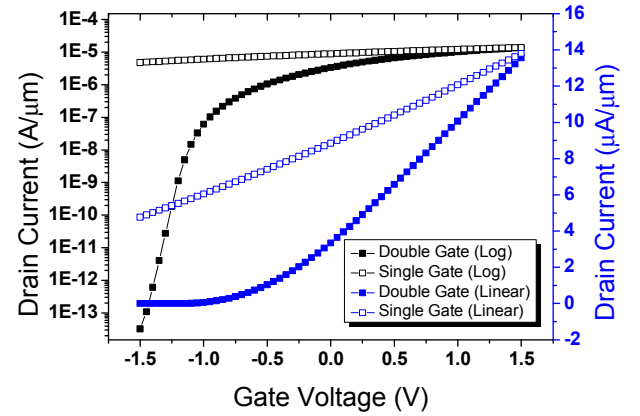
Fig. 2: Comparison between 3D and 2D simulation of V_{GS} Vs I_{DS} Characteristics at V_{DS}=1.5 V

B. *Effect of Single Gate and Double Gate*

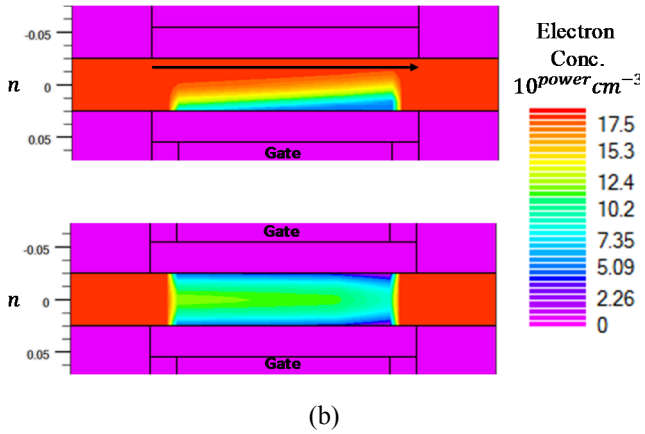
Fig. 3a shows the effect of single gate and common mode double gate on the transfer characteristics of the JLFET. A single gated JLFET results in a resistive structure. This is due to a poor gate control, which is incapable of completely depleting the highly doped nanoribbon channel of JLFET. This is evident from the electron concentration contour plot shown in Fig. 3b at V_{GS}=-1.5V. JLFET with a single gate, the channel is not depleted effectively and a low resistivity leaky path is observed far from the single gate as indicated by the arrow mark. Double gate results in better I-V characteristics with $\frac{I_{D+}}{I_{D-}}$ of 4.2x10^8, which is seven orders of magnitude higher compared to the single gate where it was mere 2.9. This shows that having a double gate is critical and key to achieve a higher on-to-off ratio. For further discussions, I_{D+} and I_{D-} is considered as the drain current at V_{GS} of -5 V and +5V, respectively.

C. *Influence of Quantum Effects on Current Density*

The quantum effects on the current density of the simulation was studied using both the Poisson and Schrodinger-Poisson equation. The transfer characteristics of the JLFET from solution of Poisson equation and Schrodinger-Poisson equation is shown in Fig. 4a. The electron concentration for the two cases at V_{GS}=-1.5V is shown in Fig. 4b. As shown in Fig. 4b. the Poisson equation overestimates the carrier density closer to the oxide-semiconductor interface compared to Schrodinger-Poisson equation, consequently resulting in a maximum difference of ~7.2% in the transfer characteristics of the JLFET.

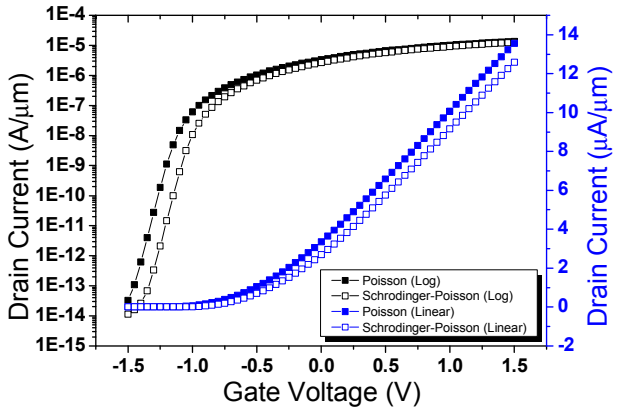


(a)

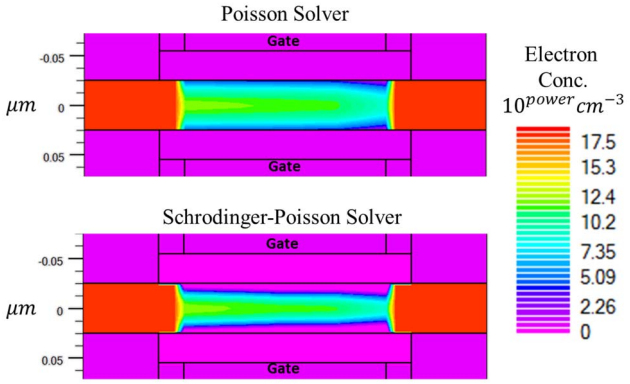


(b)

Fig. 3: Effect of Single Gate Vs Double Gate on the (a) Transfer characteristics (b) Channel electron concentration at V_{GS}=-1.5V.



(a)



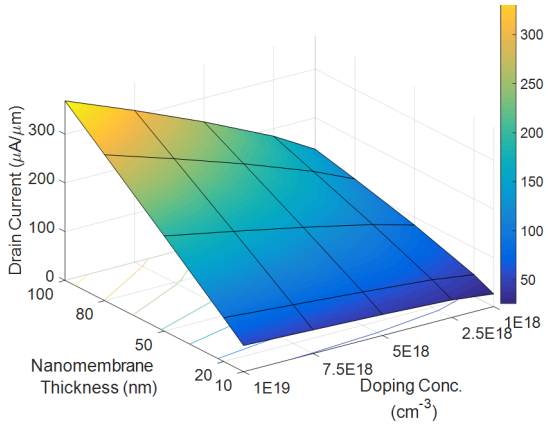
(b)

Fig. 4: Effect of quantum effects on the (a) Transfer characteristics (b) Channel electron concentration from solution to Poisson equation and Schrodinger-Poisson equation at V_{GS}=-1.5V.

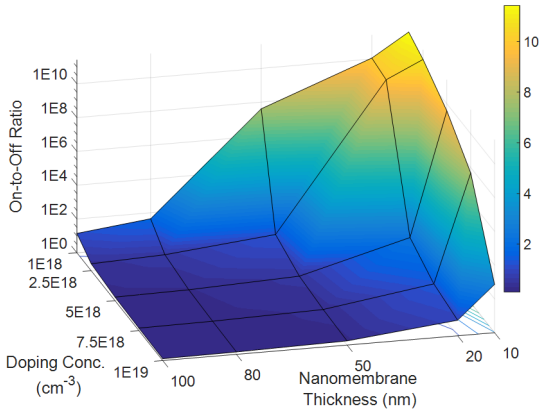
Therefore, Schrodinger-Poisson solver was used for further simulation.

D. *Effect of Thickness of the Nanoribbon and Doping*

The thickness of the nanoribbon was varied between 10 to 100 nm and the doping concentration was varied between 10^{18} to 10^{19} cm^{-3}. Fig. 5(a) shows the effect of the thickness of the nanoribbon and the doping on the I_{ON} current. Thicker the nanoribbon and higher the doping more the I_{ON} current. However, as shown in Fig. 5(b), the on-to-off ratio decreases with thicker nanoribbon and higher doping. This is because of increase in the off-state leakage current as the gate is not able to completely deplete the channel. For optimal performance, thinner the nanoribbon thickness is higher the possible value for doping concentration to achieve higher on current with sufficient on-to-off ratio. For nanoribbons of thicknesses 10, 20 and 50 nm, the doping should be less or equal to 7.5x10^{18}, 4x10^{18} and 2x10^{18}, respectively to achieve higher current with on-to-off ratio >10^6. However, the doping cannot be lowered further than 10^{18} cm^{-3} as it should be in the degenerate regime to get ohmic contact in the source and drain region. With a nanoribbon thickness of 50 nm, a doping concentration of 10^{18} cm^{-3}, an Al_2O_3 thickness of 15 nm and Pt as gate material results in a current of 84 μA/μm. This leads to a current of 3.36 mA for a 40 μm channel width which is suitable for driving μLED as given in section II.



(a)



(b)

Fig. 5: Effect of thickness of the Nanoribbon and Doping on the (a) ON current and (b) On-to-off ratio.

IV. Conclusion

In summary, the simulation study of nanoribbon based JLFET devices presented in this paper shows that they have the high-performance and hold promise for solving the doping related challenges in flexible and printable electronics. The device structure presented here can drive micro LEDs which typically require high drive current. Based on the simulation based optimization, a current of 3.36 mA for a 40 µm channel width is achievable with an on-to-off ratio of 4.02x 10^7. JLFET based approach. The study related to presence of gate on either side of the nanoribbon indicates that the dual gate configuration is essential to achieve the high-performance transistors for a 50-nm nanoribbon. The studies related to the effect of doping and nanoribbon thickness on device performance indicate that, for nanoribbons of thicknesses 10, 20 and 50 nm, the doping should be less or equal to 7.5x10^{18}, 4x10^{18} and 2x10^{18}, respectively to achieve higher current with on-to-off ratio >10^6. The use of metal gate provides a promising alternative to polysilicon gate for flexible electronics application.

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References

[1] A. Nathan, A. Ahnood, M. T. Cole, S. Lee, Y. Suzuki, P. Hiralal, F. Bonaccorso, T. Hasan, L. Garcia-Gancedo, and A. Dyadyusha, "Flexible electronics: the next ubiquitous platform," Proceedings of the IEEE, vol. 100, pp. 1486-1517, 2012.

[2] R. A. Street, "Thin‐Film Transistors," Advanced Materials vol. 21, pp. 2007-2022, 2009.

[3] C. G. Núñez, W. T. Navaraj, E. O. Polat, and R. Dahiya, "Energy autonomous flexible and transparent tactile skin," Advanced Functional Materials vol. 1606287, 2017.

[4] R. Dahiya, W. T. Navaraj, S. Khan, and E. Polat, "Developing electronic skin with the sense of touch," Inf. Display, pp. 2-6, 2015.

[5] E. O. Polat, O. Balci, N. Kakenov, H. B. Uzlu, C. Kocabas, and R. Dahiya, "Synthesis of Large Area Graphene for High Performance in Flexible Optoelectronic Devices," Scientific Reports, vol. 5, Nov 18 2015.

[6] D.-H. Kim, N. Lu, R. Ma, Y.-S. Kim, R.-H. Kim, S. Wang, J. Wu, S. M. Won, H. Tao, A. Islam, K. J. Yu, T.-i. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H.-J. Chung, H. Keum, M. McCormick, P. Liu, Y.-W. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, and J. A. Rogers, "Epidermal Electronics," Science, vol. 333, pp. 838-843, 2011.

[7] Y. Sun and J. A. Rogers, "Inorganic Semiconductors for Flexible Electronics," Advanced Materials, vol. 19, pp. 1897-1916, 2007.

[8] S. Khan, L. Lorenzelli, and R. S. Dahiya, "Technologies for Printing Sensors and Electronics over Large Flexible Substrates: A Review," Sensors Journal, IEEE, vol. 15, pp. 3164-3185, 2015.

[9] D. Shakthivel, W. T. Navaraj, C. García Núñez, F. Liu, and R. Dahiya, "Transfer Printing Si Nanowires for Flexible Large Area Electronics," presented at the Innovations in Large Area Electronics (InnoLAE) Conference, Cambridge, UK, 2016.

[10] R. Dahiya, G. Gottardi, and N. Laidani, "PDMS residues-free micro/macrostructures on flexible substrates," Microelectronic Engineering, vol. 136, pp. 57-62, 2015.

[11] R. S. Dahiya, A. Adami, C. Collini, and L. Lorenzelli, "Fabrication of single crystal silicon micro-/nanostructures and transferring them to flexible substrates," Microelectronic Engineering, vol. 98, pp. 502-507, 2012.

[12] J. Xiang, W. Lu, Y. Hu, Y. Wu, H. Yan, and C. M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," Nature, vol. 441, pp. 489-93, May 25 2006.

[13] K. Takei, T. Takahashi, J. C. Ho, H. Ko, A. G. Gillies, P. W. Leu, R. S. Fearing, and A. Javey, "Nanowire active-matrix circuitry for low-voltage macroscale artificial skin," Nat Mater, vol. 9, pp. 821-826, 10//print 2010.

[14] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junctionless multigate field-effect transistor," Applied Physics Letters, vol. 94, p. 053511, 2009.

[15] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," Nat Nano, vol. 5, pp. 225-229, 03//print 2010.

[16] S. J. Choi, D. I. Moon, S. Kim, J. P. Duarte, and Y. K. Choi, "Sensitivity of Threshold Voltage to Nanowire Width Variation in Junctionless Transistors," IEEE Electron Device Letters, vol. 32, pp. 125-127, 2011.

[17] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Performance estimation of junctionless multigate transistors," Solid-State Electronics, vol. 54, pp. 97-103, 2// 2010.

[18] N. McAlinden, D. Massoubre, E. Richardson, E. Gu, S. Sakata, M. D. Dawson, and K. Mathieson, "Thermal and optical characterization of micro-LED probes for in vivo optogenetic neural stimulation," Optics Letters vol. 38, pp. 992-994, 2013/03/15 2013.

[19] R. S. Dahiya and S. Gennaro, "Bendable ultra-thin chips on flexible foils," IEEE Sensors Journal, vol. 13, pp. 4030-4037, 2013.

[20] S. Khan, N. Yogeswaran, W. Taube, L. Lorenzelli, and R. Dahiya, "Flexible FETs using ultrathin Si microwires embedded in solution processed dielectric and metal layers," Journal of Micromechanics and Microengineering, vol. 25, p. 125019, 2015.

[21] N. Shashank, V. Singh, W. Taube, and R. Nahar, "Role of Interface Charges on High-k Based Poly-Si and Metal Gate Nano-Scale MOSFETs," Journal of Nano-and Electronic Physics, vol. 3, p. 937, 2011.

[22] "ATLAS User Manual," 2017.