Bending Effects in a Flexible Dual Gated Graphene FET: a Verilog-A Model Implementation

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***Abstract*— This paper presents the Verilog-A implementation of charge control based model of dual gated graphene field effect transistor (GFET) and initial results towards bending induced changes in their electrical response. The ambipolar region of the device has been described using the saturation and displacement current models. The output characteristics derived from Verilog - A simulation is in good agreement with the reported experimental results. The model has been extended to study the behaviour of a bendable GFET and the simulation indicates negligible change in the electrical properties in the test range of bending.**

Key words— Dual gate, Graphene Field Effect transistor, Verilog-A, Bending effects..

I. INTRODUCTION

Graphene is a semimetal 2DEG (two-dimensional electron gas) whose fascinating intrinsic properties are determined by the network of sp^2 hybridized carbon atoms arranged in a honeycomb lattice [1-3]. The conical dispersion of its carriers' band structure around K and K' equivalent points makes the charge carriers behave like massless relativistic chiral-particles moving at the Fermi velocity, v_F. Consequently, the carrier mobility of the field effect transistors based on graphene (GFETs) is much higher than those based on conventional semiconductors and this makes GFET attractive for future nanoscale devices [4]. However, the absence of band gap in graphene, results in devices with poor on/off current ratio, therefore limits the use of GFETs in the development of logical circuits [5]. Nevertheless, GFET could greatly benefit radio frequency (RF) electronics owing to its high carrier mobility and high saturation current and complete transistor switching-off is not a prerequisite [6]. Other areas where graphene has been used recently are sensors in flexible electronics applications such as e-skin, where graphene's other features such as inherent bendability and optical transparency have been exploited [7-10]. Further the development of flexible GFET would enable the development of high performance flexible electronics for portable and wearable electronic applications where conformability is a necessity. One major issue in the case of graphene based devices in flexible electronics (generally for devices made of any material) is the bending induced changes in the response of devices. For future electronic circuit design, it is important to understand such variations to ensure reliable operation of the device under different bending states. In this paper, we have investigated the behaviour of a GFET device under various bending states. The study is based on the modified model that simulated the kink like behaviour in the saturation current of a dual gate GFET [3]. We have modified the transistor model by using the analytical studies initially presented by Meric *et. al* [11], and subsequently by Scott *et. al* [12] and Umoh *et. al* [13]. The proposed model has been implemented in Verilog-A, which is widely used for circuit modelling [14, 15].

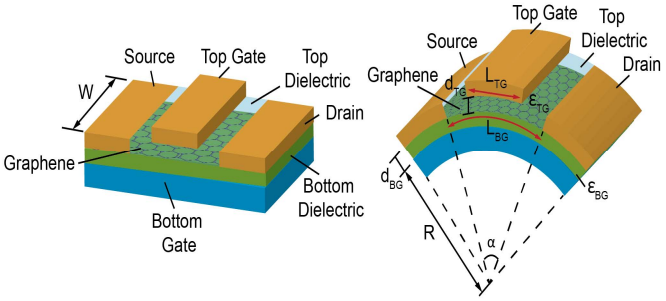

Fig.1. Schematic of the dual gate GFET

This paper is organised as follows: Section II presents the transistor layout of the modelled GFET device. Section III establishes the drain current equation used for model. The results are presented in the Section IV. Finally, Section V presents the conclusion of the paper.

II. GFET LAYOUT

The cross-sectional view of a dual gate transistor is depicted in Fig. 1. The device comprises of a monolayer graphene sandwiched between two dielectric layers. The top gate is isolated from graphene by a dielectric of thickness, d_{TG} and dielectric constant of ε_{TG}. Similarly, the back gate is isolated from the monolayer graphene by a dielectric layer of thickness d_{BG} and dielectric constant of ε_{BG}. The formation of top gate channel is controlled by a top gate bias ($V_{gs(top)}$) applied to the gate of length L_{TG} (1µm) and width W (2.1µm). The back-gate voltage ($V_{gs(back)}$) controls source and drain contact resistances and threshold voltage of the top gate channel. In this study, we considered the thickness of the top and bottom gate dielectric as 15nm and 285nm and their permittivity as 16 and 3.9 respectively.

III. GFET MODEL

The operation of GFET differs significantly from the conventional metal oxide semiconductor field effect transistors

978-1-5386-3974-0/17/$31.00 ©2017 IEEE

(MOSFET). The current conduction in the operation regime of MOSFET is due to either the electrons or holes depending on whether it is n-or p-channel device. Unlike MOSFET, graphene exhibits an ambipolar conduction where both electrons and holes contribute towards the drain current depending on applied bias. The ambipolar conduction observed in graphene is due to its unique band structure. It has been observed that the output characteristics of GFET exhibit a sort of saturation current with a kink feature at high drain to source voltage (V_{ds}). This is characteristics feature of ambipolar channel devices. This behaviour of GFET is well described in [11]. The drain current of the transistor is modelled considering these regions of operation with the contact resistances at the drain and source and access resistance assumed as constant.

A. Determining the Top and Back Gate Capacitance

The application of gate bias results in accumulation of charge carriers along the GFET's channel. Therefore, graphene behaves as a thin metallic capacitor, whose capacitance is affected by the intrinsic electrons and holes density of states (DOS). This results in a quantum capacitance (C_q), defined as a material's intrinsic charge storage which is excited by small electric potential [16]. The quantum capacitance is given by

$$C_q = \frac{\sqrt{n_o}}{\sqrt{\pi}} \frac{q^2}{\hbar v_f} \quad (1)$$

where v_f is the Fermi velocity, q is the electronic charge n_o is minimum sheet carrier concentration which is reported in the range of 0.5×10^{12} cm^{-2} [11].

The quantum capacitance is influenced by the charge density of the channel [17]. In the GFET model considered here, the top gate capacitance C_{top} is a series combination of top gate oxide capacitance, C_e and quantum capacitance, C_q. Therefore, the final top gate capacitance is expressed as $C_{top} = C_q * C_e / (C_q + C_e)$. The effect of quantum capacitance on the total back gate capacitance is negligible as the back gate dielectric capacitance is much smaller than the quantum capacitance.

B. Drain Current Model

In the following, we briefly summarize the model described by Meric *et. al* [11] and Scott *et. al* [12]. According to their model, the output current of a GFET can be distinguished into three operation regimes namely: triode, unipolar and ambipolar (second linear regime). In the triode ($V_{ds} < V_{ds(sat)}$) and unipolar regimes ($V_{ds} = V_{ds(sat)}$), current conduction is due to one-type charge carriers. In addition in the unipolar region pinch-off of the channel is observed which results in the saturation of the drain current. Further increase in V_{ds} ($V_{ds} > V_{ds(sat)}$) leads to GFET entering the ambipolar conduction regime. In the ambipolar regime, increasing V_{ds} results in movement of pinch off region from drain end towards the source end. The current in the ambipolar region is due to both holes and electrons with the pinch off region acting as the point of recombination. The drain current in GFET channel is given by:

$$I_d = \frac{W}{L} \int_0^L en(x) v_{drift}(x) dx \quad (2)$$

where $n(x)$ is the carrier concentration at the point x in the channel, where $x = 0$ at the source end and $x = L$ at the drain end of the channel under the top gate and $v_{drift}(x)$ is the drift velocity of a carrier at position x. At high $V_{ds,}$ drain current saturates owing drift velocity of charge carriers attaining a saturation velocity beyond a critical electric field (E_C). Beyond E_C the drift velocity becomes independent of the electric field. The drift velocity is given by [12]

$$v_{drift}(x) = \frac{\mu E}{1 + \mu E / v_{sat}} \quad (3)$$

where μ is the mobility of the charge carriers and v_{sat} is the saturation drift velocity. The threshold voltage V_0 of the device is defined in [11] as

$$V_0 \cong V^0_{gs(top)} + (C_{back}/C_{top})(V^0_{gs(back)} - V_{gs(back)}) \quad (4)$$

where $V^0_{gs(top)}$ and $V^0_{gs(back)}$ are the top and back gate voltage at the Dirac point, respectively.

In the model, the drain current can be determined by integrating current equation (2) along the channel and including the source drain series resistance, R_S. This results in a closed expression, which is then solved to obtain the drain current in the linear regime [12].

$$I_d = \frac{1}{4R_s}[V_{ds} - V_c + I_o R_s + \sqrt{(V_{ds} - V_c + I_0 R_s)^2 - 4 I_0 R_s} V_{ds} \quad (5)$$

where $V_c = E_C L$ and $I_0 = 2(\frac{W}{L}) \mu_0 V_c C_{top} (V_{gtop} - V_0 - \frac{V_{ds}}{2})$.

As GFET enters the unipolar regime, drain current begins to saturate and becomes independent of the V_{ds}. The source drain saturation voltage ($V_{ds(sat)}$), can be obtained by equating the derivative ($\frac{\delta I_{ds}}{\delta V_{ds}}$) of drain current (5) equal to zero thus resulting in a saturation voltage, $V_{ds(sat)}$ given by [12].

$$V_{ds(sat)} = \frac{2\gamma V g_0}{1+\gamma} + \frac{1-\gamma}{(1+\gamma)^2} \left[V_c - \sqrt{V_c^2 - 2(1+\gamma) V_{g0} V_c} \right] \quad (6)$$

where $\gamma = \frac{R_s}{R_C}$, $R_C = \frac{1}{(W/L)\mu_0 C_{top} V_C}$. The saturation drain current can be then obtained by substituting equation (6) into (5) resulting in the saturation drain current given by [12]

$$I_{d(sat)} = \frac{\gamma}{R_s (1+\gamma)^2} \left[-V_c + (1+\gamma) \; V_{g0} + \sqrt{V_c^2 - 2(1-\gamma) V_c V_{g0}} \right] \quad (7)$$

As V_{ds} surpasses saturation voltage, $V_{ds(sat),}$ GFET enters ambipolar regime. In ambipolar region, charge carriers on the source side are holes while on the drain side are electrons resulting in an ambipolar transport. The drain current contribution due to hole can be described by the saturation current in equation (7). The electron contribution towards the drain current is determined by saturation displacement current

(I_{disp}) as proposed by Umoh *et. al* [13] where μ_n is the alterative carrier mobility:

$$I_{disp} = \frac{W}{2L}\mu_n C_{top} V_{ds(sat)}{}^2 \left(\frac{V_{ds}}{V_{ds(sat)}} - 1\right)^2 \quad (8)$$

Therefore, the total drain current is given by

$$I_d = I_{d(sat)} + I_{disp} \quad (9)$$

C. *Effect of Uniaxial Bending*

In this section, the planar model is modified to include the bending effects. The model considers that the bending occurs along the direction of channel length of the transistor according to the geometry described in Fig. 1. The bending of GFET is assumed to results in a cylindrical shape. Therefore, the capacitance of the top and back gate dielectric is modified as follows:

$$C_{back} = \alpha\varepsilon_{BG} W / \ln\left(1 + \frac{d_{BG}}{R}\right) \quad (10)$$

$$C_e = \alpha'\varepsilon_{TG} W / \ln(1 + \frac{d_{TG}}{R+d_{BG}}) \quad (11)$$

where

$$\alpha = \frac{L_{BG}}{R}$$

and

$$\alpha' = \frac{L_{TG}}{R+d_{BG}+d_{TG}}$$

where α is the bending angle. We can also consider the strain induced effects on the monolayer graphene due to bending. However, in this work we considered only the capacitance effect.

IV. RESULTS

This section of the paper presents results and discussion of Verilog-A implemented model. The application of back-gate voltage, $V_{gs(back)}$, electrostatically dopes the channel region of GFET. A positive $V_{gs(back)}$ bias results in the accumulation of electron (n-type channel) whereas negative $V_{gs(back)}$ bias results in hole accumulation (p-type) in the channel. The output characteristics of GFET for $V_{gs(back)}$ of +40 and -40V is presented below. The Verilog- A model results are compared with the experimental results of GFET developed by Meric et al [11].

A. *Back-gate voltage of -40V*

Fig. 2 shows the output characteristics of GFET for a back-gate bias, $V_{gs(back)}$, -40V at different $V_{gs(top)}$ of -0.3V, -0.8V, -1.3V, -1.8V, -2.3V and -2.8V. The results of the GFET model implemented in Verilog-A shows an excellent agreement with experimental results from [11] for μ=700 $cm^2(V.s)^{-1}$, R_s = 800 and V_c = 0.45V. The output characteristics of GFET resembles MOSFET for high $V_{gs(top)}$ (-2.8V, -2.3V, -1.8V and-1.3V). However, for low $V_{gs(top)}$ (-0.3V), the kink

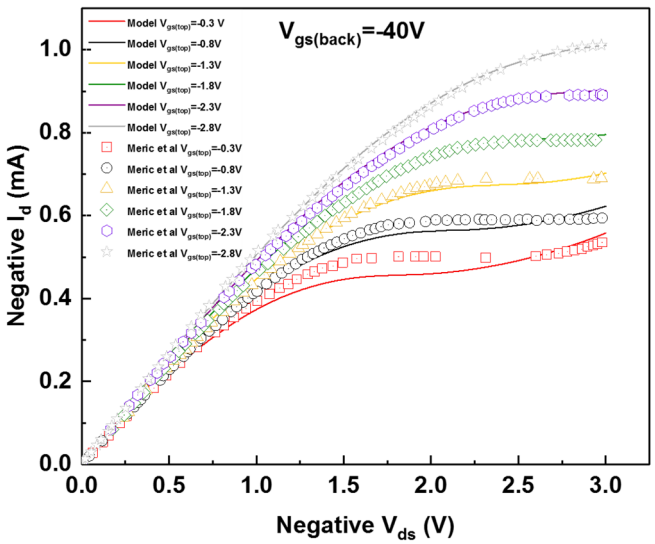

Fig. 2. Output characteristics of Verilog –A model and Meric *et. al* [11] experimental data for $V_{gs(back)}$=-40 and $V_{gs(top)}$ at -0.3V, -0.8V, -1.3V, -1.8V, -2.3V and -2.8V (from bottom to top).

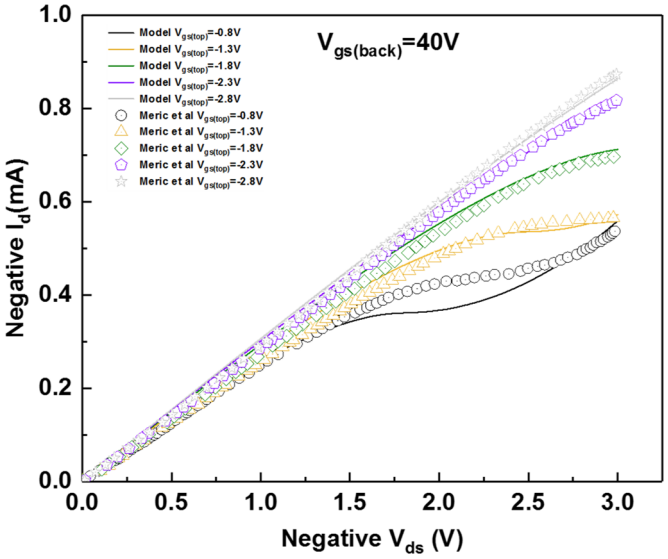

Fig. 3. Output characteristics of Verilog –A model and the Meric *et. al* [11] experimental data for $V_{gs(back)}$ = 40 and $V_{gs(top)}$ at -0.8V, -1.3V, -1.8V, -2.3V and -2.8V (from bottom to top).

behaviour is observed in the output characteristics. This due to transition of the channel from unipolar to ambipolar behaviour.

B. *Back-gate voltage of 40V*

The back-gate voltage of 40V results in the n-channel device. Fig 3 depicts the output characteristics of GFET at different top-gate bias of -2.8V, -2.3V, -1.8V, -1.3V and -0.8V respectively. The good agreement between the model and experimental value is obtained with μ= 1200 cm^2 $(V.s)^{-1}$, R_s = 1500 and V_c = 1.5V. Further, the excellent agreement between the experimental and Verilog-A is obtained at all $V_{gs(top)}$.

C. *Bending Effect on GFET*

The bending effect on GFET performance was considered by using Eq. (10) and (11) for a bending radius of 50mm, 30mm, 20mm and 10mm.The transistor performance remained stable and no noticeable change was observed under the various

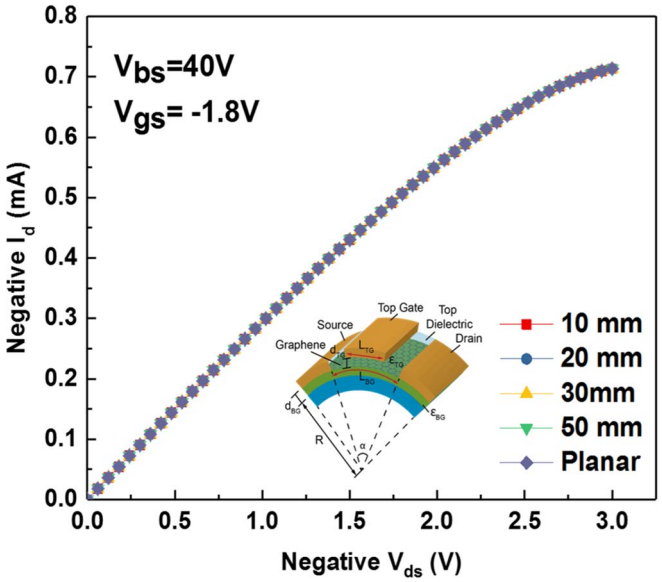

Fig.4. Output characteristics of Verilog-A model for bending radius of 10mm, 20mm, 30mm and 50mm $V_{gs(back)}$ 40V and $V_{gs(top)}$ = -1.8V

bending conditions used in this paper. This is unlike conventional MOSFET, where bending induced variations are clearly observable [14, 18]

The output characteristics of the GFET for $V_{gs(back)}$ = 40V and $V_{gs(top)}$ = -1.8V is depicted in Fig. 4. The stable performance of GFET demonstrates its potential for the development of future flexible electronics applications. However, it is critical to optimise the patterning of rigid components of the device such as metal electrode and gate dielectrics to achieve the required flexibility [2]. Further, presented Verilog-A model does not account the strain-induced effect on graphene, which would be considered in our future models.

V. Conclusion

In summary, we have reported a Verilog-A model of GFET device based on the model proposed by Scott *et. al* [12] and Umoh *et. al* [13]. The developed Verilog-A model has been validated against the experimental output characteristics of Meric *et. al* [11] for different back gate bias of +40V and -40V. In addition, we have also considered the impact of bending on the performance of GFET, modelling it as a cylindrical structure. GFET exhibited a stable performance under different bending radius with no noticeable change in the drain current. Further, the model does not account for strain induced effect on graphene on the device performance. This would be accounted in our future work.

Acknowledgment

This work was supported in part by the European Commission under Grant PITN-GA-2012-317488-CONTEST, in part by the EPSRC Engineering Fellowship for Growth-PRINTSKIN under Grant EP/M002527/1, in part by the EPSRC First Grant under Grant EP/M002519/1, in part by the Graphene Core one under grant agreement 696656.

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