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Joint sparse graph for FBMC/OQAM systems

Lei Wen, Pei Xiao, Razieh Razavi, Muhammad Ali Imran, Mohammed AL-Imari and Jing Lei

***Abstract*—As an advanced non-orthogonal multiple access (NOMA) technique, the low density signature (LDS) has never been used in filter bank multicarrier (FBMC) systems. In this paper, we model a low density weight matrix (LDWM) to utilize the intrinsic interference in FBMC systems, and propose a LDS-FBMC scheme which applies LDS to FBMC signals. In addition, a joint sparse graph for FBMC named JSG-FBMC is proposed to combine single graphs of LDS, LDWM and low density parity-check (LDPC) codes which respectively represent techniques of NOMA, multicarrier modulation and channel coding. By employing the message passing algorithm (MPA), a joint receiver performing detection and decoding simultaneously on the joint sparse graph is designed. Extrinsic information transfer (EXIT) charts and construction guidelines of the joint sparse graph are studied. Simulations show the superiority of JSG-FBMC to state-of-the-art techniques such as OFDM, FBMC, LDS-OFDM, LDS-FBMC and turbo structured LDS-FBMC.**

***Index Terms*—FBMC, Joint sparse graph, Joint detection and decoding, Multicarrier system.**

I. INTRODUCTION

During the 2010s, research interests in multiuser communications have been focused on overloaded transmissions which faces the problem of supporting more users or symbols than the number of resource units available. Under the overloaded conditions, the transmission performance degrades dramatically due to severe multiuser interference (MUI). To tackle this problem, non-orthogonal multiple access (NOMA), including power domain NOMA and code domain NOMA, has been attracting a lot of attention recently [1][2]. Unlike conventional orthogonal multiple access (OMA), NOMA is expected to improve the spectral efficiency and accommodate much more users via non-orthogonal resource allocation. Typical code domain NOMA schemes include low density signature (LDS), sparse code multiple access (SCMA), multiuser shared access (MUSA), pattern division multiple access (PDMA) and so on. As the first proposed scheme of code domain NOMA, LDS utilizes low density spreading techniques [3][4][5][6][7][8]. SCMA is an enhanced version of LDS, with a multi-dimensional constellation designed to generate codebooks and bring the shaping gain [9]. MUSA differs from multicarrier code division multiple access (MC-CDMA) in that it is basically synchronous transmission mechanism when users signals arrive at the base station, while MC-CDMA doesn't have this kind of synchronism requirement in the uplink. In addition, MUSA uses non-binary spreading sequences, while binary spreading sequences are usually applied in conventional MC-CDMA systems [10]. PDMA uses non-orthogonal patterns which are designed to maximize the diversity and minimize the overlaps of multiple users. Multiplexing in PDMA is similar to that in LDS, but the number of subcarriers connected to the same symbols in the LDS graph can be different [11]. Generally speaking, the existing NOMA schemes are mainly applied to OFDM systems. However, in future cellular networks, more advanced waveforms may be utilized. It is urgent to research the combination of NOMA and advanced waveforms other than OFDM.

Recently, filter-bank multicarrier (FBMC) has drawn attention as its ability to overcome OFDM drawbacks such as a loss of spectral efficiency due to the cyclic prefix (CP) insertion, and the incompact spectrum due to large side lobes resulting from the rectangular pulse shaping [12][13]. In this paper, we develop a novel NOMA scheme for FBMC systems. Among different prototype filters in FBMC [14][15][16], we adopt the isotropic orthogonal transform algorithm (IOTA) function as the prototype filter, where the spreading factor of the applied IOTA equals to one. In addition, to show the general effect of the proposed scheme, we also adopt other prototype filters such as the PHYDYAS filter to our design. The contributions of this paper are as follows.

1) The intrinsic interference from real and imaginary branches in FBMC is usually discarded in existing systems [12][13][14]. Note that such intrinsic interference is related to the structure of FBMC transceiver, i.e., when signals are separately processed on real and imaginary branches, it is inevitable to generate the cross-talk between the two branches in the form of intrinsic interference. In fact, the intrinsic interference contains rich information and should be exploited to improve the performance. In this paper, we use a weight matrix which defines neighboring time-frequency positions around the signal of interest to estimate the intrinsic interference. Moreover, we study the weight matrix from graphical view, i.e., to utilize the extra information offered by the intrinsic interference, we model a low density weight matrix (LDWM) to express the most significant positions around the signal. This is essentially the principle of block coding, and the embedded LDWM can improve the performance.

2) As mentioned above, LDS has never been used in FBMC systems. In this paper, we propose a LDS-IOTA scheme by applying LDS to FBMC-IOTA system, which outperforms conventional FBMC-IOTA significantly under overloaded conditions. More importantly, based on graphical models, we propose a joint sparse graph to synergistically combine LDS, LDWM and low density parity-check (LDPC) codes which respectively represent NOMA, multicarrier modulation and channel coding. LDS, LDWM and LDPC codes are related to multiuser interference, FBMC's intrinsic interference and channel interference, respectively. Our proposed scheme is hereinafter referred to as joint sparse graph for IOTA (JSG-IOTA). By using message passing algorithm (MPA) [17], multiuser detection and intrinsic interference utilization as well as channel decoding are jointly performed in JSG-IOTA receiver. To demonstrate advantages of JSG-IOTA, we compare it with LDS-IOTA and turbo structured LDS-IOTA. Simulations

TABLE I
SUMMARY OF KEY NOTATIONS

K	Number of users	$v'_{k,m,n,u}$	Signal at n^{th} chip generated by LDS spreader during the time of index u
M	Data length of each user	$v'^{(\mathrm{i})}_{k,m,n,u}$	Intrinsic interference of the real FFT chain
N	Number of chips for spreading	$v'^{(\mathrm{r})}_{k,m,n,u}$	Intrinsic interference of the imaginary FFT chain
J	Number of parity-check equations of LDPC codes	$\hat{v'}_{k,m,n,u}$	Estimated value of $v'_{k,m,n,u}$
c_n	The n^{th} chip, also represents chip node	$\hat{v'^{\mathrm{R}}}_{k,m,n,u}$	Real part of $\hat{v'}_{k,m,n,u}$
$v_{k,m}$	The m^{th} data symbol of the k^{th} user, also represents variable node	$\hat{v'^{\mathrm{I}}}_{k,m,n,u}$	Imaginary part of $\hat{v'}_{k,m,n,u}$
$i_{n,u}$	The intrinsic interference on the n^{th} subcarrier during the time of index u, also represents intrinsic-interference node	$y(t)$	Received signal
$p_{k,j}$	The j^{th} parity-check equation of the k^{th} user, also represents parity-check node	$g_{n,u}(t)$	synthesis basis
$d_{c,lds}$	Number of symbols that are superimposed at one chip	$z(t)$	AWGN
$d_{v,lds}$	Number of chips that are spread by one symbol	σ_A^2	Variance of AWGN
$d_{v,ldpc}$	Number of parity-check nodes connected to one variable node	$\mathbf{v}$	Transmitted vector
$d_{p,ldpc}$	Number of variable nodes connected to one parity-check node	$\mathbf{v}_{[n]}$	Vectors containing the symbols transmitted by every user that spread its data on the n^{th} chip
$d_{i,ldwm}$	Number of chips connected to one intrinsic-interference node	$\mathbf{r}_{k,m,n,u}$	Received spreading sequence for the data symbol m of the k^{th} user
$d_{c,ldwm}$	Number of intrinsic-interference node connected to one chip	$\mathbf{r}_{[n]}$	Received signature vectors by every user that spread its data on the n^{th} chip
$\mathbf{S}_k$	Spreading matrix for the k^{th} user	$\kappa_{n,k,m}$	Normalization coefficient
$\mathbf{S}$	Low density spreading signatures for OFDM	$L_{c_n \to v_{k,m}}$	LLR delivered from chip node c_n to variable node $v_{k,m}$
$\mathbf{H}_k$	Parity-check matrix for the k^{th} user	$L_{v_{k,m} \to c_n}$	LLR delivered from variable node $v_{k,m}$ to chip node c_n
$\mathbf{H}$	Low density parity-check matrices for LDPC codes	$L_{v_{k,m} \to p_j}$	LLR delivered from variable node $v_{k,m}$ to parity-check node p_j
$\mathbf{W}_n$	Weight matrix for the n^{th} chip	$L_{p_j \to v_{k,m}}$	LLR delivered from parity-check node p_j to variable node $v_{k,m}$
$\mathbf{W}$	Low density weight matrices for intrinsic interferences	$L_{c_n \to i_{n,u}}$	LLR delivered from chip node c_n to intrinsic-interference node $i_{n,u}$
$\mathbf{A}_u$	Transmit power gain of users during the time of index u	$L_{i_{n,u} \to c_n}$	LLR delivered from intrinsic-interference node $i_{n,u}$ to chip node c_n
$\mathbf{E}_{k,u}$	Channel gain for the k^{th} user during the time of index u	$L_{v_{k,m}}$	Final estimation of variable node $v_{k,m}$
ψ_n	Set of data symbols that interfere on chip c_n	CNDD	Chip node detector-decoder
$\psi_n/(k,m)$	Set of data symbols (excluding $v_{k,m}$) that interfere on chip c_n	VNDD	Variable node detector-decoder
$\varepsilon_{k,m}$	Set of chips that $v_{k,m}$ is spread on	PND	Parity-check node decoder
$\varepsilon_{k,m}/n$	Set of chips (excluding c_n) that $v_{k,m}$ is spread on	IND	Intrinsic-interference node decoder
ϕ_j	Set of data symbols that connect to parity-check node $p_{k,j}$	$I_{A,I\&V}$	Average mutual information between the bits on the IND&VNDD edges and the $a\ priori$ LLR
$\phi_j/(k,m)$	Set of data symbols (excluding $v_{k,m}$) that connect to parity-check node $p_{k,j}$	$I_{E,I\&V}$	Average mutual information between the bits on the IND&VNDD edges and the extrinsic LLR
$\omega_{k,m}$	Set of parity-check nodes that connect to $v_{k,m}$	$I_{A,C\&P}$	Average mutual information between the bits on the CNDD&PND edges and the $a\ priori$ LLR
$\omega_{k,m}/j$	Set of parity-check nodes (excluding $p_{k,j}$) that connect to $v_{k,m}$	$I_{E,C\&P}$	Average mutual information between the bits on the CNDD&PND edges and the extrinsic LLR
γ_n	Set of intrinsic interferences that connect to chip c_n	$D_{CNDD}(x)$	Degree distribution polynomials of chip nodes
$\gamma_n/(n,u)$	Set of intrinsic interferences (excluding $i_{n,u}$) that connect to chip c_n	$D_{VNDD}(x)$	Degree distribution polynomials of variable nodes
$\eta_{n,u}$	Set of chips that connect to intrinsic-interference node $i_{n,u}$	$D_{PND}(x)$	Degree distribution polynomials of parity-check nodes
$\eta_{n,u}/n$	Set of chips (excluding c_n) that connect to intrinsic-interference node $i_{n,u}$	$D_{IND}(x)$	Degree distribution polynomials of intrinsic-interference nodes

verify the superiority of JSG-IOTA to other techniques.

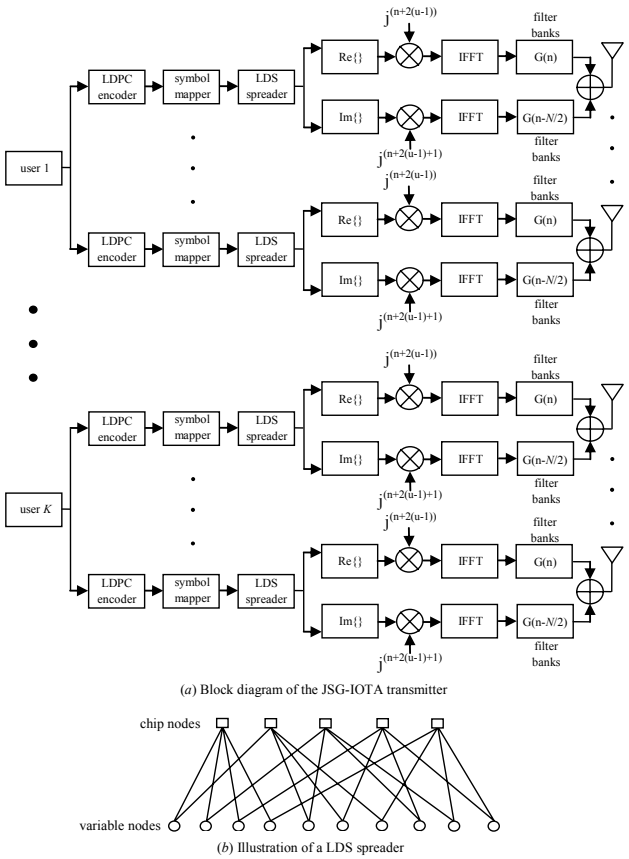
3) In LDS-IOTA, the intrinsic interference utilization and LDS as well as LDPC code are separately designed. Study on a joint sparse graph is more complicated than any other single graphs. We utilize the extrinsic information transfer (EXIT) charts to analyse the joint sparse graph, and summarize its construction guidelines by graph theory.

The rest of this paper is structured as follows. In Section II, the JSG-IOTA model is presented. Section III presents the receiver algorithm. JSG structures and EXIT charts are studied in Section IV. Section V shows construction guidelines of JSG-IOTA. In Section VI, the JSG-IOTA performance is simulated. Section VII gives conclusions of our research.

In this paper, $\mathrm{Re}\{\cdot\}$ (or the superscript R) and $\mathrm{Im}\{\cdot\}$ (or the superscript I) denote the real and imaginary part of a complex signal, respectively. TABLE I shows notations of the paper.

II. JSG-IOTA SYSTEM MODEL

Let us assume a wireless uplink with K users simultaneously transmitting their information to a single base station (BS), where each user and BS have N_T and N_R antennas, respectively. JSG-IOTA block diagrams are presented in Fig.1 and Fig.2. We assume that $N_T = 1$, N is the processing gain of spreading, J is the parity-checks of LDPC codes, and each user has a data vector consisting of M data symbols.



(*a*) Block diagram of the JSG-IOTA transmitter

(*b*) Illustration of a LDS spreader

Fig. 1. JSG-IOTA transmitter model

A. Transmitter Model

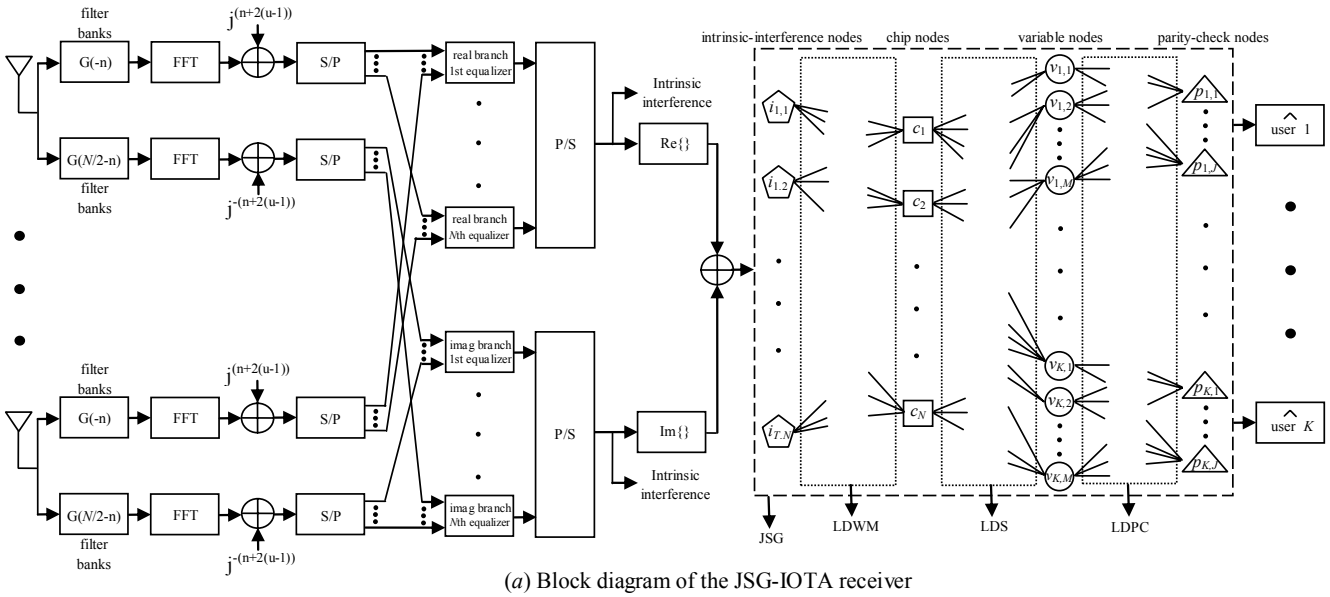
Fig.1 (a) shows the block diagram of JSG-IOTA transmitter, where the IOTA modulators are implemented by separate IFFT blocks followed by a bank of filters for the I and Q components [18][19]. Note that multiuser communications are considered in our model. An $N/2$ rotation of IFFT output is used to shift the zero frequency subcarrier to middle position. Unlike conventional spreading technique, the LDS spreader is configured to guarantee that the ratio of $d_{v,lds}$ to N is small enough ($d_{v,lds}$ is the number of chips that are spread by one symbol), and the number of symbols that are superimposed on each chip, $d_{c,lds}$, is much less than the total number of symbols. Fig.1 (b) illustrates the LDS principle by using a simple exemplary system with 5 subcarriers and 10 data symbols, where chip nodes and variable nodes respectively represent chips and data symbols. It shows that each symbol is spread over 2 chips, and each chip is used by 4 symbols that may belong to different users.

B. Intrinsic Interference Utilization

The JSG-IOTA receiver shown in Fig.2 (a) is implemented by filter banks followed by the FFT block, where the FFT operations are conducted separately for the I and Q branches. The residual signal from I and Q channels is referred to as the intrinsic interference and usually discarded in the demodulation processes. In [18], the intrinsic interference is exploited to improve the channel estimation. The authors presented a general theoretical framework for interference approximation method (IAM) preamble design and applied it to identify the optimal IAM preamble sequence which resulted in a higher gain. In [20], the intrinsic interference is exploited instead of being discarded at the receiver side in order to improve the equalization performance. It was shown in the paper that the real and the time-shifted imaginary components can be highly correlated. This analysis led to a new simple and efficient equalizer utilizing this correlation. Also in [16], an analysis on intrinsic interference of a causal multirate OFDM/OQAM systems is conducted. These findings reveal the fact that the intrinsic information can be exploited for performance improvements. In our work, we find that such intrinsic interference contains rich inherent information that has never been utilized. As shown in Fig.2 (b), the intrinsic interference can be calculated by multiplying neighboring signals with a weight matrix which is determined by the employed pulse shaping filter. It can be seen that for the symbol of frequency and time index (n, u), its intrinsic interference is determined by the neighboring 24 symbols, i.e., 5 frequency-indexed rows and 5 time-indexed columns in the weight matrix. In fact, this is essentially the principle of block coding and the intrinsic interference serve as parity-check/redundant symbols. Therefore, we treat the intrinsic interference as parity symbols, and utilize MPA on the weight matrix to exploit the inherent code structure of the IOTA function. Each element in the weight matrix processes the information received from its adjacent elements. The estimated intrinsic interference is computed based on the weight matrix, whereas the chips combine several parity-check/intrinsic interference observations made by the adjacent elements in the weight matrix. Let $\mathbb{X}$ be the constellation alphabet for the transmitted symbol, the computational complexity of the intrinsic interference utilization is in order of $\mathcal{O}\left(\mid \mathbb{X} \mid^{24}\right)$, representing a very high complexity. There is a trade-off between the performance and the computational complexity. A denser weight matrix will result in more accurate decoding but the complexity will increase exponentially with more nonzero elements of the matrix. Our study reveals that majority elements in the weight matrix have marginal values and can be safely ignored, i.e., regarded as zeros, in order to reduce the computational complexity. Consequently, lower density weight matrices (labeled by different color fonts in Fig.2 (b)) are formed, and the complexity order can be significantly reduced. Detailed analysis of nonzero elements selection is presented in Section V.

C. Receiver Model

Based on above discussion, graphical blocks in the JSG-IOTA receiver in Fig.2 (a) can be configured to include four kinds of nodes: intrinsic-interference nodes $i_{n,u}(n \in [1,N], u \in [0,\mathbb{Z}])$, chip nodes $c_n(n \in [1,N])$, variable nodes $v_{k,m}(k \in [1,K], m \in [1,M])$ and parity-check nodes $p_{k,j}(k \in [1,K], j \in [1,J])$, representing the intrinsic interference corresponding to the symbol on the n^{th} subcarrier during the time of index u, the n^{th} chip, the m^{th} data symbol and the j^{th} parity-check equation of the k^{th} user, respectively.



(*a*) Block diagram of the JSG-IOTA receiver

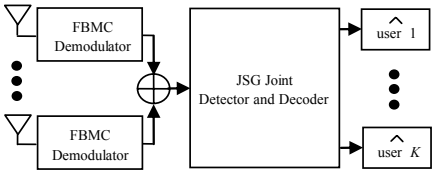
Frequency \ Time	*u*-2	*u*-1	*u*	*u*+1	*u*+2
n-2	0	-0.0021	0	0.0021	0
n-1	-0.0991	-0.1898	0.2486	-0.1898	-0.0991
n	0	-0.5756	1	0.5756	0
n+1	0.0991	-0.1898	-0.2486	-0.1898	0.0991
n+2	0	-0.0021	0	0.0021	0

Real branch

Frequency \ Time	*u*-2	*u*-1	*u*	*u*+1	*u*+2
n-2	0	-0.0021	0	0.0021	0
n-1	0.0991	0.1898	0.2486	0.1898	0.0991
n	0	0.5756	0	-0.5756	0
n+1	-0.0991	0.1898	-0.2486	0.1898	-0.0991
n+2	0	-0.0021	0	0.0021	0

Imaginary branch

(*b*) Weight matrix of the intrinsic interference of the JSG-IOTA



(*c*) Complete receiver structure of JSG-IOTA

Fig. 2. JSG-IOTA receiver model

In the receiver, LDWM, LDS and LDPC respectively represent the low density weight matrix of intrinsic interference in FBMC, the low density signature of LDS [5], and the low density parity-check matrix of LDPC [21]. These three single subgraphs stem from FBMC modulation, NOMA and channel coding, respectively. In the receiver, chip nodes act as a bridge to link intrinsic-interference nodes and variable nodes, meanwhile, variable nodes and parity-check nodes are connected. By doing so, a joint sparse graph, i.e., JSG, is modeled in Fig.2 (a). In addition, Fig.2 (c) shows the complete receiver structure of JSG-IOTA.

III. JOINT DETECTION AND DECODING

In this section, the receiver algorithm based on Fig.2 (a) is presented. The signature and the parity-check matrix for the k^{th} user are $\mathbf{S}_k = [\mathbf{s}_{k,1}, ..., \mathbf{s}_{k,M}] \in \mathbb{C}^{NM}$ and $\mathbf{H}_k = [\mathbf{h}_{k,1}, ..., \mathbf{h}_{k,M}] \in \mathbb{C}^{JM}$, respectively, where $\mathbb{C}$ represents the complex field. The weight matrix for the n^{th} chip is $\mathbf{W}_n = [\mathbf{w}_{n,1}, ..., \mathbf{w}_{n,T}] \in \mathbb{C}^{KT}$. We assume $\mathbf{S} = [\mathbf{S}_1, ..., \mathbf{S}_K] \in \mathbb{C}^{N(MK)}$, $\mathbf{W} = [\mathbf{W}_1, ..., \mathbf{W}_N] \in \mathbb{C}^{K(TN)}$ and $\mathbf{H} = [\mathbf{H}_1, ..., \mathbf{H}_K] \in \mathbb{C}^{J(MK)}$ respectively denote LDS of FBMC, LDWM of intrinsic interferences and parity-check matrices of LDPC. $\mathbf{A}_u = diag(A_{1,u}, ..., A_{K,u})$ is the transmit power gain during the time of index u, and $E_{k,u} = diag(e_{k,1}, ..., e_{k,N})$ is the channel gain for the k^{th} user during the time of index u. $\psi_n = \{(k,m) : \mathbf{s}^n_{k,m} \neq 0\}$ and $\varepsilon_{k,m} = \{n : \mathbf{s}^n_{k,m} \neq 0\}$ are the set of symbols that interfere on chip node c_n and the set of chip nodes that $v_{k,m}$ is spread on, respectively; $\gamma_n = \{(n,u) : \mathbf{w}^n_{n,u} \neq 0\}$ and $\eta_{n,u} = \{n : \mathbf{w}^n_{n,u} \neq 0\}$ are the set of intrinsic interference nodes that connect to chip node c_n and the set of chip nodes that connect to intrinsic-interference node $i_{n,u}$, respectively; $\phi_j = \{(k,m) : \mathbf{h}^j_{k,m} \neq 0\}$ and $\omega_{k,m} = \{j : \mathbf{h}^j_{k,m} \neq 0\}$ are the set of symbols that connect to parity-check node $p_{k,j}$ and the set of parity-check nodes that connect to $v_{k,m}$, respectively.

We define $L_{c_n \to i_{n,u}}$ is the log-likelihood ratio (LLR) transferred from chip node c_n to intrinsic-interference node $i_{n,u}$, $L_{i_{n,u} \to c_n}$ is the LLR transferred from $i_{n,u}$ to c_n. Similarly,

$L_{v_{k,m}\to c_n}$ and $L_{v_{k,m}\to p_{k,j}}$ are the LLR transferred from variable node $v_{k,m}$ to chip node c_n and parity-check node $p_{k,j}$, respectively. $L_{c_n\to v_{k,m}}$ and $L_{p_{k,j}\to v_{k,m}}$ respectively represent the LLR transferred from c_n and $p_{k,j}$ to $v_{k,m}$. $L_{v_{k,m}}$ is the accumulated LLR of $v_{k,m}$. Let $v'_{k,m,n,u} = s^n_{k,m} v_{k,m}$ be the signal at n^{th} chip generated by the LDS spreader during the time of index u, the signal on the data symbol m for the k^{th} user is $\mathbf{r}_{k,m,n,u} = A_{k,u}E_{k,u}v'_{k,m,n,u}$. In our system model, the transmit power of each user is assumed to be one Watt, and the equal power allocation between chips of each user is assumed. The received signal in a multicarrier system (including CP-based OFDM and FBMC) can be written in a general form as [18][19][22][23]

$$y(t) = \sum_{k=1}^{K}\sum_{m=1}^{M}\sum_{n=1}^{N}\sum_{u=-\infty}^{+\infty} \mathbf{r}_{k,m,n,u} g_{n,u}(t) + z(t) \quad (1)$$

where $z(t)$ and $g_{n,u}(t)$ are additive white gaussian channel (variance is σ_A^2) and the synthesis basis which is obtained by the time-frequency shifted version of the prototype function, respectively.

In the OFDM, the synthesis basis can be expressed as [24]

$$g_{n,u}(t) = \begin{cases} \exp(\mathrm{j}2\pi(n-1)Ft) & uT_0 - T_{\mathrm{cp}} \le t \le uT_0 + T \\ 0 & otherwise \end{cases} \quad (2)$$

where $F = 1/T$ is subcarrier frequency spacing, T_{cp} is the length of CP and $T_0 = T + T_{\mathrm{cp}}$ is OFDM symbol duration.

In the JSG-IOTA,

$$g_{n,u}(t) = \exp(j((n-1)+u)\pi/2)\exp(j2\pi(n-1)v_0 t) g(t-u\tau_0) \quad (3)$$

where $g(t)$ is the well-localized IOTA pulse filter, and $v_0\tau_0 = 1/2$. The transmitted signals have symbol duration τ_0 and subcarrier spacing v_0. One can either set $v_0 = F$, $\tau_0 = T/2$ or $v_0 = F/2$, $\tau_0 = T$. Here, we adopt the former approach, i.e., the subcarrier spacing is kept the same as in OFDM, but symbol duration is reduced by half. The received signal can be expressed by (4).

The demodulated signal is

$$\begin{aligned} \hat{v'^{\mathrm{R}}_{k,m,n,u}} &= \mathrm{Re}\left\{\int y(t) g^*_{n,2u}(t)dt\right\} \\ \hat{v'^{\mathrm{I}}_{k,m,n,u}} &= \mathrm{Re}\left\{\int y(t) g^*_{n,2u+1}(t)dt\right\} \end{aligned} \quad (5)$$

By sampling $y(t)$ at rate $1/T_{\mathrm{s}}$ during time interval $[uT - \tau_0, uT + \tau_0]$, the received signal can be written as (6), where $i = -N/2, ..., N/2-1$. Denoting

$$y_i[u] = y[uN + i] = y(uT + iT_{\mathrm{s}}) \quad (7)$$

(6) can be reformed as (8), where $\otimes$ denotes the convolution operation, and

$$D^i_N(x_{k,m,n,u}) = \sum_{n=1}^{N} x_{k,m,n,u}\exp(\mathrm{j}\pi((n-1)+2u)/2) \exp(\mathrm{j}2\pi(n-1)i/N) \quad (9)$$

$$g_i[u] = g[uN + i] = g(uT + iT_{\mathrm{s}}) \quad (10)$$

The phase correction ($j^{((n-1)+2u)}$ for the I channel and $j^{((n-1)+2u+1)}$ for the Q channel) before the IFFT operation is due to the first exponential term in (9). An $N/2$ rotation of IFFT output is needed here to shift the zero frequency subcarrier to middle position.

In the receiver, by sampling the received signal at rate $1/T_{\mathrm{s}}$, (5) can be reformed as (11), where

$$g_i[-u] = g[-uN + i] = g(-NT + iT_{\mathrm{s}}) \quad (12)$$

By repeating the above process on the imaginary branch, (13) can be derived.

Owing to the real-orthogonality condition on $g(t)$, i.e., $\mathrm{Re}\left\{g_{n,u}(t)g^*_{n_0,u_0}(t)\right\} = \delta_{n,n_0}\delta_{u,u_0}$, (5) can be written as

$$\hat{v'_{k,m,n,u}} = \int y(t) g^*_{n,u}(t)dt = A_{k,u}E_{k,u}v'_{k,m,n,u} + \underbrace{\sum_{(n',u')\neq(n,u)} A_{k,u'}E_{k,u'}v'_{k,m,n',u'}\int g_{n',u'}(t)g^*_{n,u}(t)dt + z_{n,u}}_{i_{n,u}} \quad (14)$$

Since the prototype function $g(t)$ is chosen to be well localized both in time and frequency, the intrinsic interference $i_{n,u}$ in (14) only depends on a restricted set of time-frequency positions (n', u') around the signal of interest. Assuming that the channel remains relatively constant at those positions, the intrinsic interference $i_{n,u}$ can be approximated as

$$\begin{aligned} i_{n,u} &= A_{k,u}E_{k,u}\underbrace{\sum_{(n',u')\neq(n,u)} v'_{k,m,n',u'}\int g_{n',u'}(t)g^*_{n,u}(t)dt}_{\mathrm{j}v'^{(\mathrm{i})}_{k,m,n,u}} \\ &= A_{k,u}E_{k,u}\mathrm{j}v'^{(\mathrm{i})}_{k,m,n,u} \end{aligned} \quad (15)$$

The distribution of the weight matrix shown in Fig.2 (b) stems from the above formula, and is determined by IOTA pluse shaping $g(t)$. Combining (14) and (15) yields

$$\hat{v'_{k,m,n,u}} = A_{k,u}E_{k,u}[v'_{k,m,n,u} + \mathrm{j}v'^{(\mathrm{i})}_{k,m,n,u}] + z_{n,u} \quad (16)$$

In Fig.2 (a), the input to the real and the imaginary branch equalizers at the JSG-IOTA receiver can be expressed as

$$\begin{aligned} y^{\mathrm{R}}_{k,m,n,u} &= A_{k,u}E_{k,u}[v'^{\mathrm{R}}_{k,m,n,u} + \mathrm{j}v'^{(\mathrm{i})}_{k,m,n,u}] + z^{\mathrm{R}}_{n,u} \\ y^{\mathrm{I}}_{k,m,n,u} &= A_{k,u}E_{k,u}[v'^{(\mathrm{r})}_{k,m,n,u} + \mathrm{j}v'^{\mathrm{I}}_{k,m,n,u}] + z^{\mathrm{I}}_{n,u} \end{aligned} \quad (17)$$

where $v'^{(\mathrm{i})}_{k,m,n,u}$ and $v'^{(\mathrm{r})}_{k,m,n,u}$ are the FBMC's intrinsic interference of real and imaginary FFT chains, respectively. Given the knowledge of the channel state, the transmitted signal can be recovered by zero forcing (ZF) equalization, which is expressed by (18), where $z'_{n,u}$ denote the combined noise term. As a result, the FBMC's intrinsic interference can be eliminated. An MMSE equalization can be designed similarly.

For the joint sparse graph, there are two sets of soft information coming from the intrinsic interference: the first one is combined by the Q component of the output of the real branch equalizer and I component of the output of the imaginary branch equalizer, i.e., $v'^{(\mathrm{r})}_{k,m,n,u} + \mathrm{j}v'^{(\mathrm{i})}_{k,m,n,u}$, while the second one is calculated based on neighboring time-frequency positions around the signal of interest. If the

$$y(t)=\sum_{k=1}^{K}\sum_{m=1}^{M}\sum_{n=1}^{N}\sum_{u=-\infty}^{+\infty}[\mathbf{r}^{\mathrm{R}}_{k,m,n,u}g_{n,2u}(t)+\mathbf{r}^{\mathrm{I}}_{k,m,n,u}g_{n,2u+1}(t)]+z(t) \tag{4}$$
$$=\sum_{k=1}^{K}\sum_{m=1}^{M}\sum_{n=1}^{N}\sum_{u=-\infty}^{+\infty}[\mathbf{r}^{\mathrm{R}}_{k,m,n,u}g(t-2u\tau_0)+\mathrm{j}\mathbf{r}^{\mathrm{I}}_{k,m,n,u}g(t-(2u+1)\tau_0)]\times\exp(\mathrm{j}((n-1)+2u)/2)\exp(\mathrm{j}2\pi(n-1)v_0t)+z(t)$$

$$y(uT+iT_{\mathrm{s}})=\sum_{k=1}^{K}\sum_{m=1}^{M}\sum_{n=1}^{N}\sum_{l=-\infty}^{+\infty}[\mathbf{r}^{\mathrm{R}}_{k,m,n,l}g(uT+iT_{\mathrm{s}}-lT)+\mathrm{j}\mathbf{r}^{\mathrm{I}}_{k,m,n,l}g(uT+iT_{\mathrm{s}}-lT-T/2)] \tag{6}$$
$$\times\exp(\mathrm{j}\pi((n-1)+2l)/2)\exp(\mathrm{j}2\pi(n-1)i/N)+z$$

$$y_i[u]=\sum_q g(qT+iT_{\mathrm{s}})\left\{\sum_{n=1}^{N}\mathbf{r}^{\mathrm{R}}_{k,m,n,u-q}\exp[\mathrm{j}\pi((n-1)+2u-2q)/2]\exp[\mathrm{j}2\pi(n-1)i/N]\right\} \tag{8}$$
$$+\sum_q g(qT+iT_{\mathrm{s}}-T/2)\left\{\sum_{n=1}^{N}\mathrm{j}\mathbf{r}^{\mathrm{I}}_{k,m,n,u-q}\exp[\mathrm{j}\pi((n-1)+2u-2q)/2]\exp[\mathrm{j}2\pi(n-1)i/N]\right\}+z$$
$$=\sum_q\left\{g_i[q]D^i_N(\mathbf{r}^{\mathrm{R}}_{k,m,n,u-q})+g_{i-\frac{N}{2}}[q]D^i_N(\mathrm{j}\mathbf{r}^{\mathrm{I}}_{k,m,n,u-q})\right\}+z$$
$$=g_i[u]\otimes D^i_N(\mathbf{r}^{\mathrm{R}}_{k,m,n,u})+g_{i-\frac{N}{2}}[u]\otimes D^i_N(\mathrm{j}\mathbf{r}^{\mathrm{I}}_{k,m,n,u})+z$$

$$\hat{v'^{\mathrm{R}}_{k,m,n,u}}=\mathrm{Re}\left\{T_{\mathrm{s}}\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1}\sum_{l=-\infty}^{+\infty}y(lT+iT_{\mathrm{s}})g^*_{n,2u}(lT+iT_{\mathrm{s}})\right\} \tag{11}$$
$$=\mathrm{Re}\left\{T_{\mathrm{s}}\exp[-\mathrm{j}\pi((n-1)+2u)/2]\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1}\sum_{l=\infty}^{+\infty}y_i[l]g_i[l-u]\exp[-\mathrm{j}2\pi(n-1)i/N]\right\}$$
$$=\mathrm{Re}\left\{T_{\mathrm{s}}\exp[-\mathrm{j}\pi((n-1)+2u)/2]\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1}y_i[u]\otimes g_i[-u]\exp[-\mathrm{j}2\pi(n-1)i/N]\right\}$$
$$=\mathrm{Re}\left\{T_{\mathrm{s}}j^{((n-1)+2u)}\sum_{i=-\frac{N}{2}}^{\frac{N}{2}-1}y_i[u]\otimes g_i[-u]\exp[-\mathrm{j}2\pi(n-1)(i+\frac{N}{2})/N]\right\}$$

difference between these two values is small enough, we reach a decision that its correlated chips are highly reliable, and set $\Pr(\hat{v'_{k,m,n,u}}=v'_{k,m,n,u})=1$. Otherwise the soft information of the correlated chips needs to be updated. It should be noted that the intrinsic interference node in Fig.2 (a) is not the first set mentioned above, but the second one, which means that these nodes are calculated based on the weight matrix. The weight matrix of the intrinsic interference is represented by a sparse graph to propagate the information, and each message will be calculated iteratively from the previous values of the neighboring nodes. In a typical run, intrinsic-interference nodes and variable nodes update at the same time. For the chips in error and their corresponding intrinsic-interference nodes, their LLR can be calculated by (19), where $\eta_{n,u}/n$ is the set of chips (excepting c_n) that connect to intrinsic-interference node $i_{n,u}$.

In LDS-IOTA and LDPC code, variable nodes only receive LLR from chip nodes and parity-check nodes, respectively. Nevertheless, in JSG-IOTA, calculation of $L_{v_{k,m}\to c_n}$ uses LLRs of chip nodes and parity-check nodes at the same time.

$$L_{v_{k,m}\to c_n}=\sum_{n'\in\varepsilon_{k,m}\backslash n}L_{c_{n'}\to v_{k,m}}+\sum_{j\in\omega_{k,m}}L_{p_{k,j}\to v_{k,m}} \tag{20}$$

where $\varepsilon_{k,m}\setminus n$ represents the set of chip nodes (excepting c_n) which $v_{k,m}$ is spread on. When executing MPA for the joint detection and decoding, the more kinds of nodes that are connected to a variable node, the more reliable information that can be utilized when processing that variable node.

The updating of $L_{v_{k,m}\to p_{k,j}}$ utilizes LLRs of chip nodes

$$\hat{v'^{\mathrm{I}}_{k,m,n,u}} = \mathrm{Re}\left\{T_s j^{-((n-1)+2u)} \sum_{i=1}^{N} y_{i-1}[u] \otimes g_{i-1-\frac{N}{2}}[-u]\exp[-\mathrm{j}2\pi(n-1)(i-1)/N]\right\} \tag{13}$$

$$\begin{aligned}\hat{v'_{k,m,n,u}} &= \mathrm{Re}\left\{y^{\mathrm{R}}_{k,m,n,u}/A_{k,u}E_{k,u}\right\} + \mathrm{jIm}\left\{y^{\mathrm{I}}_{k,m,n,u}/A_{k,u}E_{k,u}\right\} + (z^{\mathrm{R}}_{n,u}/A_{k,u}E_{k,u}) + (z^{\mathrm{I}}_{n,u}/A_{k,u}E_{k,u}) \\ &= {v'}^{\mathrm{R}}_{k,m,n,u} + \mathrm{j}{v'}^{\mathrm{I}}_{k,m,n,u} + z'_{n,u}\end{aligned} \tag{18}$$

$$L_{i_{n,u}\to c_n} = \frac{\sum_{c_n=1} \exp(\sum_{n'\in\eta_{n,u}\backslash n} \frac{c_{n'}}{2} L_{c_{n'}\to i_{n,u}} - \frac{1}{2\sigma_A^2} \parallel {v'}^{(\mathrm{r})}_{k,m,n,u} + \mathrm{j}{v'}^{(\mathrm{i})}_{k,m,n,u} - i_{n,u} \parallel^2)}{\sum_{c_n=0} \exp(\sum_{n'\in\eta_{n,u}\backslash n} \frac{c_{n'}}{2} L_{c_{n'}\to i_{n,u}} - \frac{1}{2\sigma_A^2} \parallel {v'}^{(\mathrm{r})}_{k,m,n,u} + \mathrm{j}{v'}^{(\mathrm{i})}_{k,m,n,u} - i_{n,u} \parallel^2)} \tag{19}$$

and parity-check nodes as well,

$$L_{v_{k,m}\to p_{k,j}} = \sum_{j'\in\omega_{k,m}\backslash j} L_{p_{k,j'}\to v_{k,m}} + \sum_{n\in\varepsilon_{k,m}} L_{c_n\to v_{k,m}} \tag{21}$$

where $\omega_{k,m} \setminus j$ represents the set of parity-check nodes (excepting $p_{k,j}$) which link to $v_{k,m}$.

In terms of chip nodes and parity-check nodes, their messages are updated simultaneously. In LDS-IOTA, chip nodes only gather LLR of variable nodes. However, in JSG-IOTA, chip nodes utilizes LLRs of both intrinsic-interference nodes and variable nodes,

$$L_{c_n\to i_{n,u}} = \sum_{(n',u')\in\gamma_n\backslash(n,u)} L_{i_{n',u'}\to c_n} + \sum_{(k,m)\in\psi_n} L_{v_{k,m}\to c_n} \tag{22}$$

where $\gamma_n/(n,u)$ represents the set of intrinsic interferences (excepting $i_{n,u}$) which link to c_n.

$L_{c_n\to v_{k,m}}$ is calculated by (23), where $\psi_n\backslash(k,m)$ represents the set of symbols (excepting $v_{k,m}$) which link to c_n, $\mathbf{v}$ represents the transmitted vector, $p(\hat{v'_{k,m,n,u}}|\mathbf{v})$ and $p_n(v_{k',m'})$ can be respectively written as

$$p(\hat{v'_{k,m,n,u}}|\mathbf{v}) = \exp(-\frac{1}{2\sigma_A^2} \parallel \hat{v'_{k,m,n,u}} - \mathbf{r}^{\mathrm{T}}_{[n]}\mathbf{v}_{[n]} \parallel^2) \tag{24}$$

$$p_n(v_{k',m'}) = \exp(L_{v_{k',m'}\to c_n}) \tag{25}$$

Substituting (24) and (25) into (23), (26) can be derived, where $\kappa_{n,k,m}$ represents normalization factor, and

$$\max^*(a,b) \triangleq \log(e^a + e^b) \tag{27}$$

Calculation of the parity-check nodes can be expresses by

$$L_{p_{k,j}\to v_{k,m}} = \alpha^{-1}(\sum_{(k',m')\in\phi_j\backslash(k,m)} \alpha(L_{v_{k',m'}\to p_{k,j}})) \tag{28}$$

where $\phi_j \setminus (k,m)$ represents the set of symbols (excepting $v_{k,m}$) which link to $p_{k,j}$, and

$$\alpha(x) = \mathrm{sign}(x) \times (-\log\tan(\mid x \mid /2)) \tag{29}$$

The accumulated LLR of $v_{k,m}$ can be given by

$$L_{v_{k,m}} = \sum_{n\in\varepsilon_{k,m}} L_{c_n\to v_{k,m}} + \sum_{j\in\omega_{k,m}} L_{p_{k,j}\to v_{k,m}} \tag{30}$$

Finally, $v_{k,m}$ is derived as $\hat{v_{k,m}} = \arg\underset{v_{k,m}}{max} L_{v_{k,m}}$. The iteration stops once the syndromes are zeros or the maximum iteration is satisfied.

IV. EXIT CHART ANALYSIS OF JOINT SPARSE GRAPH

A. JSG Structure

Based on the receiver algorithm shown in Section III, the updating of chip nodes depends on $a\ priori$ information of neighboring intrinsic-interference nodes and variable nodes. Similarly, the updating of variable nodes utilize information of chip nodes and parity-check nodes. On the other hand, for intrinsic-interference nodes and parity-check nodes, their extrinsic messages are updated only depending on one side of $a\ priori$ information, i.e., neighboring chip nodes and variable nodes, respectively. We respectively define the sets of intrinsic-interference nodes, chip nodes, variable nodes and parity-check nodes as intrinsic-interference node decoder (IND), chip node detector-decoder (CNDD), variable node detector-decoder (VNDD) and parity-check node decoder (PND). The iterative diagram of the joint sparse graph is illustrated in Fig. 3, which is different from any existing techniques such as LDS [4] and LDPC [25]. More importantly, the iterative part of LDWM for FBMC has never been proposed before.

To explain the JSG-IOTA receiver more clearly, we present a tree structure of the joint sparse graph in Fig. 4. As the channel and IOTA demodulated information is fed into chip node directly, the tree structure is rooted at chip node c_n where we name it level 0 of the tree. According to Fig.2 and Fig. 3, each chip node is linked to some intrinsic-interference nodes and variable nodes via low density edges, thus we respectively use long dash lines and bold lines to distinguish these two connections in Fig. 4. Hence, at level 1 of the tree, there are two kinds of nodes, i.e., intrinsic-interference nodes (pentagons) and variable nodes (circles), which are connected to c_n at level 0 by different lines. For the intrinsic-interference nodes at level 1, each of them is linked to other chip nodes (rectangles) at level 2 via long dash lines. For the variable nodes at level 1, each of them is not only linked to some chip nodes at level 2 via bold lines, but also connected to some

$$
\begin{aligned}
L_{c_n \to v_{k,m}} &= f(v_{k,m} | \hat{v'}_{k,m,n,u}, L_{i_{n,u} \to c_n}, L_{v_{k',m'} \to c_n}, (k',m') \in \psi_n \setminus (k,m)) \\
&= \log(\sum p(\hat{v'}_{k,m,n,u} | \mathbf{v}) p_n(\mathbf{v} | v_{k,m})) \\
&= \log(\sum p(\hat{v'}_{k,m,n,u} | \mathbf{v}) \prod_{(k',m') \in \psi_n \setminus (k,m)} p_n(v_{k',m'}))
\end{aligned} \tag{23}
$$

$$
L_{c_n \to v_{k,m}} = \kappa_{n,k,m} \max_{\mathbf{v}_{[n]}}{}^{*} \Big(\sum_{(n,u)} L_{i_{n,u} \to c_n} + \sum_{(k',m') \in \psi_n \setminus (k,m)} L_{v_{k',m'} \to c_n} - \frac{1}{2\sigma_A^2} \parallel \hat{v'}_{k,m,n,u} - \mathbf{r}_{[n]}^{\mathrm{T}} \mathbf{v}_{[n]} \parallel^2 \Big) \tag{26}
$$

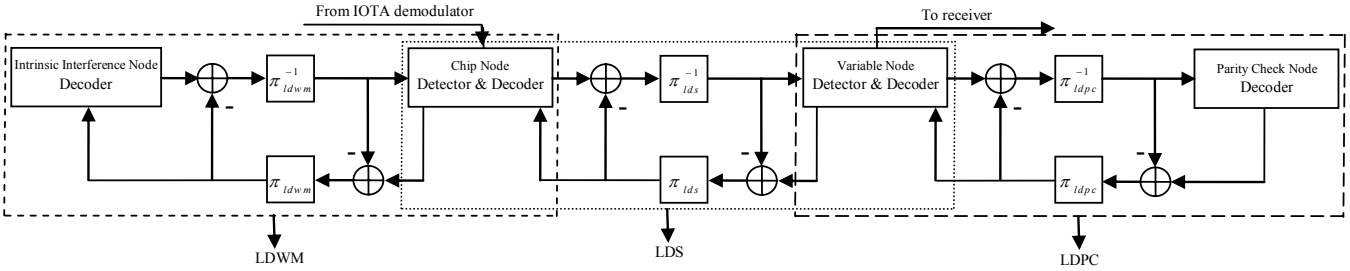


Fig. 3. Iterative diagram of the joint sparse graph

parity-check nodes (triangles) at level 2 via other kind of lines, i.e., short dash lines. Similarly, the chip nodes and the parity-check nodes at level 2 can generate more intrinsic-interference nodes and variable nodes via corresponding kinds of lines, which are drawn at level 3. Note that at level 3, the intrinsic-interference nodes have only one kind of connection to chip nodes at level 2, while the variable nodes have two kinds of connection to chip nodes and parity-check nodes at level 2. Obviously, such a tree structure is novel as it has four kinds of nodes and three kinds of edges. Note that different levels of the tree have specific kinds of nodes, i.e., odd level (level 1 or 3) consists of intrinsic-interference nodes and variable nodes, while even level (level 2) consists of chip nodes and parity-check nodes. Chip nodes and variable nodes are important due to their bridge function on the tree, and the messages of different nodes can be passed to any other kinds of nodes via the edges.

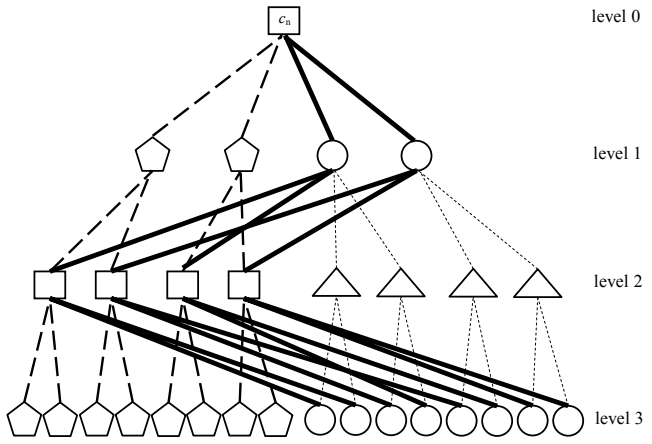


Fig. 4. Tree of the joint sparse graph

Moreover, we depict the Tanner figure of the joint sparse graph in Fig. 5 [26]. According to the receiver algorithm presented in Section III and the tree structure shown in Fig. 4, CNDD and PND compute LLRs at the same time, while IND and VNDD compute LLRs synchronously. Hence, we lay the even level nodes, i.e., CNDD (rectangles) and PND (triangles), on the left, and lay the odd level nodes, i.e., IND (pentagons) and VNDD (circles), on the right. It can be seen that, CNDD is connected to IND through long dash lines, meanwhile, it is also connected to VNDD through bold lines. In addition, VNDD is not only linked to CNDD, but also linked to PND through short dash lines. Therefore, FBMC modulation, NOMA, channel coding and the their combination, are shown in the figure.

B. EXIT Chart Analysis

SUI-3, a typical multipath fading channel model [27], is applied in the following analysis and the simulations, where the channel power delay profile is given in TABLE II. We define that $I_{A,I\&V}$ represents average mutual information (A-MI) between the symbols on IND&VNDD edges and $a\ priori$ information, $I_{E,I\&V}$ represents AMI between the symbols on IND&VNDD edges and extrinsic information. $L_{c_n \to i_{n,u}}$, $L_{c_n \to v_{k,m}}$ and $L_{p_{k,j} \to v_{k,m}}$ are both modeled as Gaussian-like distributions. $A\ priori$ information is computed as follows

$$
A = \mu_A x + z_n \tag{31}
$$

where z_n is AWGN (variance is σ_A^2); x is the symbol on edges; $\mu_A = \sigma_A^2/2$. $I_{A,I\&V} = I(X;A)$ is expressed as

$$
\begin{aligned}
I_{A,I\&V} = \frac{1}{2} \sum_{x=-1,1} \int_{-\infty}^{+\infty} & p_A(\beta | X = x) \\
& \log_2 \frac{2 p_A(\beta | X = x)}{p_A(\beta | X = -1) + p_A(\beta | X = 1)} d\beta
\end{aligned} \tag{32}
$$

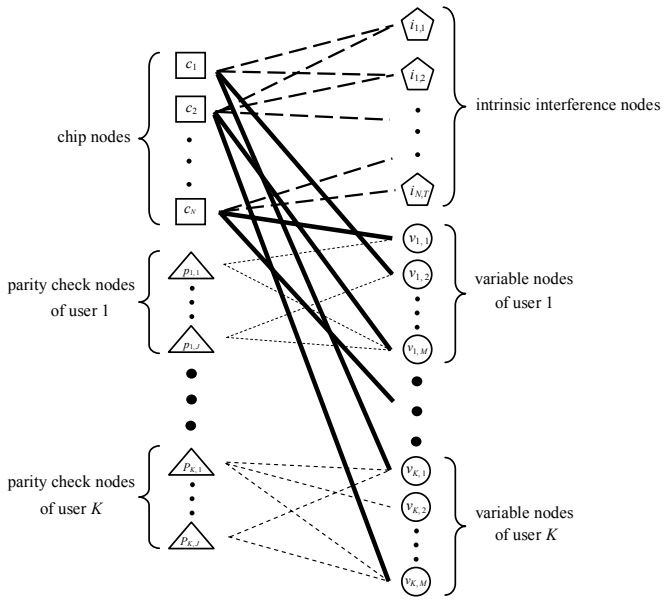


Fig. 5. Tanner figure of the joint sparse graph

As the conditional probability density function $p_A(\beta|X = x)$ is related to A,

$$I_{A,I\&V}(\sigma_A) = 1 - \int_{-\infty}^{+\infty} \frac{e^{-((\beta-\sigma_A^2/2)^2/2\sigma_A^2)}}{\sqrt{2\pi}\sigma_A} \log_2(1+e^{-\beta})d\beta \tag{33}$$

We assume

$$B(\sigma) := I_{A,I\&V}(\sigma_A = \sigma) \tag{34}$$

with

$$\lim_{\sigma\to 0} B(\sigma) = 0 \quad \lim_{\sigma\to\infty} B(\sigma) = 1 \tag{35}$$

where $\sigma \geq 0$. According to (19), (20) and (21), the EXIT formula of IND&VNDD is written as

$$I_{E,I\&V}(I_{A,I\&V}, d_{i,ldwm}, d_{v,lds}, d_{v,ldpc}) = B(\sqrt{(d_{i,ldwm} + d_{v,lds} + d_{v,ldpc} - 1)(B^{-1}(I_{A,I\&V}))^2}) \tag{36}$$

where $d_{i,ldwm}$, $d_{v,lds}$ and $d_{v,ldpc}$ are the degrees of IND in LDWM, VNDD in LDS and VNDD in LDPC, respectively. Hence, differing from existing techniques that only one kind of graph is utilized [4][25], all of LDWM, LDS and LDPC have impact on IND&VNDD.

We define that $I_{A,C\&P}$ represents AMI between the symbols on CNDD&PND edges and *a priori* information, $I_{E,C\&P}$ represents AMI between the symbols on CNDD&PND edges and extrinsic information. CNDD collects LLRs from IND, VNDD and the demodulator, while PND only receives LLR from VNDD. Updating of CNDD and PND is shown in (22), (26) and (28). $L_{i_{n,u}\to c_n}$, $L_{v_{k,m}\to c_n}$ and $L_{v_{k,m}\to p_{k,j}}$ are modeled as the output of multipath fading channels. As the updating of CNDD and PND is complicated, their EXIT curves are derived through simulations. TABLE III shows parameters of the EXIT chart analysis. Note that the system loading is described as the ratio of the number of variable nodes to the number of chip nodes. Fig. 6 depicts the EXIT charts of JSG-IOTA by red lines and LDS-IOTA by blue lines at E_b/N_0 = 12 dB. The trajectory in the figure shows that at least seven iterations are required to reach the intersection point of LDS-IOTA, whereas only five iterations are needed to reach the intersection point of JSG-IOTA. This is attributed to the more efficient message passing and the more reliable information utilized by chip nodes and variable nodes in JSG-IOTA than that in LDS-IOTA. Therefore, JSG-IOTA can reach its intersection point faster than LDS-IOTA.

TABLE II
SUI-3 CHANNEL MODEL DEFINITION

	Tap 1	Tap 2	Tap3	Units
Delay	0	0.5	1	us
Power	0	-5	-10	dB

TABLE III
SYSTEM PARAMETERS

Number of users	4
Number of chip nodes	64
Number of variable nodes	128
Number of intrinsic-interference nodes	128
Number of parity-check nodes	64
FFT size	64
Sub-channel bandwidth	15KHz
Multipath channel model	SUI-3
System loading	200%
Chips linked to each variable node	$d_{v,lds} = 2$
Variable nodes linked to each chip	$d_{c,lds} = 4$
Chips linked to each intrinsic-interference node	$d_{i,ldwm} = 4$
Intrinsic-interference nodes linked to each chip	$d_{c,ldwm} = 4$
Parity-check nodes linked to each variable node	$d_{v,ldpc} = 3$
Variable nodes linked to each parity-check node	$d_{p,ldpc} = 6$
Modulation	OQPSK

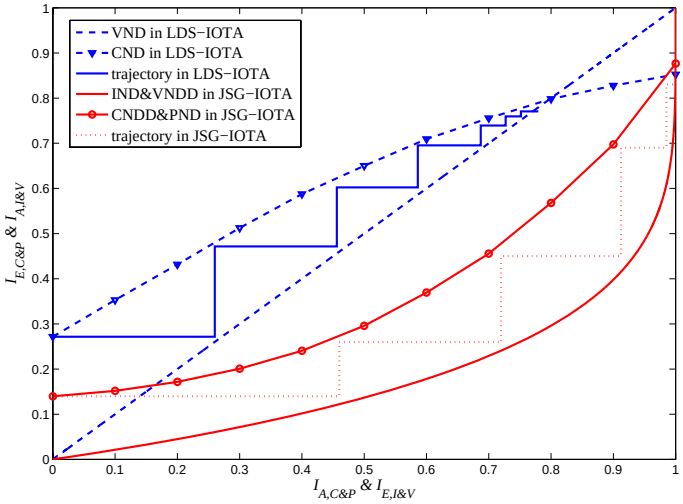


Fig. 6. EXIT chart at E_b/N_0 = 12 dB

TABLE IV
DEGREE DISTRIBUTION

Scheme	$D_{\text{IND}}(x)$	$D_{\text{CNDD}}(x)$	$D_{\text{VNDD}}(x)$	$D_{\text{PND}}(x)$
Deg_a	x^3	x^7	x^4	x^5
Deg_b	x^3	$0.1x^6+0.8x^7+0.1x^8$	$0.575x^4+0.425x^5$	$0.15x^5+0.85x^6$
Deg_c	x^3	$0.075x^6+0.85x^7+0.075x^8$	$0.315x^3+0.685x^4$	$0.63x^4+0.37x^5$
Deg_d	x^3	$0.045x^6+0.91x^7+0.045x^8$	$0.375x^3+0.625x^4$	$0.75x^4+0.25x^5$

V. EXIT CHART ASSISTED JSG CONSTRUCTION

In this section, we discuss how to use EXIT charts to optimize the JSG construction [28].

A. Degree Distribution

We define the the following formulas, i.e.,

$$D_{\text{IND}}(x)=\sum_{d=1}^{d_{i,ldwm}} P_{\text{IND}}x^{d-1} \tag{37}$$

$$D_{\text{CNDD}}(x)=\sum_{d=1}^{d_{c,ldwm}+d_{c,lds}} P_{\text{CNDD}}x^{d-1} \tag{38}$$

$$D_{\text{VNDD}}(x)=\sum_{d=1}^{d_{v,lds}+d_{v,ldpc}} P_{\text{VNDD}}x^{d-1} \tag{39}$$

$$D_{\text{PND}}(x)=\sum_{d=1}^{d_{p,ldpc}} P_{\text{PND}}x^{d-1} \tag{40}$$

as the degree distribution polynomials of IND, CNDD, VNDD and PND, respectively, where P_{IND}, P_{CNDD}, P_{VNDD} and P_{PND} represent the fractions of all edges connected to the corresponding nodes. According to Fig.2 (b), we assume that each intrinsic-interference node is determined by four neighboring time-frequency positions around the signal of interest, hence $d_{i,ldwm}=4$. Nevertheless, other degrees can be varied.

In EXIT charts, to obtain a as low bit error rate (BER) as possible, EXIT curves have to intersect at (I_A, I_E) = (1, 1) point [29][30]. The JSG in TABLE III is a regular graph without any optimization. As revealed by [29] and [30], a better code will generate an EXIT chart that has a higher intersection point closing to the (1, 1) point. Therefore, the construction strategy is to adjust the EXIT charts in order to approach the (1, 1) point while keeping the tunnel open. Based on Fig. 5, chip nodes utilize LLRs from FBMC demodulator, IND and VNDD, while parity-check nodes only utilizes LLR from VNDD without direct FBMC information, hence parity-check nodes reduce AMI of CNDD&PND. Once the ratio of the edges connected to parity-check nodes is decreased slightly, the curve of CNDD&PND should be higher, consequently the optimized shape will generate a near-capacity JSG. More importantly, the EXIT charts can be intersected more closely to the (1, 1) point and a better performance can be achieved. According to the discussion, TABLE IV presents different degree distributions. It can be seen that Deg_a is a regular JSG which is shown in TABLE III, while others are irregular JSG. Obviously, comparing with Deg_a, Deg_c and Deg_d mildly reduce the degree of parity-check nodes, and the polynomials of variable nodes and chip nodes are adjusted correspondingly. By contrast, Deg_b raises the edge proportion of parity-check nodes.

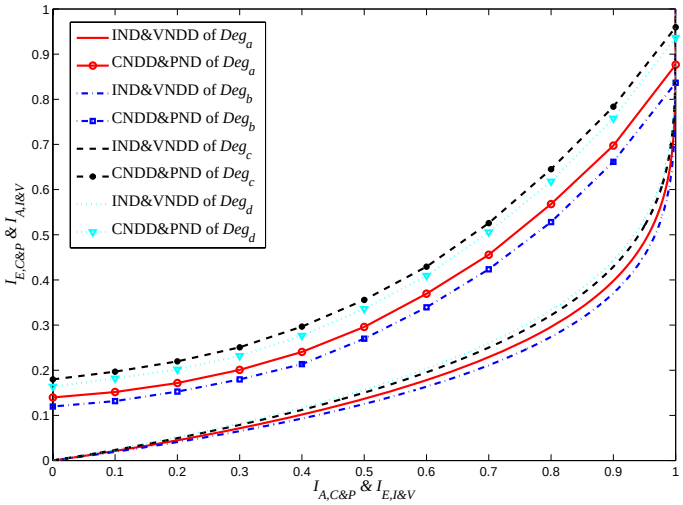


Fig. 7. EXIT chart for different degree distributions

Fig.7 depicts EXIT charts for different degree distributions at E_b/N_0 = 12 dB. In TABLE IV, Deg_c and Deg_d slightly decrease the weight of the parity-check nodes, as a result, their AMI between the symbols and the extrinsic information of CNDD&PND both lift up in Fig.7. In addition, their intersection points become higher, meaning that a lower BER can be obtained. On the contrary, Deg_b increases the weight of parity-check nodes, and its AMI as well as intersection point both sink. Therefore, a lower density of PND in general results in a scheme that is more robust to interference on the joint sparse graph. It is noteworthy that although the PND weight of Deg_d is less than that of Deg_c, but the intersection point of Deg_d is lower than that of Deg_c, indicating Deg_c outperforms Deg_d. This is related to the function of PND, i.e., performing parity-check for error correction. As explained above, it is necessary to design the degree distributions carefully and strike a balance between the optimization processing and the original function of the parity-check node. This ensures efficient operations of belief propagation executed at the JSG-IOTA receiver. For the joint sparse graph, Deg_c is a preferable choice since it has the highest intersection point among these schemes.

B. Short Cycle

Based on graph theory, the edge number of the shortest cycle in a graph is referred to as the girth. Avoiding short

cycles is important, since a short cycle may reduce the efficiency of message passing due to self-propagated information transmitting to the same node in limited iterations [31]. The EXIT charts shown in Fig.7 do not take account of cycles, and their girths are four.

Fig. 8 illustrates the EXIT charts for girths of four, six and eight in JSG at E_b/N_0 = 12 dB. Deg_c is chosen as the degree distribution. In the case of girth = 8, the degree distributions have to be adjusted slightly, i.e., Deg_c': $D_{IND}(x)$ = x^3, $D_{CNDD}(x)$ = $0.07x^6+0.86x^7+0.07x^8$, $D_{VNDD}(x)$ = $0.31x^3+0.69x^4$ and $D_{PND}(x)$ = $0.62x^4+0.38x^5$. We can see that the curves of girth = 4 and girth = 6 almost overlap, while that of girth = 8 is higher than other two scenarios. Therefore, our advice is to eliminate cycles with length of four and six while designing a JSG.

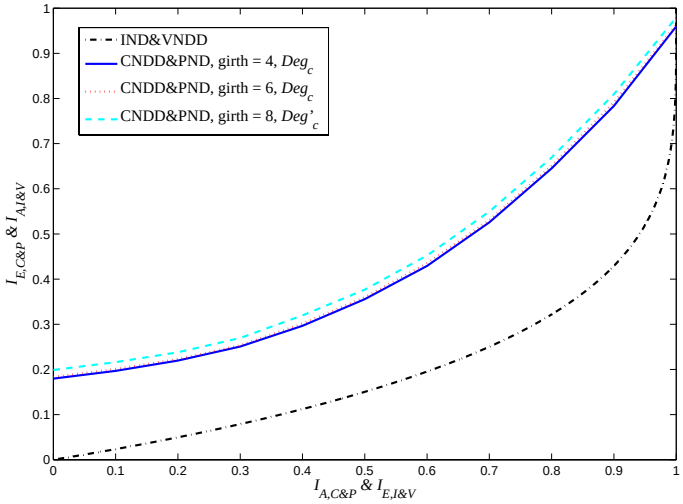


Fig. 8. EXIT chart for different schemes

C. Maximum Achievable Throughput

In order to show the theoretical threshold of JSG, we study the capacity of maximum achievable throughput. [29] and [30] have pointed out that the maximum achievable throughput in an iterative system can be expressed by the area under the EXIT curve of the inner code. In JSG, we define the area under the EXIT curve of CNDD&PND as $\mathcal{A}$, and the capacity at a E_b/N_0 is written as $\mathcal{A}(E_b/N_0)$. For comparisons, 3 scenarios of JSG-IOTA with different degree distributions and girths are presented in TABLE V, and their maximum throughputs are quantified in Fig. 9. It can be seen that, as expected, JSG-IOTA $scenario-3$ owns the highest capacity in these scenarios. Compared to the maximum achievable throughput of $scenario-3$, there are respective degradations for that of $scenario-1$ and $scenario-2$. Hence, due to the optimized degree distribution and the large girth, $scenario-3$ is the preferable scenario for JSG-IOTA, which will be further verified by performance simulations.

In addition, to quantify the gain achieved by exploiting the information of the FBMC-IOTA intrinsic interference, we investigate the capacity of JSG-IOTA $scenario-3$ excluding the low density weight matrix of the intrinsic interference,

TABLE V
JSG-IOTA SCENARIOS

Scenario	Degree distribution	Girth
$scenario-1$	Deg_a	6
$scenario-2$	Deg_b	4
$scenario-3$	Deg_c'	8

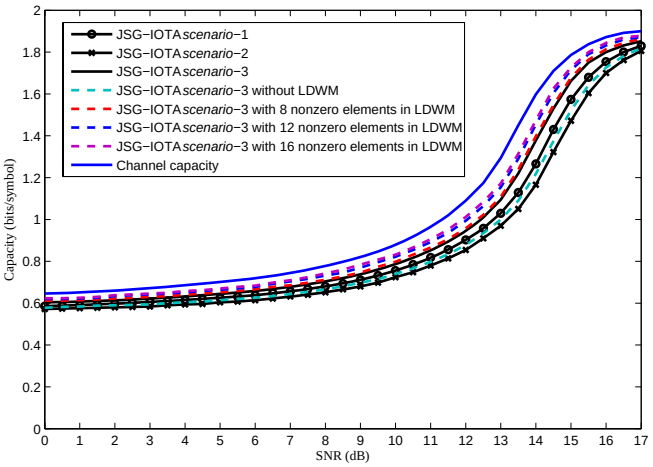


Fig. 9. Maximum effective throughput of the joint sparse graph

which is referred to as JSG-IOTA $scenario-3$ without LDWM in Fig. 9. It can be seen that, compared with JSG-IOTA $scenario-3$, there is a loss of about 0.5 dB in the medium to high SNR region in JSG-IOTA $scenario-3$ without LDWM. Therefore, the capacity of the joint sparse graph is decreased when the low density weight matrix of the intrinsic interference is not utilized. In other words, by performing MPA on LDWM, the intrinsic interference utilization can bring additional gain.

Furthermore, to find the rule to determine the number of nonzero elements in LDWM, we analyse the capacity of JSG-IOTA $scenario-3$ having different nonzero elements in the low density weight matrix of the intrinsic interference, which are referred to as JSG-IOTA $scenario-3$ with 8/12/16 nonzero elements in LDWM in Fig. 9. Five cases with different number of nonzero elements in LDWM are considered, and their details are presented in TABLE VI. According to Fig. 9 and TABLE VI, we can draw conclusions as follows.

1) When JSG-IOTA $scenario-3$ without LDWM is excluded, in the rest scenarios of TABLE VI, JSG-IOTA $scenario-3$ with 16 nonzero elements in LDWM has the highest capacity, while JSG-IOTA $scenario-3$ (note that for such a scenario, there exists 4 nonzero elements in LDWM, hence it also can be named as JSG-IOTA $scenario-3$ with 4 nonzero elements in LDWM) has the lowest capacity. Therefore, the capacity of the joint sparse graph can be increased when the number of nonzero elements in the low density weight matrix increases.

2) The curves of JSG-IOTA $scenario-3$ and JSG-IOTA $scenario-3$ with 8 nonzero elements in LDWM almost overlap, while the curves of JSG-IOTA $scenario-3$ with 12 nonzero elements in LDWM and JSG-IOTA $scenario-3$ with 16 nonzero elements in LDWM almost overlap. Hence,

TABLE VI
NONZERO ELEMENTS IN LDWM

Scenario	Number of nonzero elements	Detailed distribution of nonzero elements	Computational complexity order
$scenario-3$ without LDWM	0	No LDWM	0
$scenario-3$	4	Red elements in Fig.2 (b)	$\mathcal{O}\left(\mid \mathbb{X} \mid^4\right)$
$scenario-3$ with 8 nonzero elements in LDWM	8	Red&Blue elements in Fig.2 (b)	$\mathcal{O}\left(\mid \mathbb{X} \mid^8\right)$
$scenario-3$ with 12 nonzero elements in LDWM	12	Red&Blue&Purple elements in Fig.2 (b)	$\mathcal{O}\left(\mid \mathbb{X} \mid^{12}\right)$
$scenario-3$ with 16 nonzero elements in LDWM	16	Red&Blue&Purple&Orange elements in Fig.2 (b)	$\mathcal{O}\left(\mid \mathbb{X} \mid^{16}\right)$

compared with 4 (or 12) nonzero elements in LDWM, there is only a marginal gain when 8 (or 16) nonzero elements in LDWM are selected. However, there is obvious gap between the curves of 8 nonzero elements and 12 nonzero elements in LDWM.

3) Considering the fact that computational complexity of intrinsic interference utilization increases exponentially with the number of nonzero elements in LDWM, JSG-IOTA $scenario-3$ (with 4 nonzero elements in LDWM) strikes the best balance between performance and complexity. Although JSG-IOTA $scenario-3$ with 16 nonzero elements in LDWM has the highest capacity, its computational complexity is very high.

VI. PERFORMANCE EVALUATION

In this section, we compare JSG-IOTA with state-of-the-art techniques including OFDM, IOTA, LDS-OFDM, LDS-IOTA and turbo structured LDS-IOTA, where OFDM and IOTA represent conventional systems without LDS structure. The performances are evaluated over multipath fading channel, and the simulation parameters are presented in TABLE III. For fair comparisons, a half rate LDPC code constructed by the method of [32], is utilized by all the candidates. For OFDM-based systems (including OFDM and LDS-OFDM), we use QPSK modulation, and the length of CP is 16. For IOTA-based systems (including IOTA, LDS-IOTA, turbo structured LDS-IOTA and JSG-IOTA), we use OQPSK modulation, and the number of filter taps for each subcarrier is 5. For LDS-based systems (including LDS-OFDM and LDS-IOTA), the low density signature is constructed through EXIT charts [5]. For turbo structured LDS-IOTA, we use eight outer-inner iteration, where the turbo receiver is optimized through EXIT charts [6]. The maximum iteration number is eight for LDS-OFDM, LDS-IOTA and JSG-IOTA.

A. BER Performance

The performance of 200% loaded candidates is illustrated in Fig.10. It can be seen that LDS-OFDM and LDS-IOTA significantly outperform OFDM and IOTA, respectively. This is due to the LDS structure which can effectively eliminate the MUI and exploit the frequency diversity under overloaded conditions. Meanwhile, IOTA and LDS-IOTA respectively yield slight gain over OFDM and LDS-OFDM. Hence, compared with OFDM systems, IOTA-based systems achieve improved power efficiency (better BER performance) and spectral efficiency due to the elimination of CP. The performance advantage of IOTA will be even greater if we also consider the fact that IOTA-based systems have much lower out-of-band power radiation than OFDM systems, thus smaller guard-band is needed, leading to reduced overhead. Among all the IOTA-based systems, the BER of LDS-IOTA is higher than that of turbo structured LDS-IOTA and JSG-IOTA. Because of the inherent advantage of JSG and the effective intrinsic interference utilization, all of JSG-IOTA scenarios achieve superior performance over other systems. Due to the optimal degree distribution (Deg_c') and the long cycle (girth = 8) which are optimized by EXIT charts, JSG-IOTA $scenario-3$ respectively outperforms other candidates at BER of 10^{-6} as follows: 0.3 dB over JSG-IOTA $scenario-1$, 0.7 dB over JSG-IOTA $scenario-2$, 1.3 dB over turbo structured LDS-IOTA, 1.5 dB over LDS-IOTA, and 1.9 dB over LDS-OFDM. Moreover, JSG-IOTA $scenario-3$ without LDWM is simulated and shown a worse performance than that of JSG-IOTA $scenario-3$ (about 0.5 dB degradation at BER of 10^{-6}), verifying the effect of the intrinsic interference utilization. Furthermore, JSG-IOTA $scenario-3$ with different number of nonzero elements are evaluated, where JSG-IOTA $scenario-3$ with 16 nonzero elements in LDWM has the best performance, the BER curves of 4 (or 12) and 8 (or 16) nonzero elements in LDWM almost overlap. These results concur with EXIT charts analysis presented in Section V.

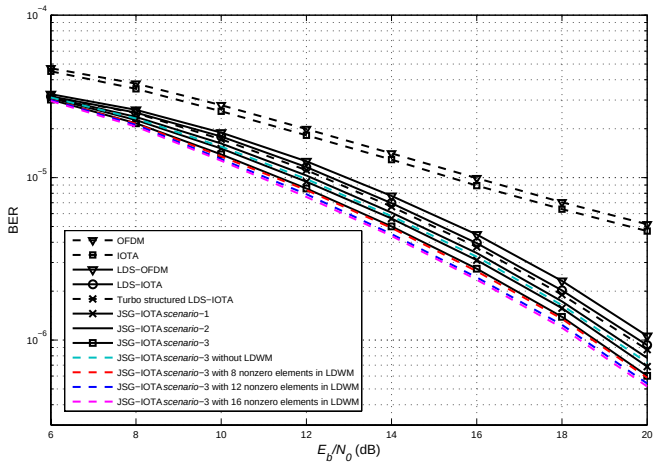


Fig. 10. Performance of different systems with 200% loading

300% loaded systems are simulated and presented in Fig.11. Similarly to the 200% loaded case, all of JSG-IOTA scenarios

still attain lower BER than other candidates. Compared with LDS-OFDM, LDS-IOTA and turbo structured LDS-IOTA, JSG-IOTA $scenario-3$ obtains 1.3 - 1.9 dB gain in the medium to high SNR region. As predicted by EXIT charts analysis, JSG-IOTA $scenario-3$ achieves a lower BER than that of JSG-IOTA $scenario-3$ without LDWM, and the performance of JSG-IOTA $scenario-3$ can be improved when the number of nonzero elements in LDWM increases.

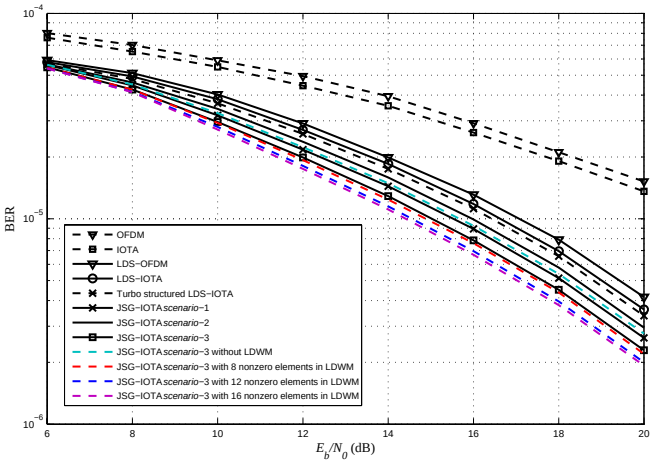


Fig. 11. Performance of different systems with 300% loading

B. Convergence Property

The convergence property of 200% loaded LDS-IOTA and JSG-IOTA $scenario-1$ at E_b/N_0 = 12 dB is shown in Fig.12, where one can see BER of the two candidates in every iteration. At the first iteration, the performance of LDS-IOTA is almost identical to that of JSG-IOTA. However, as the iterative process proceeds, BER of JSG-IOTA drops much faster than that of LDS-IOTA. After five iterations, the performance of JSG-IOTA becomes saturated, whereas LDS-IOTA needs seven iterations to reach its lowest BER. Such results concur with the trajectory prediction of the EXIT charts plotted in Fig. 6. Hence, the convergence property verifies the effectiveness of the EXIT charts.

C. Different Users' BER

In Fig.13, we show the BER of the worst and best users in LDS-IOTA and JSG-IOTA $scenario-3$ with 200% loading. We can see that some users' BER is lower than that of others, and in the low SNR region the BER degradation is less than that of high SNR region. It is related to the fact of observing the signal constellation at chip level and the primary factor of noise in the low SNR region. Thus the joint sparse graph does not give equal multiuser efficiency or in other words it does not result in the same performance for all the users. But the performance gap between the best user and the worst user in JSG-IOTA is slightly narrower than that of LDS-IOTA. More explicitly, when the joint sparse graph is applied, the variation of users performance can be reduced, meaning that a fairer and a more uniform user experience can be achieved.

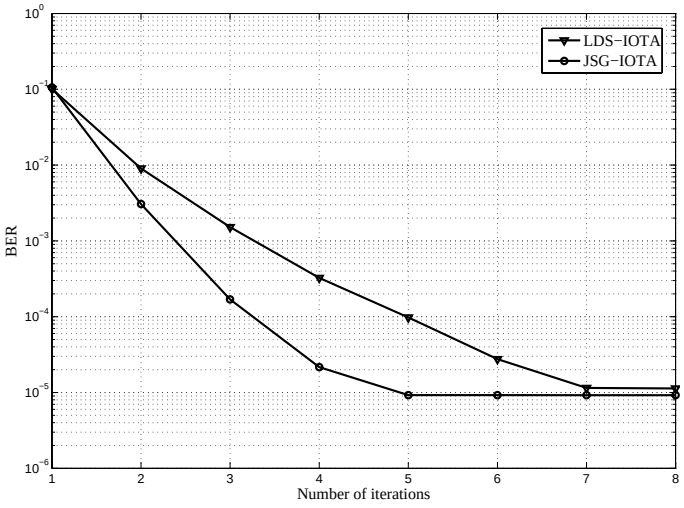


Fig. 12. Performance on different iterations at E_b/N_0 = 12 dB

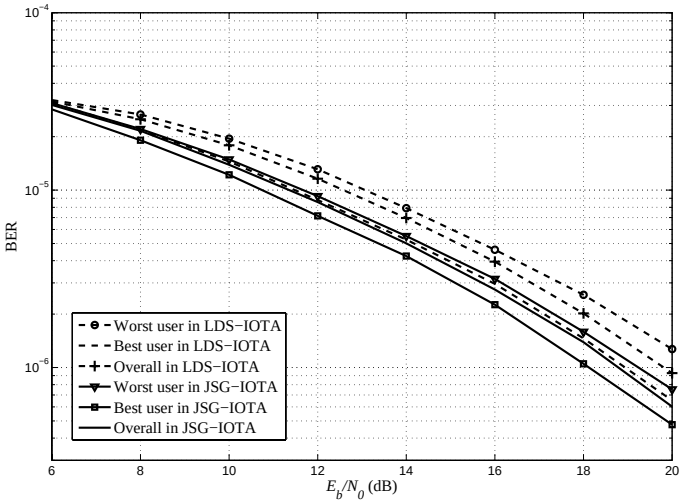


Fig. 13. Performance of different users

D. Dynamic Subcarrier Allocation

In JSG-IOTA system, the generated chips at the output of the LDS spreader are mapped to the subcarriers of the employed IOTA signal. In the simulations we have carried out so far, we assume that a static subcarrier allocation is employed, i.e., at transmitters, individual subcarriers are allocated to users for transmission without the knowledge of channel state information. However, to maximize the sum-rate with fairness consideration for JSG-IOTA, it is necessary to investigate dynamic subcarrier allocations. In other words, transmitters periodically estimate the uplink channel states of all subcarriers for each user. Based on the obtained channel state information (CSI), transmitters assign the subcarriers and power to each user through a reliable signaling channel. Fig.14 shows the effect of the subcarrier allocation in 200% loaded JSG-IOTA $scenario-3$, where the dynamic scheme allocates subcarriers to the user who has the largest channel gain [33]. As revealed by the figure, the dynamic subcarrier allocation improves the performance significantly. Compared to the static subcarrier allocation, there is about 2-3 dB gain.

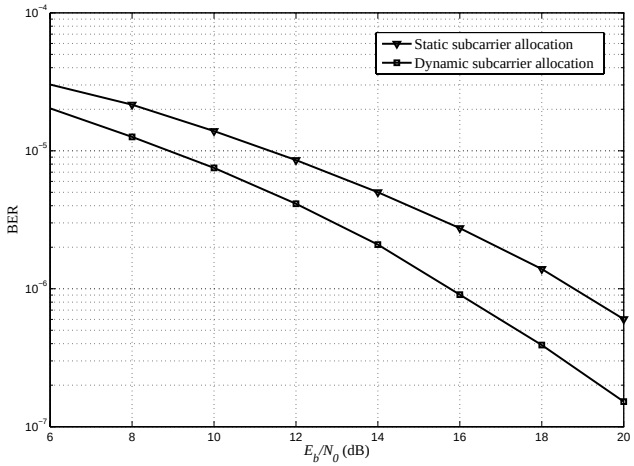


Fig. 14. Performance of different subcarrier allocation schemes

Fig.15 shows the throughput of different subcarrier allocation schemes in 200% loaded JSG-IOTA $scenario-3$. It can be observed that a higher throughput is achieved as the number of users increases. This is due to the multiuser diversity and the increase in the sum of users' power. More importantly, the results show that a larger increase is achieved by dynamic subcarrier allocation comparing to the static scheme. It should be noted that for the dynamic subcarrier allocation, CSI is required in both transmitters and receivers, while for the static subcarrier allocation, CSI is only required in receivers.

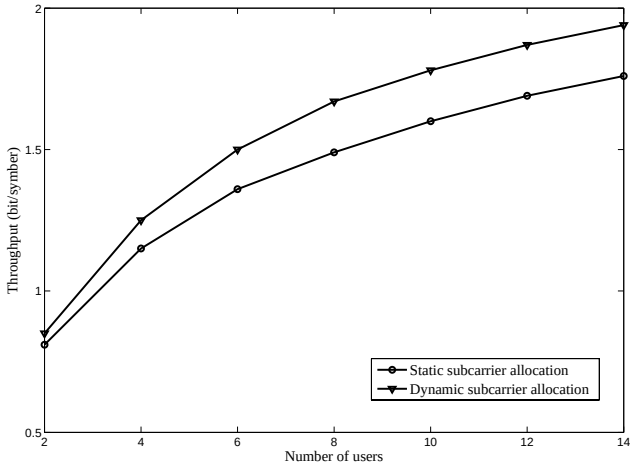


Fig. 15. Throughput of different subcarrier allocation schemes

E. Performance of the PHYDYAS Filter Based FBMC System

To show the general effect of the proposed scheme, we also adopt the PHYDYAS prototype filter to our design, and the results are presented in Fig.16. Note that the system loading is 200%, and the channel model is ITU Vehicular Channel A in the simulation. It can be seen that without the LDS structure, the PHYDYAS filter based FBMC, i.e., PHYDYAS in the figure, can not achieve a satisfactory performance under overloaded conditions. Similar to IOTA prototype filter, JSG outperforms LDS and turbo structured LDS when the PHYDYAS filter is utilized. Meanwhile, for the case of JSG, there is a performance loss if LDWM is excluded, meaning that the intrinsic interference utilization is also effective for FBMC systems with the PHYDYAS filter.

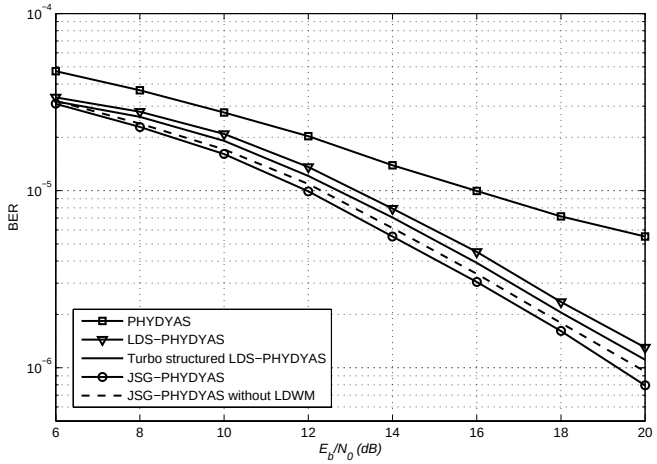


Fig. 16. Performance of PHYDYAS filter based FBMC system

VII. CONCLUSION

A joint sparse graph combing pulse shaping property (LDWM of FBMC), NOMA (LDS) and channel coding (LDPC) was proposed. Differing from single graph techniques, in the JSG-IOTA receiver, multiuser detection, intrinsic interference utilization and channel decoding are jointly conducted on JSG. By employing EXIT charts to analyse the JSG-IOTA receiver in details, the construction guidelines and the threshold of the JSG were revealed. Simulations illustrate that the JSG-IOTA $scenario-3$ can obtain the best performance, which is related to the careful design of JSG and the intrinsic interference utilization. CSI has been considered by the dynamic subcarrier allocation, and the performance of the system varies significantly. In future work, the channel effects will be considered in the filter type selection when designing JSG [22][34]. Although JSG can improve the performance, its structure is complicated and the computational complexity is high, how to design a more compact graph without information loss is a challenging topic to be explored in our future work. In addition, the joint sparse graph can be extended to MIMO scenario with beamforming and cosine-modulated multi-toned (CMT) systems.

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