High-Resolution ADCs Design in Image Sensors

Hua Fan[1], Jingxuan Yang[1], Franco Maloberti[2], Quanyuan Feng[3],
Dagang Li[4], Daqian Hu[4], Yuanjun Cen[4], and Hadi Heidari[5]
[1] State Key Laboratory of Electronic Thin Films and Integrated Devices,
University of Electronic Science and Technology of China, Chengdu, China (e-mail: fanhua7531@163.com)
[2] Department of Electrical, Computer, and Biomedical Engineering, University of Pavia 27100, Italy.
[3] School of Information Science and Technology, Southwest Jiaotong University, Chengdu 611756, China
[4] Chengdu Sino Microelectronics Technology Co.,Ltd, Chengdu, China
[5] Electronics and Nanoscale Engineering Division, School of Engineering, University of Glasgow, G12 8QQ, Glasgow, UK

Abstract—This paper presents design considerations for high-resolution and high-linearity ADCs for biomedical imaging applications. The work discusses how to improve dynamic specifications such as Spurious Free Dynamic Range (SFDR) and Signal-to-Noise-and-Distortion Ratio (SNDR) in ultra-low power and high-resolution analog-to-digital converters (ADCs) including successive approximation register (SAR) for biomedical imaging application. The results show that with broad range of mismatch error, the SFDR is enhanced by about 10 dB with the proposed performance enhancement technique, which makes it suitable for high resolution image sensors sensing systems.

Index Terms—Analog-to-Digital Converter, Successive Approximation Register(SAR) ADC, Capacitive digital-to-analog converter(DAC), Capacitor Mismatch Calibration, Image Sensing Systems.

I. INTRODUCTION

Image Sensors are increasingly becoming "Key Devices" for a broad range of products, such as medical, measuring instruments, robot vision, specialized surveillance cameras, broadcast and other industrial applications, etc, where wide dynamic range, high sensitivity, high frame rate and low noise are vital specifications to realize the best possible imaging and sensing performance. For example, CMOS image sensors can achieve over 100 dB of simultaneous-capture wide dynamic range (SCWDR) [1]. In general, development of high-resolution and wide dynamic range sensors is limited by several factors, such as vertical and horizontal readout circuit, analog to digital conversion, and data output from the sensor, then putting forward high demands on column analog-to-digital converters (ADCs), which is crucial unit to ensure sufficient vertical readout period in image sensor as shown in Fig. 1 [2], as results, high-performance ADCs have been essential for the development of highly sensitive, stable, and robust image sensor applications, furthermore, high performance image sensors often require the ADCs with on-chip capacitor mismatch calibration for the purpose of maintaining high-resolution at a very low sampling rate. Usually, precision of ADC in image sensors should be at least 12 bits, even 14-bits [2]–[4].

Charge redistribution SAR ADC consumes much less power compared with other types of ADC, in charge redistribution SAR ADC, the limited factor is mostly due to the capacitor mismatch. The resolution and its static and dynamic perfor-
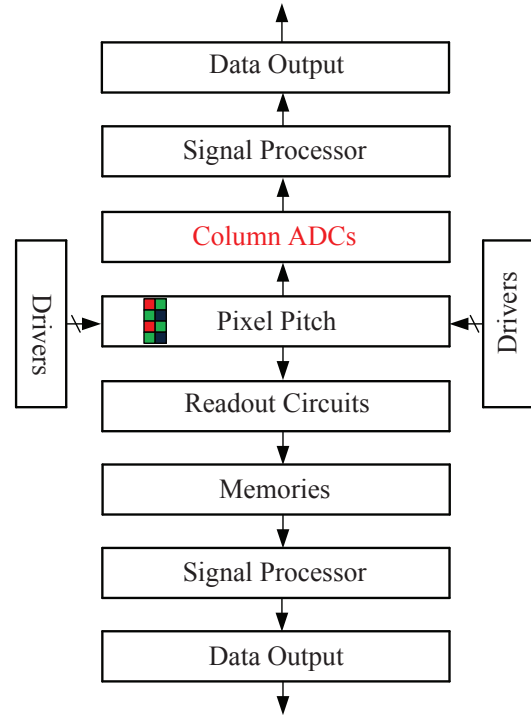

Fig. 1. Block Diagram of Image Sensor [2].

mance mostly depend on how well the match of the capacitor array. For SAR ADC, the ADC is composed of capacitors sized to produce ratios in powers of 2, or binary ratios, then errors of these ratios correspond to errors in conversion, then the largest source of the ADC error is the process variation of capacitor ratios. Several related self-calibration techniques [5] and [6] were proposed to correct capacitor ratio errors by employing additional auxiliary calibration sub-DAC for measuring and storing the capacitor matching errors into digital memory. During the subsequent conversion cycles, these data are used to correct the digital output codes digitally, since the foreground capacitor mismatch calibration is only performed during power on, no extra latency or clock cycles are introduced, but the auxiliary calibration DAC must work all the time to compensate the mismatch error of each capacitor, which consumes a lot of power. In this work, we present a modified self-calibration method that eliminates this

limitation, auxiliary DAC is only applied to measure and sort the capacitors, and does not work during the normal conversion, as a result, power can be reduced during the normal conversion. Simulation results show that with broad range of mismatch error, the SFDR is enhanced by about 10 dB and the SNDR is 5 dB better with the proposed technique for a 14-bit SAR ADC.

The remainder of this paper is organised as follows. Section II describes circuit architecture. Section III gives detailed description about the capacitor rearrangement technique proposed, then Section IV compares the performance between conventional and capacitor rearrangement technique proposed. The conclusions are finally drawn in section V.

II. SAR ARCHITECTURE

Fig. 2 shows the block diagram of the conventional 14-bit differential combined capacitor-resistor SAR ADC, binary weighted capacitive DAC is employed as DAC for 6-bit main DAC, the less significant bits are provided by a 8-bit resistor-string sub DAC.

In SAR ADC, the error of the largest capacitor will be huge compared to the small one, which is hard to predict and control, accordingly, unit element architecture may be an appropriate choice for the SAR ADC in consideration of static and dynamic linearity [7]. Here, linearity is much more important than the power consumption, for example, the power of analog front end always reaches tens of mW [8], while the power of ADC is always only an order of μW [6], [9], [10].
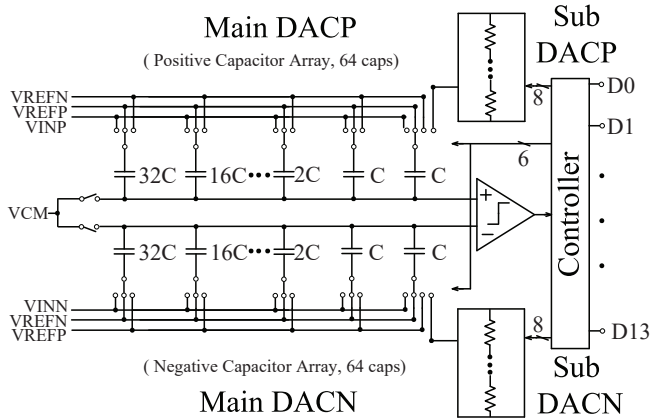

Fig. 2. A capacitor-resistor combined 14-bit SAR ADC architecture.

III. CAPACITOR REARRANGEMENT TECHNIQUE

In this section, the capacitor rearrangement technique will be discussed based on the main 6-bit capacitive DAC of capacitor-resistor combined SAR ADC in Fig. 2.

Fig. 3 shows the capacitor rearrangement technique proposed. As well known, the conventional 6-bit binary weighted charge redistribution DAC contains 64 unit capacitors, as shown in Fig. 3(a), here, unit element architecture is applied to ensure excellent static linearity, as shown in Fig. 3(b), then, measuring values of all the 64 capacitors by the measurement auxiliary DAC in Fig. 4, after measuring the values of all 64
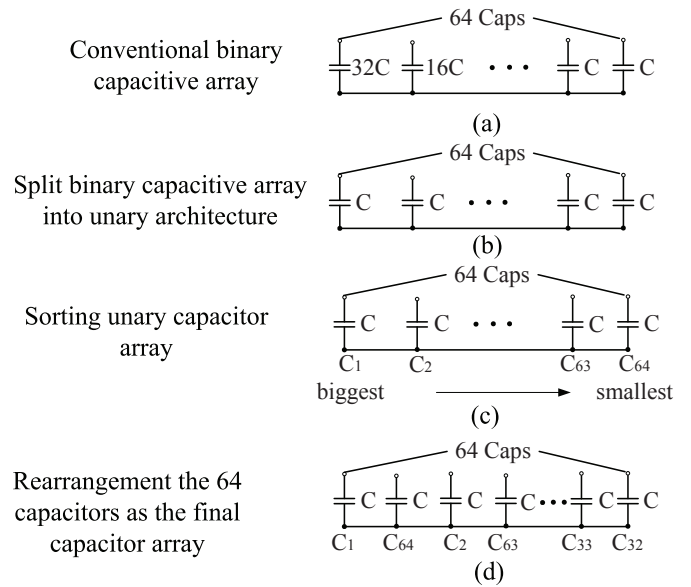

Fig. 3. (a) The conventional 6-bit binary capacitive array in Fig. 2; The proposed capacitor rearrangement method applied to the 6-bit main capacitive DAC features: (b) Split binary capacitive array into unary architecture; (c)Sorting the 64 unit capacitors; (d) Re-arranging the capacitive array as the final 6-bit capacitive array in Fig. 2.

capacitors, sorting the 64 capacitors from biggest to smallest, in Fig. 3(c), C_{64} is the smallest and the C_1 is the biggest one, then the most important point is: the 64 capacitors (from C_1 to C_{64}) are re-arranged by "one first and one last", which means the first capacitor C_1 is followed by the last capacitor C_{64}, then the third capacitor C_2 is followed by the last but one capacitor C_{63}, as shown in Fig. 3(d), finally, the re-ordered capacitors proceed with the normal binary search conversion, and the auxiliary measurement sub-DAC enters into idle mode to save power.
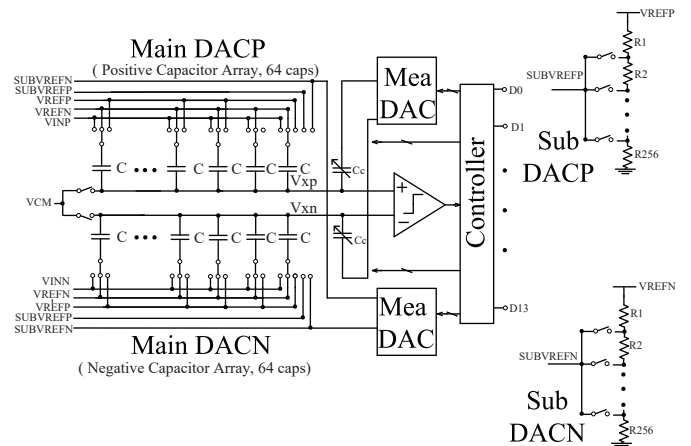

Fig. 4. A capacitor-resistor combined 14-bit SAR ADC architecture with capacitor rearrangement technique.

Finally, the block diagram of 14-bit SAR ADC with capacitor rearrangement technique is shown in Fig. 4, auxiliary sub-DAC is introduced to measure the value of each unit capacitor,
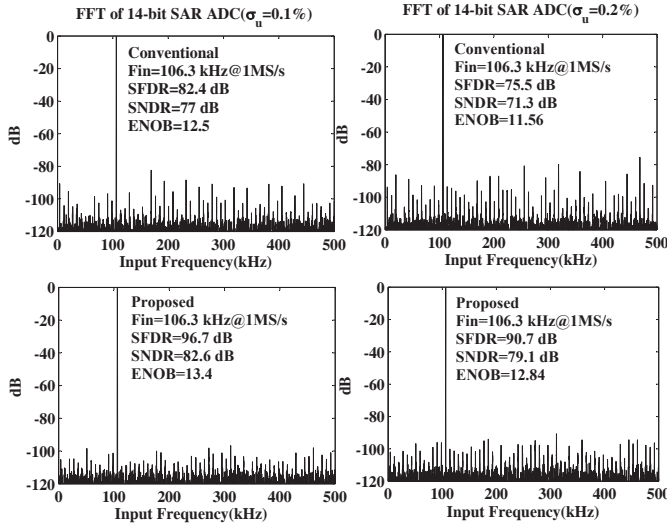
Fig. 5. FFT simulation results for 14-bit SAR ADC with respectively Conventional and rearrangement technique with σ_u=0.1% (left) and σ_u=0.2% (right).
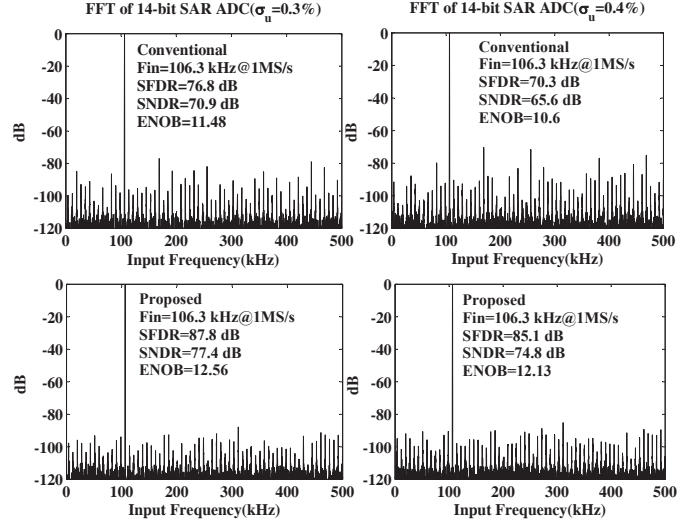

Fig. 6. FFT simulation results for 14-bit SAR ADC with respectively Conventional and rearrangement technique with σ_u=0.3% (left) and σ_u=0.4% (right).

but not works during normal conversion.

IV. SIMULATION RESULTS

To evaluate the improvement on the SFDR and SNDR of 14-bit capacitor-resistor combined ADC, a behavioral model of a capacitor-resistor combined 14-bit SAR ADC is built in Matlab. In the simulation, standard deviations of the unit capacitors of 0.1%, 0.2%, 0.3% and 0.4% are considered to cover as much diverse technologies as possible.

Fig. 5 and Fig. 6 present the power spectral density of the ADC output with/without capacitor rearrangement technique, where the input signal is a 106.3 kHz sinusoidal waveform at the full-range reference voltage. When measured at 1 MSample/s without calibration, the ADC achieves a 71.3dB SNDR and a 75.5 dB SFDR over the Nyquist bandwidth with capacitor variation of 0.2%, capacitor rearrangement technique can improve the SNDR from 71.3 dB to 79.1 dB and can improve the SFDR from 75.5 dB to 90.7 dB respectively.

Fig. 7, Fig. 8 and Fig. 9 and Fig. 10 show the SFDR and SNDR results based on two switching techniques. A total of 500 Monte Carlo simulations were performed to obtain the minimum, maximum as well as mean value of the SFDR and SNDR.

Table I and Table II conclude 500 Monte Carlo SFDR and SNDR simulation results, which show that 10 dB of improvement about SFDR and 5 dB of improvement about SNDR can be obtained in every case.

V. CONCLUSION

Capacitor mismatch calibration for SAR ADCs was proposed, simulation results show that the mean value of SNDR can be improved from 73.7 dB to 78.7 dB and the mean value of SFDR can be improved from 79.4 dB to 89.6 dB with σ_u=0.2% by using the proposed technique.
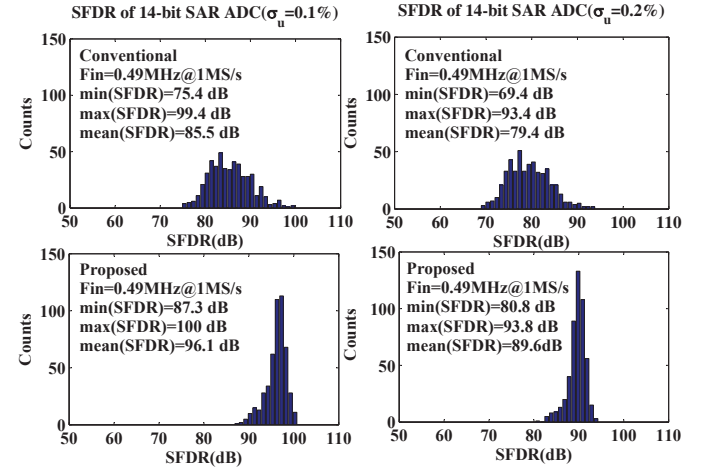

Fig. 7. 500 Monte Carlo SFDR simulation results for 14-bit SAR ADC with respectively Conventional and capacitor rearrangement with σ_u=0.1% (left) and σ_u=0.2% (right)

TABLE I
500 MONTE CARLO SFDR SIMULATION SUMMARY

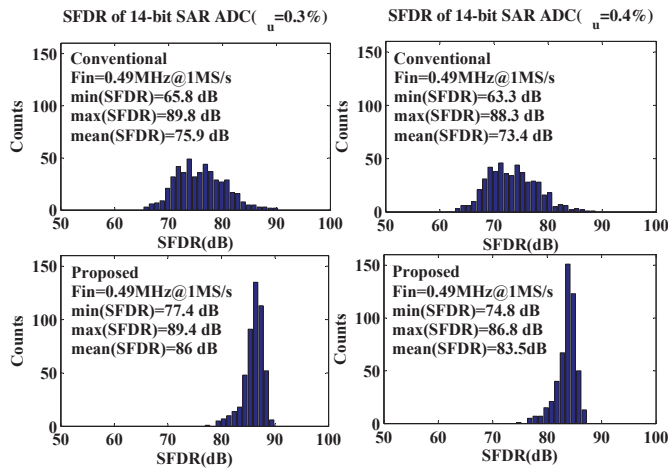|	Conventional (dB)	Proposed (dB)	Improvement (dB)
mean(SFDR)(σ_u=0.1%)	85.5	96.1	10.6
mean(SFDR)(σ_u=0.2%)	79.4	89.6	10.2
mean(SFDR)(σ_u=0.3%)	75.9	86	10.1
mean(SFDR)(σ_u=0.4%)	73.4	83.5	10.1

Fig. 8. 500 Monte Carlo SFDR simulation results for 14-bit SAR ADC with respectively Conventional and capacitor rearrangement with σ_u=0.3% (left) and σ_u=0.4% (right)
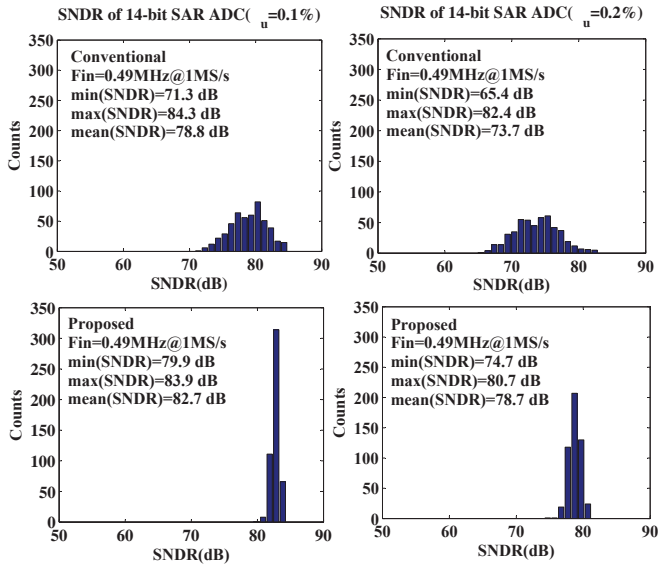

Fig. 9. 500 Monte Carlo SNDR simulation results for 14-bit SAR ADC with respectively Conventional and capacitor rearrangement with σ_u=0.1% (left) and σ_u=0.2% (right)
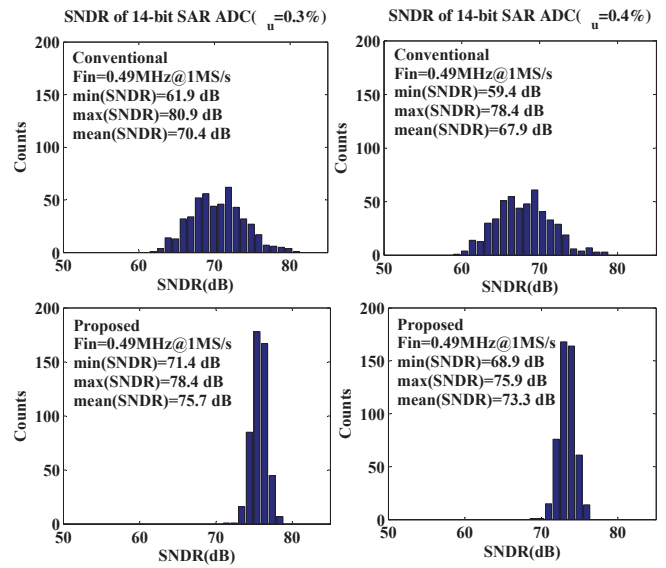

Fig. 10. 500 Monte Carlo SNDR simulation results for 14-bit SAR ADC with respectively Conventional and capacitor rearrangement with σ_u=0.3% (left) and σ_u=0.4% (right)

TABLE II
500 MONTE CARLO SNDR SIMULATION SUMMARY

	Conventional (dB)	Proposed (dB)	Improvement (dB)
mean(SNDR)(σ_u=0.1%)	78.8	82.7	3.9
mean(SNDR)(σ_u=0.2%)	73.7	78.7	5
mean(SNDR)(σ_u=0.3%)	70.4	75.7	5.3
mean(SNDR)(σ_u=0.4%)	67.9	73.3	5.4

REFERENCES

[1] K. Nishimura, Y. Sato, J. Hirase, R. Sakaida, M. Yanagida, T. Tamaki, M. Takase, H. Kanehara, M. Murakami, and Y. Inoue, "An over 120dB simultaneous-capture wide-dynamic-range 1.6 e-Ultra-Low-Reset-Noise Organic-Photoconductive-Film CMOS Image Sensor," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2016, pp. 110–111.

[2] H. Totsuka, T. Tsuboi, T. Muto, D. Yoshida, Y. Matsuno, M. Ohmura, H. Takahashi, K. Sakurai, T. Ichikawa, H. Yuzurihara *et al.*, "An APS-H-Size 250Mpixel CMOS image sensor using column single-slope ADCs with dual-gain amplifiers," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, 2016, pp. 116–117.

[3] Y.-R. Jo, S.-K. Hong, and O.-K. Kwon, "A Tileable CMOS X-Ray Line Detector Using Time-Delay-Integration With Pseudomultisampling for Large-Sized Dental X-Ray Imaging Systems," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 211–216, 2017.

[4] C. Y.-P. Chao, H. Tu, T. Wu, K.-Y. Chou, S.-F. Yeh, and F.-L. Hsueh, "CMOS Image Sensor Random Telegraph Noise Time Constant Extrac-tion From Correlated To Uncorrelated Double Sampling," *IEEE Journal of the Electron Devices Society*, vol. 5, no. 1, pp. 79–89, 2017.

[5] H. Fan, H. Heidari, F. Maloberti, D. Li, D. Hu and Y. Cen, "High resolution and linearity enhanced SAR ADC for wearable sensing systems," IEEE Int. Symp. Circuits and Systems (ISCAS), 2017, pp. 1-4

[6] A. T. Nguyen, J. Xu, and Z. Yang, "A 14-bit 0.17 mm^2 SAR ADC in 0.13μm CMOS for high precision nerve recording," *IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 1–4, 2015.

[7] H. Khorramabadi, "∼EE 247 Analysis and Design of VL-SI Analog Digital Interface Integrated Circuits lecture notes," *http://inst.eecs.berkeley.edu/ ee247/fa07/lectures.html*, 2009.

[8] ADI, "Low power, five electrode electrocardiogram (ECG) analog front end," *ANALOG DEVICES ADAS1000 DATASHEET*, 2012.

[9] J.-Y. Lin and C.-C. Hsieh, "A 0.3 V 10-bit 1.17 f SAR ADC With Merge and Split Switching in 90 nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 1, pp. 70–79, 2015.

[10] Z. Chen, Y. Jiang, C. Cai, H.-G. Wei, S.-W. Sin, U. Seng-Pan, Z. Wang, and R. P. Martins, "A 22.4 μW 80dB SNDR $\Sigma\Delta$ modulator with passive analog adder and SAR quantizer for EMG application," in *IEEE Asian Solid State Circuits Conference (A-SSCC)*, 2012, pp. 257–260.