Z^2-FET as capacitor-less eDRAM cell for high density integration

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***Abstract*—2D numerical simulations are used to demonstrate the Z^2-FET as a competitive embedded capacitor-less DRAM cell for low-power applications. Experimental results in 28 nm FD-SOI technology are used to validate the simulations prior to downscaling tests. Default scaling, without any structure optimization, and enhanced scaling scenarios are considered before comparing the bit cell area consumption and integration density with other eDRAM cells in the literature.**

***Keywords*—1T-DRAM, capacitor-less, DRAM, embedded, Fully depleted, integration, low-power, scaling, SOI and Z^2-FET.**

I. Introduction

Capacitor-less solutions are being currently considered as a potential technology to implement dynamic memory (DRAM) blocks in embedded low-power applications for the IoT [1]. The significant advantage over the conventional DRAM design is the absence of the charge-storage capacitor (1T-DRAM), that makes compatible the co-integration with other CMOS circuit elements, resulting in cost effective manufacturing. Although quite a few contenders have been reported for capacitor-less DRAM design, three solutions can be highlighted: the A2RAM [2], the MSDRAM [3] and the Z^2-FET [4], which have their own pros and cons. The main benefits of favoring the Z^2-FET over the others are performance, CMOS compatible fabrication and possibility of using ultra-thin bodies (UTB) without suffering from the supercoupling effect [6].

In this work, we investigate with advanced 2D numerical simulations the potential for channel length scalability of Z^2-FET operated as a single-transistor DRAM cell. Experimental results are used to validate the simulated curves in long devices (400 nm). Once the simulation deck reproduces the experimental data, the Z^2-FET dimensions are reduced while monitoring the performance of the memory cell to assess competitive integration for future nodes.

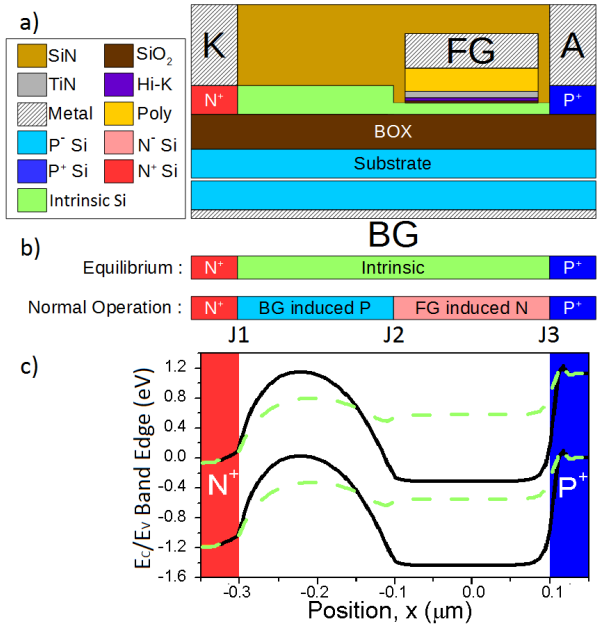

Fig. 1. a) N-type Z^2-FET basic structure. b) Effective doping in *Si* active region at equilibrium ($V_{FG} = V_{BG} = V_A = V_K = 0$ V) and in normal operation ($V_{FG} > 0$ V and $V_{BG} < 0$ V with $V_A = V_K = 0$ V). c) Energy bands diagram at equilibrium (N^+-I-P^+ diode, dashed line) and in normal memory operation (virtual N^+-P-N-P^+, solid line).

II. Z^2-FET DRAM operation

The Z^2-FET N^+-I-P^+ structure in equilibrium conditions is depicted in Fig. 1a (same potential in all terminals). The body is split into two different regions: the one with the gate stack above (L_G), driven by the front-gate terminal, and the gateless region (L_{In}), influenced by the back-gate. In order to operate the device as a memory, the gate terminals are biased with $V_{FG} > 0$ V and $V_{BG} < 0$ V to induce a complementary energy barrier, i.e. a P-N junction, at the boundary between the gated and ungated sections of the body [4], [5]. As a result, the device ends up as a N^+-P-N-P^+ structure emulating a Shockley diode [7] with three homo-junctions (J1-3), Fig. 1b,c.

The memory operation is possible thanks to a transient depletion of carriers that shifts V_{ON} (onset of the anode

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2016 REMINDER project (grant agreement No 687931) is thanked for financial support.

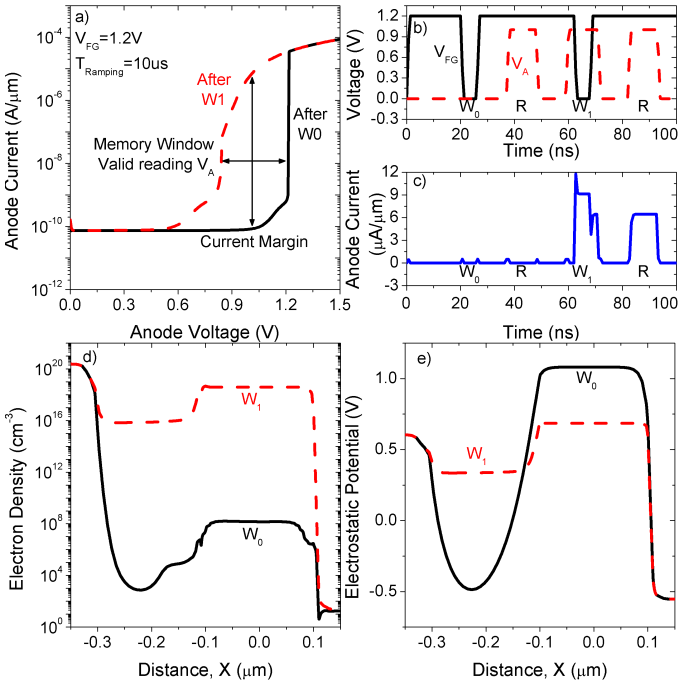

Fig. 2. a) Simulated $I_A(V_A)$ curves after programming both states. b) Fast bias pattern and c) anode readout current for a W_0-R-W_1-R-W_0-R memory operation applied to the default 200+200 nm Z^2-FET device. d) Horizontal electron density profile and e) potential along the front-channel (1 nm away from top-interface) after programming the '1'- (W_1, dashed line) and '0'-states (W_0, solid line). $V_{BG} = -1$ V and $V_K = 0$ V.

current) to larger biases, Fig. 2a. The range in-between the curves yields the memory window and current margin.

A fast bias pattern and readout current are showed in Fig. 2b-c to exemplify the memory behavior. The memory states are defined based on the carrier concentration within the body. If the electron density is high when V_A is pulsed, all three junctions J1-3 (Fig. 1b) are forward biased, the barriers collapse and the conductance hugely increases; this is the '1'-state. On the other hand, if the carrier concentration is reduced, energy barriers grow as in the deep depletion regime for a MOS capacitor [8], and the injection when reading is not enough to reduce the barriers [4], [5]. The conductivity then remains low, '0'-state, Fig. 2d-e.

In order to program the '1'-state (W_1), the front-gate is grounded while the anode is pulsed, Fig. 2b. The goal is to increase the population of both type of carriers along the body. Once the gate returns to a positive voltage, the carrier densities are high inside the device. The '0'-state is programmed (W_0) by evacuating the electrons thanks to capacitive coupling (by pulsing the front-gate and grounding the anode).

III. Simulation Setup and Experimental Comparison

The initial Z^2-FET 2D structure was built using Synopsys TCAD [9] in 28 nm FD (Fully Depleted) SOI technology [10] following the architecture of available experimental samples. The structure features a symmetric overall 400 nm

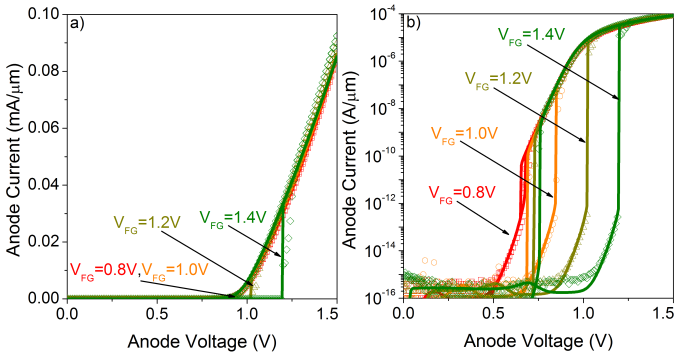

Fig. 3. Comparison of experimental data (symbols) with 2D simulations (solid lines). $I_A(V_A)$ hysteresis curves in a) linear and b) log scale for several front-gate voltages. V_A is swept from 0 to 1.5 V and way back (triangular shape) with a 24.16 s ramp time for several front-gate voltages. $L_G = L_{In} = 200$ nm, $V_K = 0$ V and $V_{BG} = -1$ V.

structure length (200 nm gated, L_G, and ungated, L_{In} regions). All devices are N-type (top gate beside the anode terminal) and feature the following characteristics: low-doped Boron body ($N_{SOI} = 10^{16}$ cm^{-3}), P-type ground-plane (GP, $N_{Sub} \approx 10^{18}$ cm^{-3}), highly-doped Boron anode (A) and Arsenic cathode (K) regions ($N_{A/K} > 10^{20}$ cm^{-3}). The original thickness of *Si*-film is 7 nm thickness with a 15 nm epitaxy that completes the ungated and A/K regions. The buried oxide (BOX) is 25 nm thick and a 0.5 μm substrate, acting as the GP, lies below. The top gate insulator is composed by a *SiO_2/HfON* multi-layer of around 3 nm, followed by a *TiN* metal-gate stack. The front and back-gate workfunctions are close to mid-gap. Finally, a *SiN* layer encapsulates the whole device.

The electrical models and parameters accounted during the simulations are: room temperature (300 K), Fermi-Dirac statistics, band-to-band tunneling [11], SRH generation/recombination, surface recombination and interfacial charge layer in between the top insulator layers *SiO_2/HfON*. Due to the thin *Si*-film, quantum corrections were included based on the density gradient quantization [9], simultaneously with Schenk band-gap narrowing model [12] to account for doping and carrier concentrations impact [9]. Regarding the mobility models, default transversal field dependence (with remote Coulomb scattering), high-field saturation, carrier-carrier scattering and the *thinlayer* (for the inversion and accumulation layer mobility, *IALmob*) models [9] were used.

The anode voltage was swept in forward and backward directions to evaluate the hysteresis loop. The access resistance ($R_A = R_K = 400\ \Omega \cdot \mu$m) and the carrier lifetimes (*taumax* in Synopsys [9], $2.5 \cdot 10^{-8}$ s for electrons and 10^{-8} s for holes) were tuned to obtain similar maximum anode current and hysteresis loop as in the experimental curves. The comparison is illustrated in Fig. 3 in a) linear and b) log scale for several V_{FG}. The simulations (solid lines) match the experimental results (symbols) for every bias considered.

IV. Z^2-FET Scaling

Different technological, geometrical parameters and operation conditions affect the scaling of this device when operated

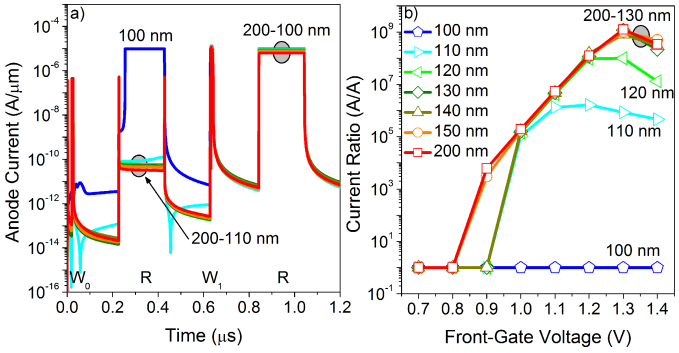

Fig. 4. a) Current readout at $V_{FG} = 1$ V for a W_0 ($V_A = 1$ V and $V_{FG} = 0$ V), R ($V_A = 1$ V and $V_{FG} = 1$ V), W_1 ($V_A = V_{FG} = 0$ V), R bias pattern. b) Current ratio (I_1/I_0) for different lengths. $V_K = 0$ V and $V_{BG} = -1$ V. Programming and reading last 5 ns and 200 ns, respectively.

as a memory cell: i) biasing conditions (V_{FG}, V_A and V_{BG}) ii) thicknesses of the semiconductor and dielectric layers (t_{Si}, t_{Epi}, t_{Ox} and t_{BOX}), iii) doping profiles, iv) carriers lifetime and v) operating speed (access and programming times)...

As shown by Wan et al [13], the Z^2-FET can be successfully shrunk down to very short channels, while still keeping excellent memory operation. With the goal of reducing the costs and time to market we focus on the Z^2-FET DRAM cell scaling using *standard* 28 FD SOI technology [10] (no layer thickness or doping profiles are modified).

A. Symmetric scaling

In this first attempt, the gate and intrinsic regions are concomitantly scaled, starting from $L_G = L_{In} = 200$ nm. A W_0-R-W_1-R bias pattern is employed to test the Z^2-FET memory capabilities. Figure 4a shows adequate memory operation (different '0'- and '1'-state current levels) down to $L_G = L_{In} = 110$ nm. For $L_G = L_{In} = 100$ nm, the '0'-state is corrupted (equals the '1'-state current) and the memory operation fails. The current ratio (I_1/I_0) is illustrated in Fig. 4b as a function of the reading/holding front-gate voltage. No improvement is observed for $L_G = L_{In} \geq 130$ nm where the curves merge together. As the device is scaled down, the minimum front-gate voltage inducing memory operation rises. Larger voltages compensate the short-channel effects (SCE), that gradually reduce the V_{FG}-induced J3 energy barrier height. For very large V_{FG} the effect is opposite, the anode voltage is not high enough to completely forward bias J3 and the '1'-state current decays. At the same time, the current ratio drops since the '0'-state current increases and resembles more and more the stationary '1'-state. Notice that faster reading operations accentuate the non-equilibrium condition improving the scaling.

B. Asymmetric scaling

The condition $L_G = L_{In}$ is relaxed. Figure 5a-b shows the current ratio extracted for some asymmetric architectures using the same pattern as in the previous section. There is no significant reduction in the current ratio when shortening L_G beyond 110 nm for a fixed L_{In}. Hence, the gateless region turns out to be the major inconvenient limiting the Z^2-FET density integration. Intrinsic lengths below 110 nm present the same challenge as in the symmetric scaling (Fig. 4b). The gated region can be reduced down to at least 60 nm. For $L_G = 50$ nm, the current ratio collapses for $V_{FG} = 1$ V, but remains reasonable for $V_{FG} = 1.1$ V, Fig. 5b.

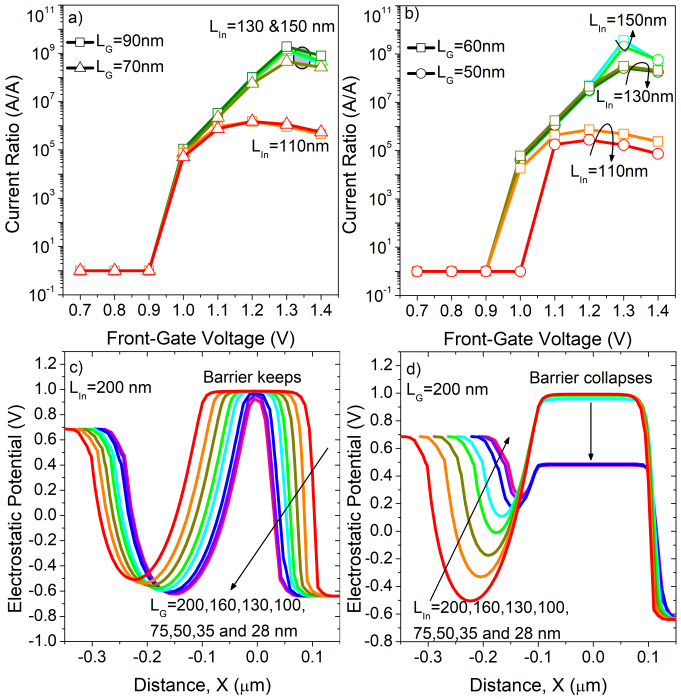

Fig. 5. a-b) Current ratio (I_1/I_0) against V_{FG} for different gate and intrinsic regions lengths. Simulated horizontal mid-channel potential when scaling c) the gate length or the d) intrinsic ungated region for 200, 160, 130, 100, 75, 50, 35 and 28 nm. $V_{FG} = 1$ V, $V_{BG} = -1$ V and $V_A = V_K = 0$ V.

Figure 5c-d clarifies the reasons why the ungated region scaling threatens the memory operation. Reducing the length of the front-gate does not significantly modify the hole injection from the anode, the barrier height is preserved, Fig. 5c. On the contrary, shortening the ungated region leads to the rapid collapse of the electron injection barrier, followed by that of holes, Fig. 5d. SCE impact more the ungated region simply due to the poorer electrostatic control, thicker back oxide and *Si*-film, with respect to the gated region.

C. Anode and GP bias tuning

A deeper scaling can be achieved by adapting the biasing conditions. The idea is to reinforce the energy barriers such as to counteract the influence of the lateral SCE. A higher V_{FG} implies a higher V_A, meaning an increase in the power consumption. A trade-off is necessary since some parameters restrict the scaling of the gated portion of the body, e.g. the back-gate bias that counterbalances the V_{FG} effect.

Figure 6a-b demonstrates how it is possible to reduce L_G down to 28 nm without suffering much degradation by adjusting simultaneously the anode and front-gate bias. On the

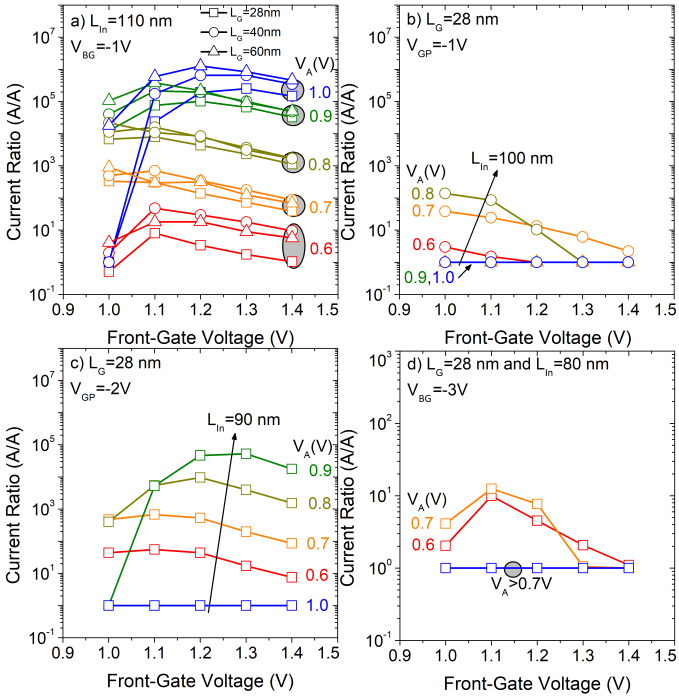

Fig. 6. Simulated current ratios for a) $L_{In} = 110$ nm, b) $L_G/L_{In} = 28/100$ nm, c) $L_G/L_{In} = 28/90$ nm and d) $L_G/L_{In} = 28/80$ nm with different GP bias. $V_K = 0$ V.

other hand, L_{In} is limited to 100 nm. This happens also for $L_G = 40$ or 60 nm. A more negative GP bias is required to keep the ungated region potential barrier and continue the scaling. $L_{In} = 90$ nm is possible with V_{BG} to -2 V (Fig. 6c) and $L_{In} = 80$ nm with -3 V (Fig. 6d), yet the current ratio significantly drops. Notice that the current ratio only exceeds 1 for a certain range of V_{FG}. Very high/low gate voltages always/never block the Z^2-FET, thus the current during the '0'- and '1'-states get equal.

The Z^2-FET can be further scaled down by modifying the architecture [13] (not *standard* 28 FD-SOI technology anymore). By thinning the SOI and the BOX layers and by increasing the body doping, the cell maintains the memory operation down to $L_G/L_{In} = 28/28$ nm, Fig. 7a. However, metrics such as the retention time or current levels are affected, Fig. 7b. Nonetheless, these cells might suit certain applications where ultra-high density is required and very high access rates will be used (no need for very long retention times).

Table I summarizes the Z^2-FET minimum size when optimized for the current ratio (larger than 10). The no scaling scenario, initial 400 nm long Z^2-FET, at default biasing conditions is used to normalize the figures of merit.

D. Retention time

Another important figure of merit is the retention time. Figure 8 shows the normalized retention time for some of the previously scaled Z^2-FETs. The retention is extracted as the time it takes the unstable '0'-state to swap into the stationary

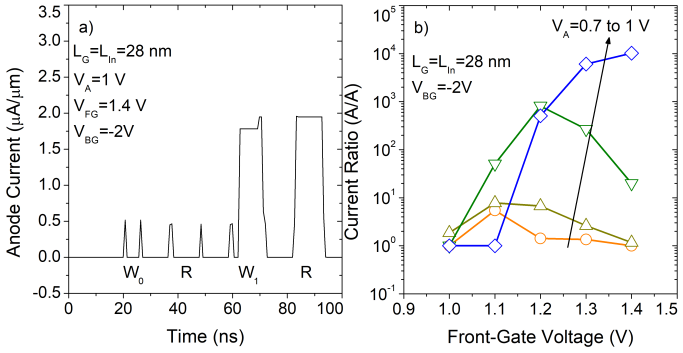

Fig. 7. a) Memory operation and b) current ratio of Z^2-FET cell scaled beyond 28 FD-SOI technology: $t_{Si} = 4.8$ nm, $t_{BOX} = 15$ nm, $N_{In} = 10^{17}$ cm^{-3} and no silicon epitaxy. $V_K = 0$ V.

TABLE I. Z^2-FET SCALING SUMMARY OPTIMIZED FOR THE CURRENT RATIO. BOLD NUMBERS INDICATE THE REFERENCE BIAS.

Scenario	L_G (nm)	L_{In} (nm)	I_1/I_0 (-)	t_{Ret} (-)	V_{FG} (V)	V_A (V)	V_{BG} (V)
No scaling	200	200	1.00	1.00	**1.0**	**1.0**	**-1.0**
Symmetric	110	110	1.2e+4	0.33	1.2	**1.0**	**-1.0**
Asymmetric	60	110	8.03	0.17	1.2	**1.0**	**-1.0**
Bias tuning	28	100	8.7e-4	0.06	1.0	0.8	**-1.0**
GP tuning	28	80	7.9e-5	0.05	1.1	0.7	-3.0

TABLE II. Z^2-FET SCALING SUMMARY OPTIMIZED FOR THE RETENTION TIME. BOLD NUMBERS SHOW THE REFERENCE BIAS.

Scenario	L_G (nm)	L_{In} (nm)	I_1/I_0 (-)	t_{Ret} (-)	V_{FG} (V)	V_A (V)	V_{BG} (V)
No scaling	200	200	1.00	1.00	**1.0**	**1.0**	**-1.0**
Symmetric	110	110	1.2e+4	0.33	1.2	**1.0**	**-1.0**
Asymmetric	60	110	8.03	0.17	1.2	**1.0**	**-1.0**
Bias tuning	28	100	2.4e-4	0.15	1.0	0.7	**-1.0**
GP tuning	28	80	6.0e-5	0.06	1.0	0.7	-2.0

'1'-state due to parasitic injection of carriers from anode and cathode, thermal and SRH generation. The retention is obtained during a continuous reading operation, the worst case featuring the larger leakage due to the reduction in the anode-channel barrier with the applied reading V_A. Lower anode voltages satisfying $V_A < V_{FG}$ tend to provide larger retention times since the injection of carriers from the lateral terminal is better controlled and the Z^2-FET triggering is delayed. Table II shows the scaling limits when the Z^2-FET cell is optimized for the retention time.

Scaling the cell improves the density integration at the expense of the memory performance (retention and current ratio) as shown in Tables I and II. The minimum length will be then defined by the minimum size satisfying both the minimum retention time and current levels within the maximum allowed tolerance while ensuring an adequate operation.

V. EDRAM DENSITY INTEGRATION COMPARISON

Since the reading operation involves exclusively the drain bias (V_{FG} remains unchanged), a selector is added to each Z^2-FET memory bit cell to avoid sneak currents. A minimum-size transistor may play the role as wordline (WL) but it negatively impacts the maximum density integration due to the bit cell

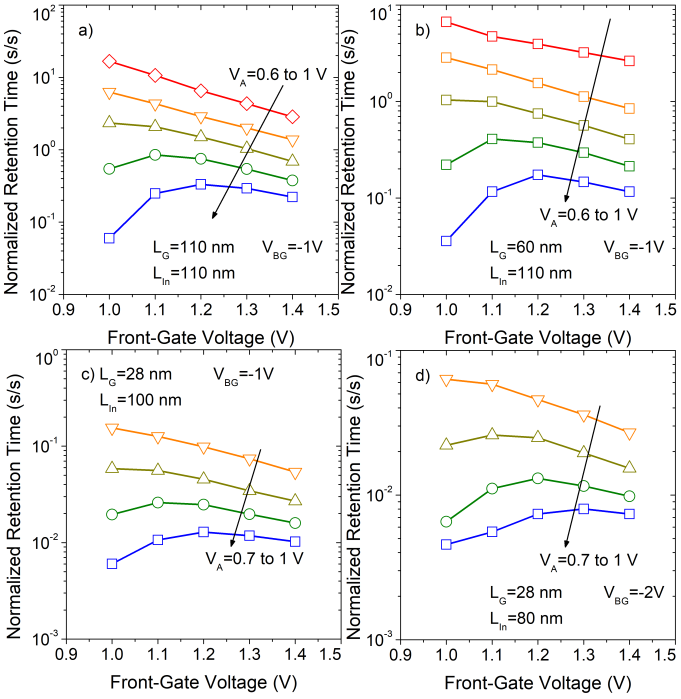

Fig. 8. Simulated retention time for scaled Z^2-FETs: a) $L_G/L_{In} = 110/110$ nm, b) $L_G/L_{In} = 60/110$ nm, c) $L_G/L_{In} = 28/100$ nm and d) $L_G/L_{In} = 28/80$ nm. $V_K = 0$ V.

area increase. Together with the selector, extra circuitry is required to sense and discriminate the memory states. eDRAM peripheral circuitry typically consumes around 50% (overhead surface percentage, A_{Over}) of the total available surface [14]. Figure 9 shows a) a simplified layout and b) electric diagram of a 2x2 Z^2-FET memory matrix. To simplify the study, the separations between the Z^2-FET and other elements, bitline (BL), select line (SL) or the selector transistor (WL), are considered to be equal, S. The Z^2-FET bit cell area is thus given by Eq. 1.

$$A_{bit} = (W + 2 \cdot S) \cdot (L_G + L_{In} + L_S + 3 \cdot S) \quad (1)$$

with L_S being the selector transistor length. The density integration in Mb/mm^2 for any memory cell can be expressed as Eq. 2 (with A_{bit} given in mm^2).

$$D_{mm^2} = (1 - A_{Over}/100) \cdot (A_{bit} \cdot 1024^2)^{-1} \quad (2)$$

Figure 10 depicts the a) bit cell area and b) density integration estimations for the Z^2-FET as 1T-DRAM. The bit cell area grows linearly with $L_G + L_{In}$ while the final integration density exhibits a more complex behavior strongly affected by the overhead consumption. A bit cell area of 0.083 μm^2 is found for a 400 nm long Z^2-FET ($L_S = 28$ nm, $W = 100$ nm and $S = 30$ nm) leading to a 5.75 Mb/mm^2 density ($A_{Over} = 50\%$).

In order to be competitive and have similar densities with respect to other 1T+1C eDRAM designs, Table III, the Z^2-FET

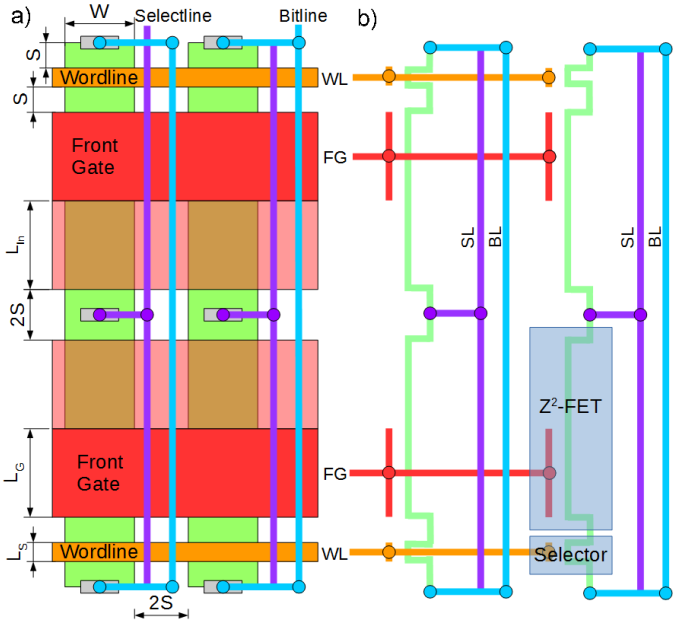

Fig. 9. Simplified diagram of a) possible layout and b) electrical connections for a 2x2 symmetric Z^2-FET memory matrix. Identical spacing between elements, S, is considered. Green colour: active silicon region; solid red: Z^2-FET front-gate; light red: intrinsic Z^2-FET region; orange: selector device front-gate acting as wordline; purple: select line; light blue: bitline.

TABLE III. SUB-40 NM NODE EDRAM. $A_{Over} = 50\%$ BY DEFAULT.

-	Technology	Node	A_{bit} (μm^2)	D_{mm^2} (Mb/mm^2)	A_{Over} (%)
Intel	Bulk Tri-Gate	22 [14]	0.029	17.50	46.8
TSMC	Bulk Planar	28 [15]	0.035	13.62	50.0
		20 [15]	0.021	22.71	50.0
IBM	SOI Planar	32 [16]	0.039	12.22	50.0
		22 [17]	0.026	18.34	50.0

TABLE IV. Z^2-FET INTEGRATION SUMMARY. $W = 100$ NM, $L_S = 28$ NM, $S = 30$ NM AND $A_{Over} = 50\%$.

Scenario	L_G (nm)	L_{In} (nm)	A_{bit} (μm^2)	A_{ratio} [15] (-)	D_{mm^2} (Mb/mm^2)
No scaling	200	200	0.083	2.37	5.75
Symmetric	110	110	0.054	1.54	8.82
Asymmetric	60	110	0.046	1.31	10.35
Bias tuning	28	100	0.039	1.12	11.64
GP tuning	28	80	0.036	1.02	13.18
Advanced	28	28	0.028	0.79	17.12

overall length needs to be below 200 nm while $S \leq 40$ nm. The density rapidly worsens if S increases. Without scaling, the Z^2-FET bit cell is almost 2.4 times larger than typical eDRAM for the same technological node [15], table IV. By symmetrically scaling the devices without any structure enhancement, the bit cell area ratio decreases to 1.5. On the other hand, asymmetrically scaling the ungated region with respect to the front-gate reduces the ratio down to 1.3. Finally, by adjusting the biasing conditions and the GP, the ratio can be lowered to 1.1 and 1, respectively. All these values can be further improved by narrowing the width beyond 100 nm.

If one selector is shared for each wordline, A_{bit} is given by:

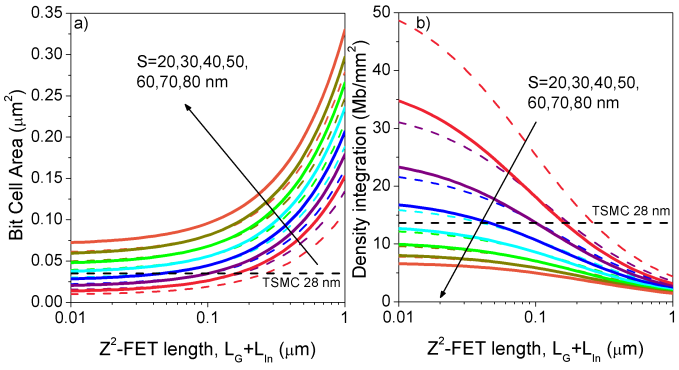

Fig. 10. a) Z^2-FET bit cell area consumption and b) maximum density integration for different values of S as a function of the Z^2-FET overall length ($L_G + L_{In}$). $W = 100$ nm (thick solid lines) and $W = 60$ nm (thinner dashed lines). Horizontal dashed line corresponds to the TSMC 28 nm eDRAM cell [15]. $L_S = 28$ nm and $A_{Over} = 50$ %.

$$A_{bit} = (W + 2 \cdot S) \cdot (L_G + L_{In} + 2 \cdot S) \quad (3)$$

This scenario represents a boost of around 22% area reduction at same conditions. In such case, the bias optimized cell with $W = 100$ nm would feature 0.031 μm^2 and a ratio of 0.9. In any case, even if choosing a Z^2-FET size presenting lower density integration, the reduced processing cost, low power and simplicity may motivate the use of the Z^2-FET as eDRAM.

VI. Conclusion

Z^2-FET experimental data is used to perform 2D-TCAD simulations and analyze the device integration as eDRAM. Symmetric structures are too long and prevent the cell to be competitive at same technology node. Shortening the gate length independently becomes the simpler way to approach the same density integration. Enhancing the architecture or tuning the biasing potentially enables similar or higher capacity compared to other cells in the literature, over 15 Mb/mm^2, maintaining simultaneously the advantages of 1T-DRAM cells.

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