Investigation of Inversion, Accumulation and Junctionless mode Bulk Germanium FinFETs

Vasanthan Thirunavukkarasu [a,b,c], Jaehyun Lee [b], Toufik Sadi [b], Vihar P. Georgiev [b], Fikru-Adamu Lema [b], Karuppasamy Pandian Soundarapandian [b], Yi-Ruei Jhan [a], Shang-Yi Yang [a], Yu-Ru Lin [a], Erry Dwi Kurniawan [a,b], Yung-Chun Wu [a,*] and Asen Asenov [c,d]

[a] Department of Engineering and System Science, National Tsing Hua University, Hsinchu 300, Taiwan
[b] Nano Science and Technology Program, Taiwan International Graduate Program, Academia Sinica, Taipei 115, Taiwan and National Tsing Hua University, Hsinchu 300, Taiwan
[c] Device Modeling Group, School of Engineering, University of Glasgow, Glasgow, Scotland, UK
[d] Gold standard Simulations Ltd. (now part of Synopsys), Glasgow G3 7JT, Scotland, UK

Abstract—The characteristic performance of n-type and p-type inversion (IM) mode, accumulation (AC) mode and junctionless (JL) mode, bulk Germanium FinFET device with 3-nm gate length (L_G) are demonstrated by using 3-D quantum transport device simulation. The simulated bulk Ge FinFET device exhibits favorable short channel characteristics, including drain-induced barrier lowering (DIBL<10mV/V), sub threshold slope (SS~64mV/dec.). Electron density distributions in ON-state and OFF-state also show that the simulated devices have large I_{ON}/I_{OFF} ratios. Homogenous source/drain doping is maintained and only the channel doping is varied among different operating modes. Also, a constant threshold voltage $|V_{TH}|$~0.31V is maintained. Moreover, the calculated quantum capacitance (C_Q) values of the Ge nanowire emphasizes the importance of quantum confinement effects (QCE) on the performance of the ultra-scaled devices.

***Keywords*— Germanium, junctionless, FinFETs, 3D TCAD simulation, quantum confinement effects.**

[*] **Corresponding author**:

Prof. Yung-Chun Wu
Department of Engineering and System Science, National Tsing Hua University, 101, section 2 Kuang Fu Road, Hsinchu 30013, Taiwan.
TEL: +886-3-5715131 ext. 34287 FAX: +866-3-5720724
E-mail: ycwu@ess.nthu.edu.tw
Mailing address:
R408 ESS Building, National Tsing Hua University, 101, section 2 Kuang Fu Road, Hsinchu 30013, Taiwan.

1. Introduction

Germanium promises to keep Moore's law alive even in sub-10nm Technology and is considered as a promising candidate to mitigate the constraints that arise in such ultra-scaled devices [1-2]. Whilst ultra-scaled Silicon based devices are demonstrated both theoretically and experimentally, [3-4] drive current (I_{DSAT}) saturation and degraded performances of bulk Si CMOSFET limits the prospects of further scaling. Ge offers various advantages over its counterpart Si such as higher injection velocity, higher mobility, higher density-of-states and higher drive current, low contact resistance with metals, low processing temperature for process integration and smaller gate delay [5-9]. Especially when device dimensions shrink below sub 10-nm nodes, the device performances are heavily influenced by quantum confinement effects. In particular, the band diagram, valley-splitting in different sub-bands, charge distribution in different valleys, charge density occupied in the lowest sub-bands, density of states and effective mass are highly dependent on type of material used in the channel and the gate electrostatics. Germanium will be more advantageous than Si in sub-10nm device nodes. Hence various research groups are focusing on gate dielectrics, metal gates for Ge, surface passivation in Ge MOSFET and integration of Ge with Si. Such Ge transistors with admirable electrical characteristics were demonstrated by many research groups in the past [10-12]. In this work, we analyzed the performance of scaled Germanium FinFETs and compared their device characteristics with a 3-nm bulk Silicon FinFET with similar device dimensions [13]. As Germanium is a potential material, this paper tries to explore the transport properties and the effect of quantum confinement on performance of Ge-based transistors. In this work, we for the first time report the charge distribution in different sub-bands of Ge devices. We have compared Si and Ge device density of states and band structure too. Junctionless (JL) devices with homogenous source drain doping will be the preferred mode of operation in ultra-scaled logic devices due to the various advantages such as reduced scattering and simpler device fabrication processes [14-17]. Thus we comprehensively analyzed the JL mode of operation which will serve as a benchmark for future scaled device dimensions.

2. Simulation Approach

2.1 Device Structure

Fig. 1 shows the structure of the simulated device. We applied oxide thickness (EOT) of 0.3 nm. A nano-fin structure (L_G =F_W=F_H=3 nm) with gate length (L_G), fin width (F_W) and fin height (F_H) of 3-nm is used. A constant source/drain doping concentration of $1.0x10^{20}$ cm^{-3} is used in all modes of device operation. The channel concentration of JL and IM FinFET is set to $1.0x10^{20}cm^{-3}$ and $1.0x10^{18}$ cm^{-3} respectively. The Bulk doping concentration used for the device simulation is $5x10^{18}cm^{-3}$. A work function value of 4.40eV is used for IM and JL NFETs; whereas, AC NFETs are simulated with work function 4.41eV. In case of p-type IM and AC modes, work function used is 4.37eV; whereas, p-type JL mode is simulated with a work function of 4.33eV.

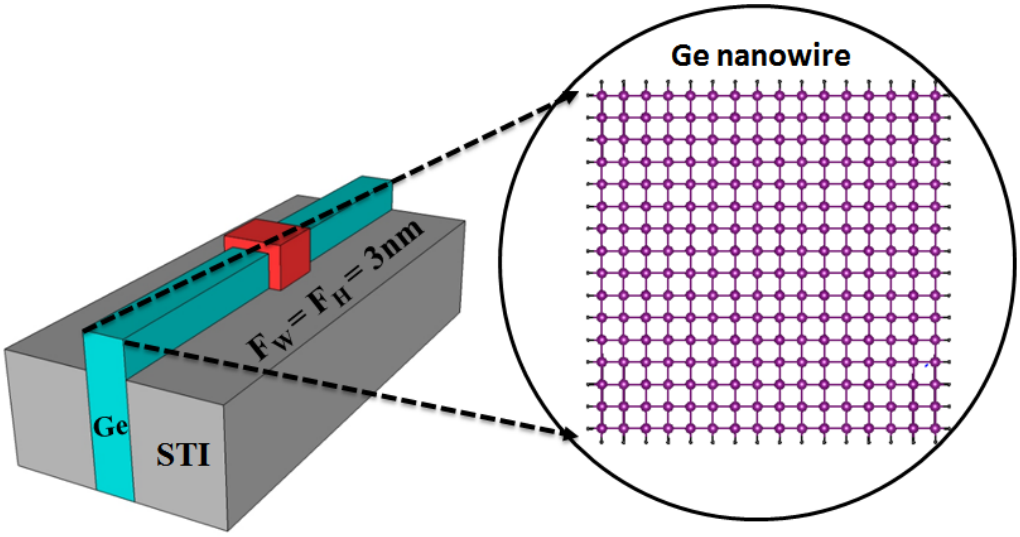

Fig. 1. Simulated IM, AC & JL mode Germanium Bulk FinFET device with 3-nm nano-fin structure (L_G=F_W=F_H=3nm).

2.2 Simulation Model

We have used the Atomistix Toolkit software packages [18-20] that uses density functional theory (DFT) to investigate electrical properties of hydrogen-passivated Si and Ge nanowires. The generalized gradient approximation (GGA) proposed by Perdew, Burke, and Ernzerhof (PBE) was adopted for exchanged and correlation functional [21]. The double-ζ singly polarized (DZP) pseudo atomic orbital basis set generated by the Fritz-Haber Institute (FHI), and 75 Ha of cutoff energy for electron density are used. All atoms are fully relaxed until maximum force of any atoms becomes less than 0.05 eV/Å. With optimized atomic structures of Si and Ge nanowire, we calculated quantum capacitance using [22];

$$C_Q = \frac{e^2}{4kT}\int g(E)sech^2\frac{E-E_F}{2kT}dE \qquad (1)$$

where *k*, *e*, *T*, *g(E),* and E_F are Boltzmann constant, elementary charge, temperature, density-of-states (DOS) and Fermi-level energy, respectively. For DOS calculations, we have applied 51×1×1 Monkhorst-Pack k-grids.

The device characteristics are obtained by solving 3D quantum transport equations provided by robust Synopsys Sentaurus tool. To include quantization effects, a potential-like quantity Λ_n (electrons) and Λ_p (holes) are introduced in density calculation.

$$p = Nv\, F1/2\left(\frac{E_{F,p} - Ev - \Lambda_p}{k\,Tp}\right) \quad (2)$$

$$n = Nc\, F1/2\left(\frac{Ev - E_{F,n} - \Lambda_n}{k\,Tn}\right) \quad (3)$$

n and p are the electron and hole concentrations respectively; N_v and N_c are the effective density of states of valence band E_v and conduction band E_c respectively; Fermi–Dirac integral is given by $F_{1/2}$; T_n and T_p denotes electron temperature and hole temperature respectively;

$$\Lambda_p = -\frac{\gamma\hbar^2}{12m_p}\left[\nabla^2 ln\, p + \frac{1}{2}(\nabla ln\, p)^2\right] \quad (4)$$

$$\Lambda_n = \frac{\gamma\hbar^2}{12m_n}\left[\nabla^2 ln\, n + \frac{1}{2}(\nabla ln\, n)^2\right] \quad (5)$$

This quantum device simulation considers other models such as, the band-gap narrowing model, S–R–H recombination with doping dependent models and band-to-band tunneling (BTBT) model [17, 23]. In ultra-scaled Ge FinFETs, quantum confinement effects (QCE) results in band gap widening and mitigates the BTBT leakage; doping is optimized to prevent source-drain tunneling in our structure [24-26]. The Mathiessen's mobility model accounts for the mobility calculated in the device simulation. Furthermore details are available in [17, 23].

3. Results and Discussion

As shown in Fig. 2, the effect of confinement on charge dynamics, can be studied using Eigen functions of the first four sub bands in Ge nanowire which is accurately captured using multi-sub band Monte Carlo solver solving a 3D Poisson - 2D Schrödinger equations [27, 28]. Edges are the boundaries of the semiconductor and oxide. Wave-function is very small in sub-bands of Γ (Gamma) valley. The L and X valleys, (especially lowest sub bands 1 and 2) contribute largely with physically significant wave-function and others sub bands are depleted of carriers. Energetically, from sub-bands, the lowest valleys provide large contribution to the overall electron transport [29]. We clearly see that there is a coupling in Y-Z directions of the L and X valleys which induces the alignment of the Eigen-states diagonally along the 3-D channel cross-section.

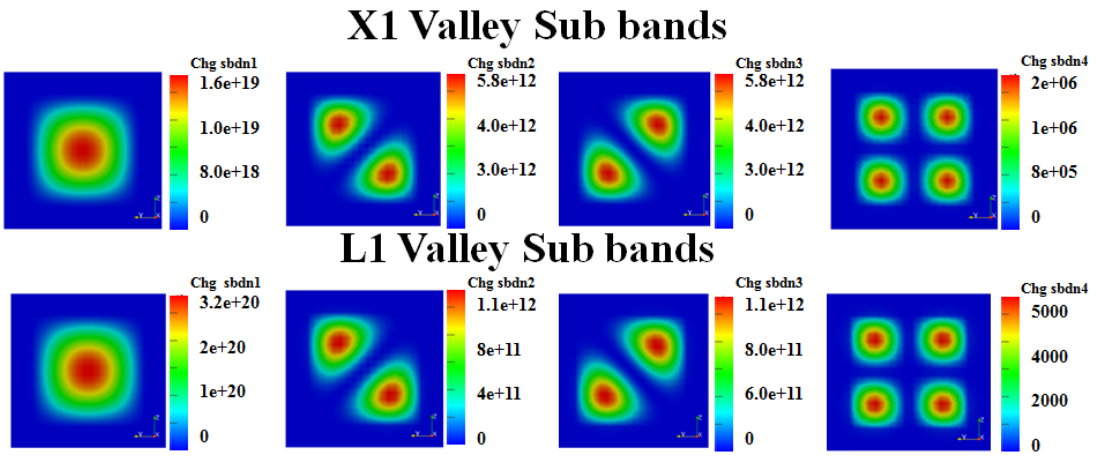

Fig. 2. Eigen functions of the first four sub bands in Ge nanowire with a diameter of 3-nm.

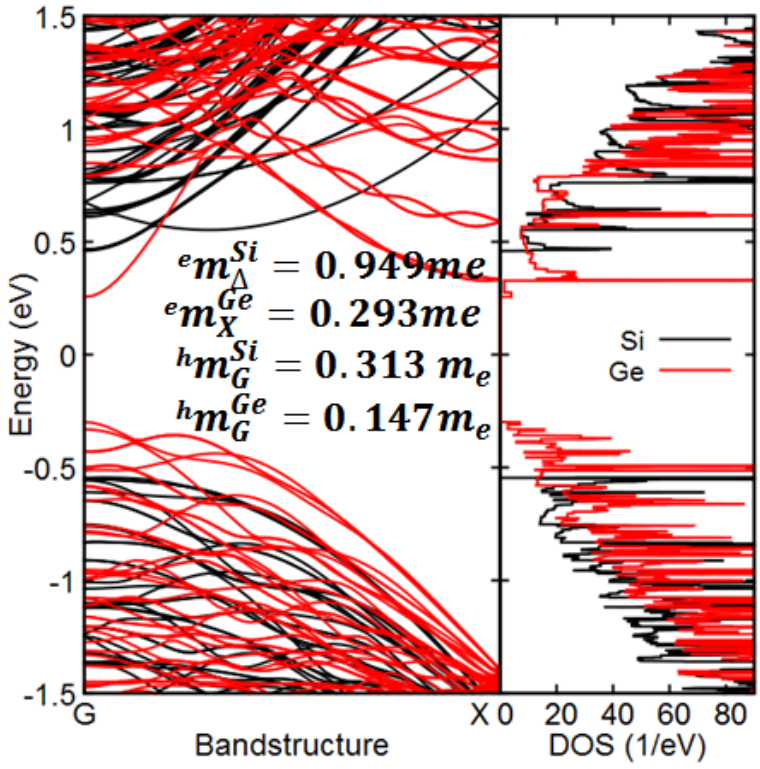

Fig. 3. Band structure and density-of-states of the hydrogen passivated Si and Ge nanowire structures calculated based on DFT GGA method with the effective mass values shown in the inset.

Fig. 3 shows the band structure and DOS of the simulated 3nm Ge and Si nanowire calculated by DFT-GGA method. Quantum capacitance (C_Q) is proportional to DOS. When the Fermi-level is at the conduction-band-edge (CBE), at 300K, the CQ for a highly doped Si and Ge nanowire is around 3.8748 fF/μm and 1.6552 fF/μm respectively. Clearly, the C_Q of Ge is lower than Si. The extracted effective mass in Ge is $^{h}m_{G}^{Ge}$=0.147m_e. Germanium has smaller effective mass than Silicon. Thus for scaled devices, in QC limit, depending on operating conditions, performance of Ge and Si devices are comparable.

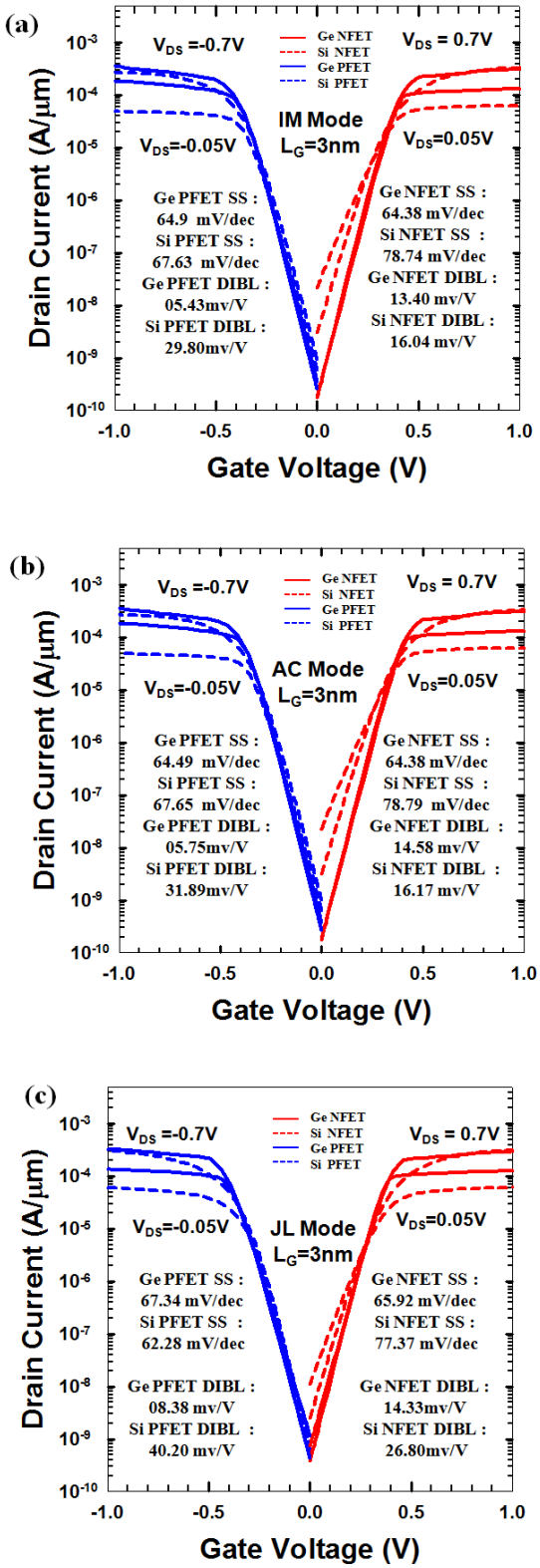

Fig. 4. I_D-V_G of the Ge Bulk FinFET operating in (a) IM, (b) AC & (c) JL modes; with SS and DIBL values shown inset.

Fig. 4 shows the transfer characteristics of the simulated Ge FinFETs. The I_{SAT} of Ge PFET is around 3.3×10^{-4} A/μm. The ISAT of Si PFET is around 2.8×10^{-4} A/μm. Fig.

4(a) and Fig.4(b), shows that IM & AC mode have similar characteristics. The IM PFET DIBL value is ~5X times higher for Si compared to Ge. The effective gate length in JL device is larger than the physical gate length. Hence as shown in Fig. 4(c) the I_D-V_G of Ge JL NFET achieves almost ideal SS value of 65.92 mV/dec. and Si JL NFET has SS value of 77.37 mV/dec. The DIBL value of Ge JL PFET and Si JL PFET are 8.38mV/V and 40.20mV/V, resp. which proves that JL devices have better immunity to short channel effects (SCE). By using optimum doping, SCE can be tuned [24]. It is noteworthy, that off-state current is low owing to the scaled nano-fin. The ultra-scaled nano-fin provides good electrostatic controllability of gate intrinsically which improves device characteristics.

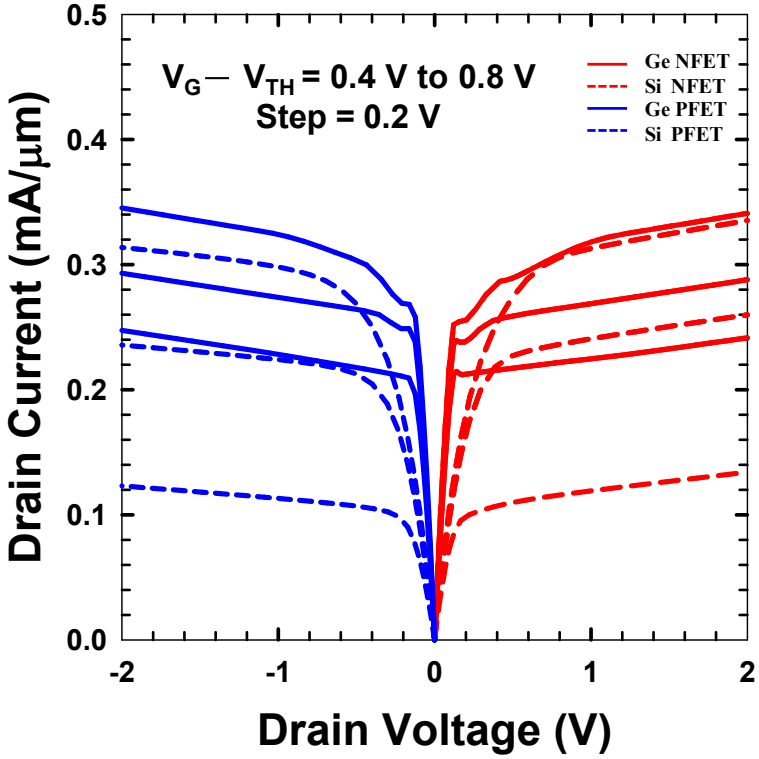

Fig. 5. I_D-V_D output characteristics curves of the Ge Bulk FinFET operating in JL mode; inset with overdrive voltage (V_{OV}), $|V_{OV}| = |V_G - V_{TH}|$.

Fig. 5 shows the I_D-V_D output characteristics curves of Ge PFET operating in junctionless mode. Owing to the light hole effective mass (${}^{h}m_G^{Ge}$=0.147m_e) the quantum capacitance (C_Q) is low in Ge devices compare to Si devices, which in turn degrades gate to channel capacitance (as $C_G \cong C_Q$, in QC limit). We are currently investigating the influence of quantum confinement on scattering in Ge devices with more sophisticated simulation tools, in detail for possible future communication.

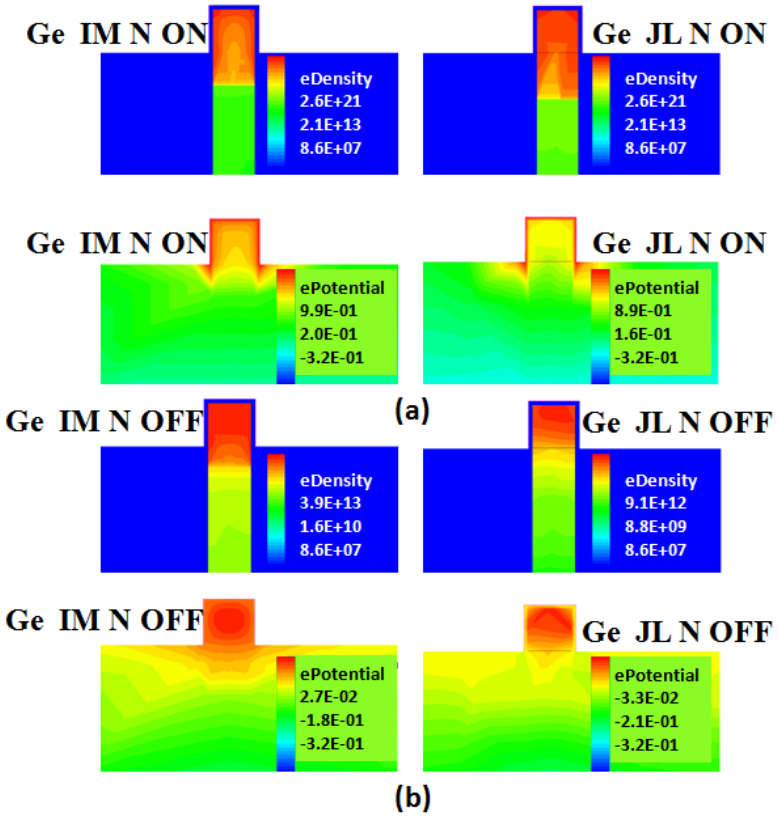

Fig. 6. Electric field distributions (bottom) and electron density distributions (top) of the n-type IM and JL devices along the 3-D channel cross-section when the devices operate in (a) on state (V_{GS} = 0.7V) and (b) off state (V_{GS}=0V).

Fig. 6 compares electrostatic potential and electron density distribution along the nano-fin channel cross-section in Ge IM & JL NFETs. The charge transport path is localized within the fin cross-section and does not penetrate the substrate, thus leakage path can be shut off [30]. Fig. 6(a) & Fig. 6(b), shows n-type Ge Bulk FinFET on-state (V_{GS}=0.7V) and off-state (V_{GS}=0V) electric field distribution respectively; the charge carriers occupy the nano-fin cross-section fully; hence, the current conduction path is almost similar in IM and JL devices.

4. Conclusion

In conclusion, we analyzed, the performance of Ge FinFETs with 3-nm gate length in JL, IM and AC modes. Ge devices have comparable device characteristics to that of Si. However, smaller effective mass of Germanium results in degradation of quantum capacitance. The observed transfer, output characteristics iterates the fact that quantum confinement effects will play a vital role in determining the performance of ultra-scaled Ge logic devices.

Acknowledgement

The authors would like to thank the Ministry of Science and Technology, Taiwan, for supporting this research (MOST 103-2221-E-007-114-MY3). The Taiwan National

Center for High-performance Computing (NCHC) is greatly appreciated for its TCAD simulation support. The authors would like to thank Professor Jean-Pierre Colinge for sharing his profound knowledge on junctionless transistors and his suggestions that helped us to improve this work immensely.

References

[1] C. Hu, “Device Challenges and Opportunities,” in VLSI Symp. Tech. Dig., pp. 4-5, Jun. 2004. doi: 10.1109/VLSIT.2004.1345359.

[2] K. Suzuki, K Ikeda, Y. Yamashita, M. Harada, N. Taoka, O. Kiso, T. Yamamoto, N. Sugiyama, S. Takagi, "Ion-Implanted Impurity Profiles in Ge Substrates and Amorphous Layer Thickness Formed by Ion Implantation," in Electron Devices, IEEE Transactions on , vol.56, no.4, pp.627-633, April 2009. doi: 10.1109/TED.2009.2014193

[3] S. Migita, Y. Morita, M. Masahara, H. Ota, “Fabrication and Demonstration of 3-nm-Channel-Length Junctionless Field-Effect Transistors on Silicon-on-Insulator Substrates Using Anisotropic Wet Etching and Lateral Diffusion of Dopants “in Jpn. J. Appl. Phys., 52 pp.04CA01-01 - 04CA01-5, Feb. 2013. doi: 10.7567/JJAP.52.04CA01.

[4] V. Thirunavukkarasu, Y. R. Jhan, Y. B. Liu, E. D. Kurniawan, Y. R. Lin, S. Y. Yang, C. H. Cheng, Y. C. Wu, "Gate-all-around junctionless silicon transistors with atomically thin nanosheet channel (0.65 nm) and record sub-threshold slope (43 mV/dec)" in Applied Physics Letters, vol. 110, no.3, pp. 032101-1 - 032101-5, Jan. 2017. doi: 10.1063/1.4974255.

[5] P. Bhatt, and K. Chaudhuri, S. Kothari, A. Nainani, and S. Lodha, "Germanium oxynitride gate interlayer dielectric formed on Ge(100) using decoupled plasma nitridation", Applied Physics Letters, 103, pp.172107-1 - 172107-5 , Oct. 2013. doi:10.1063/1.4826142.

[6] T. Low, Y. T. Hou, M. F. Li, Chunxiang Zhu, D. L. Kwong and A. Chin, "Germanium MOS: an evaluation from carrier quantization and tunneling current," Symposium on VLSI Technology. Digest of Technical Papers, Kyoto, Japan, 2003, pp. 117-118. doi: 10.1109/VLSIT.2003.1221113.

[7] V. P. H. Hu, M. L. Fan; P. Su, C. T. Chuang, "Comparative Leakage Analysis of GeOI FinFET and Ge Bulk FinFET," in Electron Devices, IEEE Transactions on , vol.60, no.10, pp.3596-3600, Oct. 2013. doi: 10.1109/TED.2013.2278032.

[8] W. Choi, J. Lee and M. Shin, "p-Type Nanowire Schottky Barrier MOSFETs: Comparative Study of Ge- and Si-Channel Devices," in IEEE Transactions on Electron Devices, vol. 61, no. 1, pp. 37-43, Jan. 2014. doi: 10.1109/TED.2013.2292008.

[9] J. Lee and M. Shin, "Simulation Study of Germanium p-Type Nanowire Schottky Barrier MOSFETs," in IEEE Electron Device Letters, vol. 34, no. 3, pp. 342-344, March 2013. doi: 10.1109/LED.2012.2237375.

[10] V. P. H. Hu, Y. S. Wu and P. Su, "Investigation of Electrostatic Integrity for Ultrathin-Body Germanium-On-Nothing MOSFET," in IEEE Transactions on Nanotechnology, vol. 10, no. 2, pp. 325-330, March 2011. doi: 10.1109/TNANO.2010.2041010.

[11] K. H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken and K. De Meyer, "Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFETs," in IEEE Transactions on Electron Devices, vol. 59, no. 2, pp. 292-301, Feb. 2012. doi: 10.1109/TED.2011.2175228.

[12] I. H. Wong, Y. T. Chen, S. H. Huang, W. H. Tu, Y. S. Chen and C. W. Liu, "Junctionless Gate-All-Around pFETs Using In-situ Boron-Doped Ge Channel on Si," in IEEE Transactions on Nanotechnology, vol. 14, no. 5, pp. 878-882, Sept. 2015. doi: 10.1109/TNANO.2015.2456182.

[13] V. Thirunavukkarasu, Y. R. Jhan, Y. B. Liu and Y. C. Wu, "Performance of Inversion, Accumulation, and Junctionless Mode n-Type and p-Type Bulk Silicon FinFETs With 3-nm Gate Length," in IEEE Electron Device Letters, vol. 36, no. 7, pp. 645-647, July 2015. doi:10.1109/LED.2015.2433303.

[14] Kanchan Cecil, Jawar Singh, Influence of Germanium source on dopingless tunnel-FET for improved analog/RF performance, Superlattices and Microstructures, Volume 101, January 2017, Pages 244-252, ISSN 0749-6036, https://doi.org/10.1016/j.spmi.2016.11.039.

[15] D. Gracia, D. Nirmal, A. Nisha Justeena, Investigation of Ge based double gate dual metal tunnel FET novel architecture using various hetero dielectric materials, Superlattices and Microstructures, Available online 26 April 2017, ISSN 0749-6036, https://doi.org/10.1016/j.spmi.2017.04.045.

[16] Avik Chattopadhyay, Abhijit Mallik, Yasuhisa Omura, Device optimization and scaling properties of a gate-on-germanium source tunnel field-effect transistor, Superlattices and Microstructures, Volume 82, June 2015, Pages 415-429, ISSN 0749-6036, https://doi.org/10.1016/j.spmi.2015.02.022.

[17] C. Sahu and J. Singh, "Potential Benefits and Sensitivity Analysis of Dopingless Transistor for Low Power Applications," in IEEE Transactions on Electron Devices, vol. 62, no. 3, pp. 729-735, March 2015. doi: 10.1109/TED.2015.2389900.

[18] Atomistix ToolKit v.2016.3 Quantumwise, [online] Available: http://quantumwise.com/.

[19] M. Brandbyge, J. L. Mozos, P. Ordejón, J. Taylor, and K. Stokbro, “Density-functional method for nonequilibrium electron transport” Phys. Rev. B 65, 165401, March 2002, doi: 10.1103/PhysRevB.65.16540.

[20] J. M. Soler, E. Artacho, J. D. Gale, A. García, J. Junquera, P. Ordejón, and D. Sánchez-Portal, “The SIESTA method for ab initio order-N materials simulation”

J. Phys. Condens. Matter 14, 11, 2745, March 2002. doi.org/10.1088/0953-8984/14/11/302

[21] J. P. Perdew, K. Burke, M. Ernzerhof, "Generalized gradient approximation made simple", Phys. Rev. Lett., vol. 77, no. 18, pp. 3865-3868, 1996. doi.org/10.1103/PhysRevLett.77.3865

[22] C. Zhan, J. Neal, J. Wu, D. E. Jiang, "Quantum Effects on the Capacitance of Graphene-Based Electrodes" J. Phys. Chem. C 2015, vol. 119, pp. 22297– 22303, 2015. doi: 10.1021/acs.jpcc.5b05930

[23] TCAD Sentaurus Device manual, Synopsys SDevice, Synopsys, Inc., Version J, 2014.09, CA, USA.

[24] R. Kim, U. E. Avci and I. A. Young, "Source/Drain Doping Effects and Performance Analysis of Ballistic III-V n-MOSFETs," in IEEE Journal of the Electron Devices Society, vol. 3, no. 1, pp. 37-43, Jan. 2015. doi: 10.1109/JEDS.2014.2363389

[25] T. Krishnamohan, "Band-engineering of novel channel materials for high performance nanoscale MOSFETs," 2008 International Conference on Simulation of Semiconductor Processes and Devices, Hakone, 2008, pp. 97-100. doi: 10.1109/SISPAD.2008.4648246

[26] G. Eneman, A.S. Verhulst, A. De Keersgieter, A. Mocuta, N. Collaert, A. Thean, L.Smith, V. Moroz, "Band-to-band tunneling off-state leakage in Ge fins and nanowires: Effect of quantum confinement," 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Nuremberg, 2016, pp. 27-30. doi: 10.1109/SISPAD.2016.7605140

[27] GSS (now part of Synopsys) statistical 3D TCAD Simulator, Ver. 2015.1 [Online] http://www.goldstandardsimulations.com/.

[28] T. Sadi, E. Towie, M. Nedjalkov, C. Riddet, C. Alexander, L. Wang, V. Georgiev, A. Brown, C. Millar and A. Asenov, "One-Dimensional Multi-Subband Monte Carlo Simulation of Charge Transport in Si Nanowire Transistors", 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Nuremberg, 2016, pp. 23-26. doi: 10.1109/SISPAD.2016.7605139

[29] M. Bescond, N. Cavassilas, K. Kalna, K. Nehari, L.Raymond, J.L. Autran, M.Lannoo, A. Asenov, "Ballistic transport in Si, Ge, and GaAs nanowire MOSFETs," IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest., Washington, DC, 2005, pp. 526-529. doi: 10.1109/IEDM.2005.1609398

[30] S. Sahay and M. J. Kumar, "Diameter Dependence of Leakage Current in Nanowire Junctionless Field Effect Transistors," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 1330-1335, March 2017. doi: 10.1109/TED.2016.2645640.

Investigation of Inversion, Accumulation and Junctionless mode Bulk Germanium FinFETs

Highlights

- Quantum confinement effects will influence performances of ultra-scaled nano-devices.
- Especially, the band diagram, valley-splitting in different sub-bands, charge distribution in different valleys, charge density occupied in the lowest sub-bands, density of states and effective mass will determine the characteristics of devices.
- Junctionless Germanium Transistors will provide the optimum device performance in scaled dimensions.