Performance of Vertically Stacked Horizontal Si Nanowires Transistors: A 3D Monte Carlo / 2D Poisson Schrodinger Simulation Study

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***Abstract*— In this paper we present a simulation study of 5nm vertically stacked lateral nanowires transistor (NWTs). The study is based on calibration of drift-diffusion results against a Poisson- Schrodinger simulations for density-gradient quantum corrections, and against ensemble Monte Carlo simulations to calibrate carrier transport. As a result of these calibrated results, we have established a link between channel strain and the device performance. Additionally, we have compared the current flow in a single, double and triple vertically stacked lateral NWTs.**

I. Introduction

The electron transport properties in nanowire transistors (NWTs) could be precisely engineered by introducing strain in the channel, different channel materials and also various device cross-section geometries and gate lengths. In our recently published work [1], we established a correlation between gate length, cross-sectional geometry and electrostatic driven performance in ultra-scaled nanowires. Our results show that NWTs with elliptical cross-section have the best device performance in comparison to wires with square and circular cross-section.

In this work we extend our study by presenting results based on correlation between strain in the channel and device performance. Also we establish a correlation between the drive current and vertical stack of multiple-channel NWT. In order to evaluate the device performance, we employed two methods: 2D Poisson-Schrodinger (PS) coupled with drift-diffusion (DD) simulator and 3D ensemble Monte Carlo (EMC) taking in to account accurate quantum confinement obtained from PS+DD then we calibrate DD on EMC.

II. Methodology and Device Description

For the purpose of this work, we have created Si n-channel gate all around NWTs with an elliptical cross-section of 7 nm x 5 nm. All devices have 0.4nm SiO_2 interfacial and 0.8nm HfO_2 (High-k) layer respectively as shown in Fig.1. The doping profile has the following details: channel - $10^{14}/cm^3$, extensions - $10^{20}/cm^3$, and source/drain - $4x10^{20}/cm^3$. Also we have simulated devices with four different gate length of 8nm, 12nm, 16nm and 20nm. Moreover, the possibility of creating a transistor with multiple parallel nanowires channels as a single device has been reported in recent publication [2]. The simulation work is divided into two main steps. The first step is based on solving Poisson-Schrödinger (PS) equations and coupling them to the drift-diffusion (DD) module of the GSS 'atomistic simulator' GARAND [3]. The quasi-Fermi level from the converged DD solution is used as a fixed reference within the Poisson-Schrödinger model to transfer the current transport behaviour between solutions. The PS solution is then iterated until convergence to obtain a quantum mechanical (QM) solution of the charge density. Next the QM charge density from the Poisson-Schrödinger solution is used to obtain a fixed 'quantum correction' term. The DD loop is carried out again, using the 'quantum correction', until convergence is obtained. In this step we have used a valley reduction technique, eliminating the upper valleys (*L*- and *Γ*- valleys) of the silicon conduction band to speed up the solution. Additionally, silicon NWTs with the simulated dimensions contain the majority of charge over the biases of interest within the first ten subbands and we therefore limit the simulated subbands to this number. The second step start is based on 3D-EMC module of GARAND. The converged charge and potential profiles from the previous step are used as initial guess for the 3D-EMC. The QM correction is applied throughout the simulation period to maintain a self-consistent but time-varying electrostatic potential and field distributions. 3D EMC simulations provide accurate physical treatment of the non-equilibrium transport [4]in ultra-scaled channel transistors and result in accurate prediction of the ON-state transistor performance. The obtained results were used as a reference point to calibrate our DD simulator. In such a way we can used DD simulation for fast evaluation of the device properties taking into account the required physical constrains in such ultra-scaled devices. Moreover, during these calculations we have applied various channel strain values.

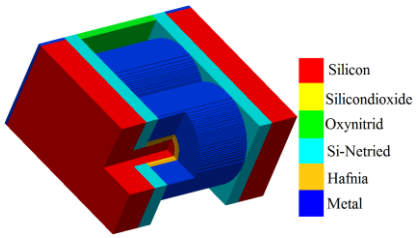

Fig. 1 3D schematic view a Si nanowire transistor (NTW) and material information for the two channel Si NWT.

III. Results and Discussions

The upper part of Fig. 2 shows the I_D-V_G characteristics for NWTs with four different gate lengths of 8nm, 12 nm, 16

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nm and 20nm. All devices are single NWTs without strain in the channel. Those single NWTs were simulated by two methods: DD+PS and EMC methods. In all figures, the solid lines correspond to low drain bias (V_D=0.05V) and the dashed lines are related to the high drain bias (V_D=0.7V). The black solid and black dashed lines in Fig. 2 correspond to a DD solution with defaults values for the mobility parameters. From the results in Fig. 2 is clear that considering such default values for the DD simulation leads to a poor estimation of the I_{ON} current for low and high drain. The recommended option is to calibrate the parameters in DD to correctly reproduce the EMC solution which captures accurately the physics in the devices. Indeed, such calibration is achieved and it is presented with blue triangles on Fig. 2 for all gate length and drain biases. Fig. 2 (down) shows I_D-V_G characteristics for all gate lengths at four different applied strain levels. The applied strain can improve drive currents by 20%-45%. Top part of Fig 3 compares the I_D-V_G curves for NWT with a single, double, and triple channel. As it is expected the tri-channel device has higher I_{ON} current in comparison to one and two channels transistors. However, it needs to be pointed out that the current is not 3 times higher for the tri-cannels device in comparison to the one channel device.

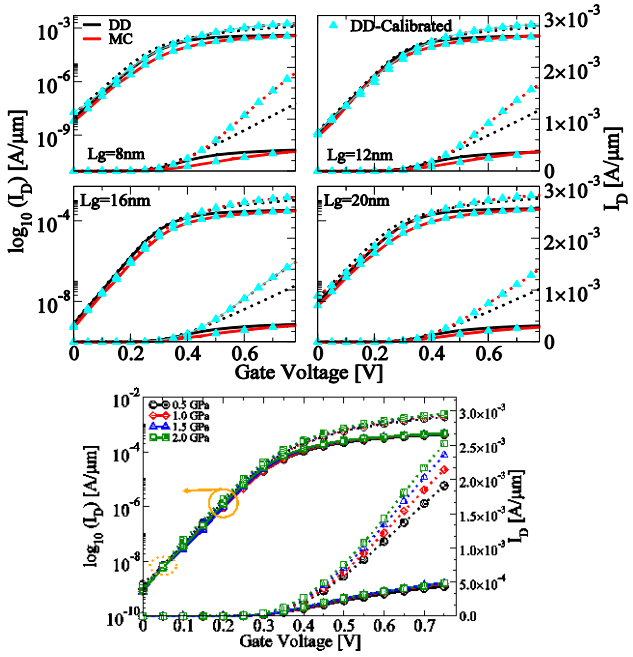

Fig 2 (top) I_D-V_G characteristics for NW with gate lengths 8nm, 12nm, 16nm, and, 20nm. (down) I_D-V_G characteristics for NW with L_G 12nm at applied uniaxial strain 0.5GPa, 1GPa, 1.5GPa and 2GPa based on EMC. Dashed lines are at V_D=0.7V and solid lines are at V_D=0.05V.

The reason for this is clearly visible on the bottom part of Fig. 3. The bottom part of Fig 3 shows the 3D view of the current density for NWTs with single, double, and triple channels devices. The transistor with two channels has almost identical current density in both channel. However, the device with tri-channels show significant difference of the current density between the top nanowire and the bottom one. The main reason for this is that the contacts are on the top of the source and drain region which makes it easier for the current to flow through the closest nanowire channel.

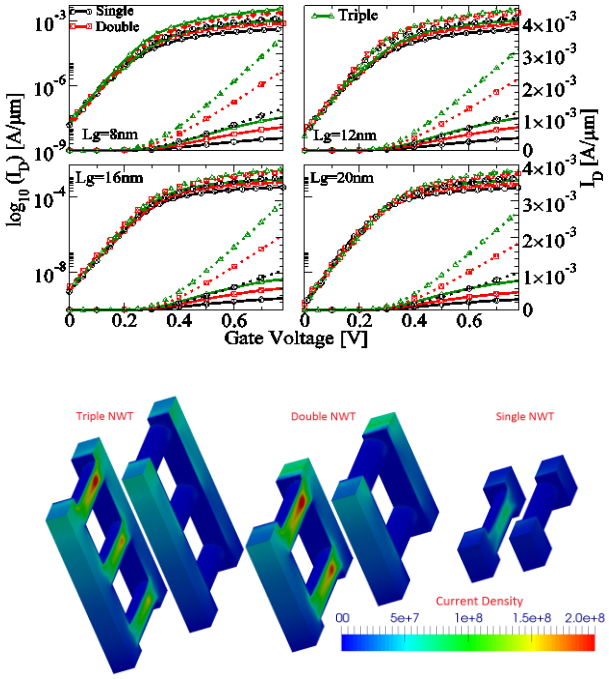

Fig 3 (top) I_D-V_G curves of single, double, triple NW. (bottom) 3D view of the current density for NWTs wit single, duple, and triple channels with L_G=12nm. Dashed lines are at V_D=0.7V and solid lines V_D=0.05V.

IV. Conclusion

In summary, we have simulated ultras-called NWTs with two methods: DD+PS and EMC. Based on those methods we have established a link between channels strain and the device performance. Flowed by implementation of calibration procedure of DD module using PS and EMC simulations over nanowire transistors for feature calculations of various sources of statistical variability and statistical oxide reliability in nanowire. Also we have compared the current flow in single, double and triple vertically stacked horizontal NWTs.

References

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