Experimental and simulation study of a high current 1D silicon nanowire transistor using heavily doped channels

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I. Introduction

Silicon nanowires have numerous potential applications, including transistors, memories, photovoltaics, biosensors and qubits [1]. Fabricating a nanowire with the required characteristics for a specific application, however, poses some challenges. For example, a major challenge is that, as the transistors dimensions are reduced, it is difficult to maintain a low off-current (I_{off}) whilst simultaneously maintaining a high on-current (I_{on}). Some sources of this parasitic leakage current include quantum mechanical tunnelling, short channel effects and statistical variability [2, 3]. A variety of new architectures, including ultra-thin silicon-on-insulator (SOI), double gate, FinFETs, tri-gate, junctionless and gate all-around (GAA) nanowire transistors, have therefore been developed to improve the electrostatic control of the conducting channel. This is essential since a low I_{off} implies low static power dissipation and it will therefore improve power management in the multi-billion transistors circuits employed globally in microprocessors, sensors and memories.

Here we demonstrate a solution by exploiting the quantum effects of a 1-dimensional (1D) Si nanowire transistor (NWT). Whilst 1D devices have been produced in many material systems [3] here we demonstrate 1D nanowires in a scalable, top-down Si technology [4].

II. Methodology and Discussions

All simulations in this study, that analyses gated high doped Si NWT, are carried out using the drift-diffusion (DD) approximation which includes density-gradient quantum corrections (DG). For the purpose of this preliminary study, we assume that the DG reproduces accurately the quantum confinement effects, which is a valid approximation for the wire with such cross-section dimensions [5] [6]. Currently work is being undertaken toward calibrating the DG correction to the 2D Schrödinger - 3D Poisson solver, used for accurate simulation of quantum confinement effects. Also the fabrication techniques and electronic properties of similar ungated and larger nanowires have been published elsewhere [7, 8].

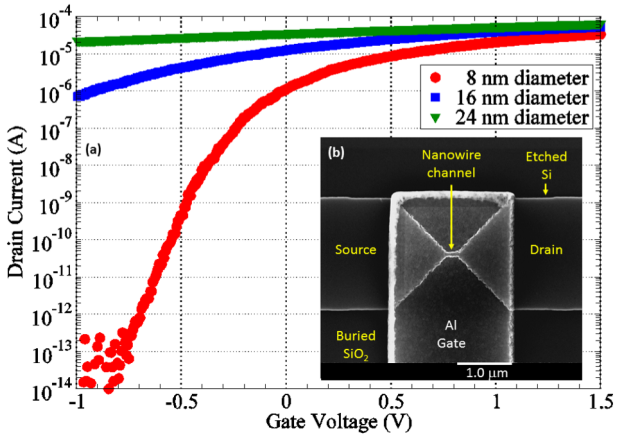

Fig. 1 (a) The drain current as a function of the gate voltage for the Si nanowires with three different diameters of 8 nm, 16 nm and 24 nm and V_D=1.5V (b) A SEM image of the gate over the top of the Si channel and parts of the source-drain regions. The nanowire has length 150 nm, 8 nm diameter of the cross-section and 16 nm SiO_2 thickness.

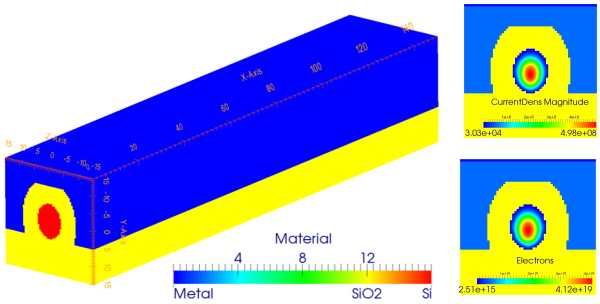

Fig. 2 (Left) A 3D view of the simulated devices, (right) 2D charge and current density distribution in the NWT at V_G=0.6V.

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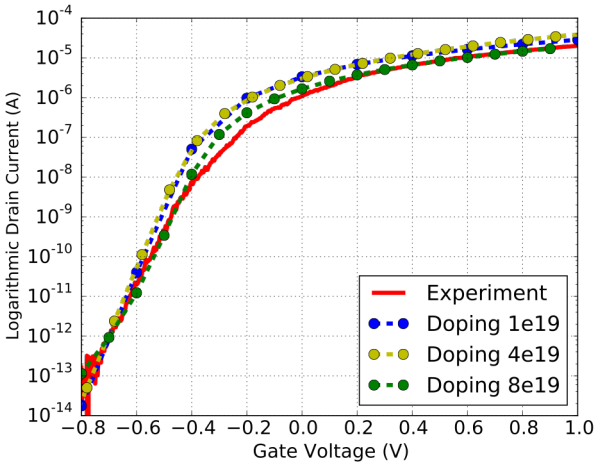

Fig. 3 Drain current vs. gate voltage. Comparison of the experiment and simulation for fixed 150nm gate length at four different theoretically assigned doping concentrations. V_D=1.5V and Si nanowires diameter of 8 nm.

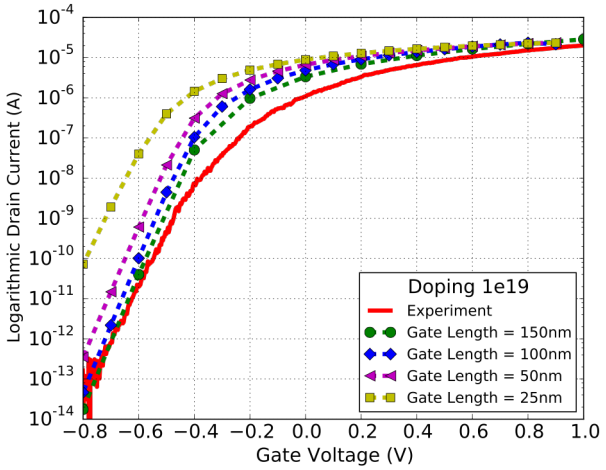

Fig. 4 Drain current vs. gate voltage. Comparison of the experiment and simulation for a doping density of 1e19/cm^3. V_D=1.5V and diameter of 8 nm of Si NWT.

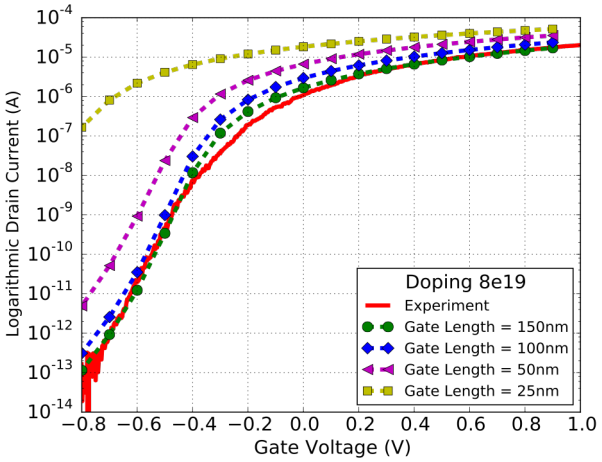

Fig. 6 Drain current vs. gate voltage. Comparison of the experiment and simulation for a doping density of 8e19/cm^3. V_D=1.5V and Si nanowires diameter of 8 nm.

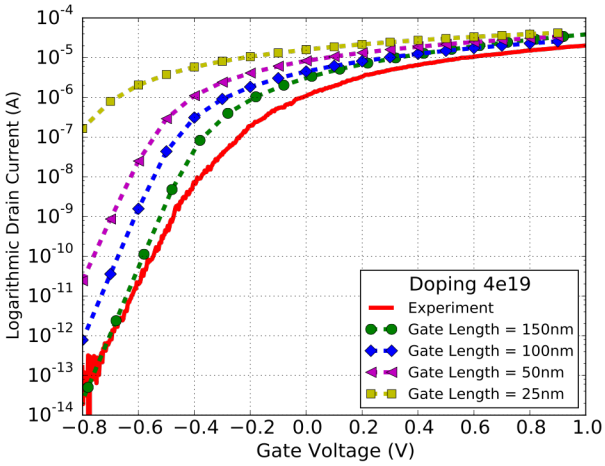

Fig. 5 Drain current vs. gate voltage. Comparison of the experiment and simulation for a doping density of 4e19/cm^3. V_D=1.5V and diameter of 8 nm of Si NWT.

The drain current as a function of gate voltage, measured for nanowires with three different diameters, is presented in Fig. 1. The nanowire diameter is measured by TEM, using the extended crystalline lattice observed in the cross-section. It confirms that using TEM and electron energy loss spectroscopy (EELS) maps. The same figure also reveals the devices lateral geometry. A wide Al gate with the total length of 2 μm is deposited but since the nanowire length is 150 nm, the effective gate-length of the wire is 150 nm. The equivalent oxide thickness is 16 nm.

From Fig. 1 is clear that only the smallest wire with the 8.0±0.5 nm diameter demonstrates good transistor characteristics, where the gate has good electrostatic control of the channel. The I_{on} to I_{off} ratio is above 10^8. As the diameter of the nanowire increases to 16 nm, the I_{on} to I_{off} ratio reduces to around 250 and for the 25 diameter case the ratio is around 2.5. The sub-threshold slope (SS) for the 8 nm nanowire is 66 mV/dec which is close to the theoretical minimum of 60 mV/dec at 300 K. The 16 nm NWT has a SS of 570 mV/dec.

Fig. 2 presents device simulations of the realistic nanowire with gate length of 150 nm and Si diameter of 8 nm. The inserts of the Fig. 2 show the current magnitude and the electron distribution in the channel, which demonstrates transport through the body of the device. This is typical for junction-less devices.

Fig. 3 demonstrates the calibration of the simulations to the experimental data. The best match between calculations and experiment is observed for the calculation with a doping density of 8e19/cm^3. This result is in agreement with the fabrication process where the wires are implanted with a doping density of of 8e19/cm^3. According to the simulations, decreasing of the doping bellow this value, to 8e19/cm^3, improves the SS. In order to obtain a fair comparison, all simulated current-voltage (I_D-V_G) curves are aligned to have the same I_{off} current, which in this case is 1 pA.

Fig. 4, Fig. 5 and Fig. 6 reveal the correlation between four different gate lengths (25 nm, 50 nm, 100 nm and 150 nm) and the I_D-V_G curves considering three different doping concentrations: 4e19/cm^3, 8e19/cm^3, 1e19/cm^3, respectively.

In all cases the NWTs with gate length up to 50 nm reveal good transistor behaviours in all channel doping densities.

Also, in NWTs with gate length of 25 nm, at two doping concentration - 4e19/cm^{3}and 8e19/cm^3, I_{off} current show significantly higher value in comparison to wires with longer gate lengths – 50 nm, 100nm and 150nm.

This trend is even more pronounced in Fig. 7. For all NWTs with the gate length above 50 nm, the I_{on}/I_{off} ratio is above 10^6 which indicates good transistor properties. Moreover, for all wires with the 25 nm gate length the I_{on}/I_{off} ratio value drops between 10^2 and 10^4. In general, the wire with the lowest doping density (1e19/cm^3) has the best I_{on}/I_{off} ratio in comparison to the 4e19/cm^3 and 8e19/cm^3 NWTs.

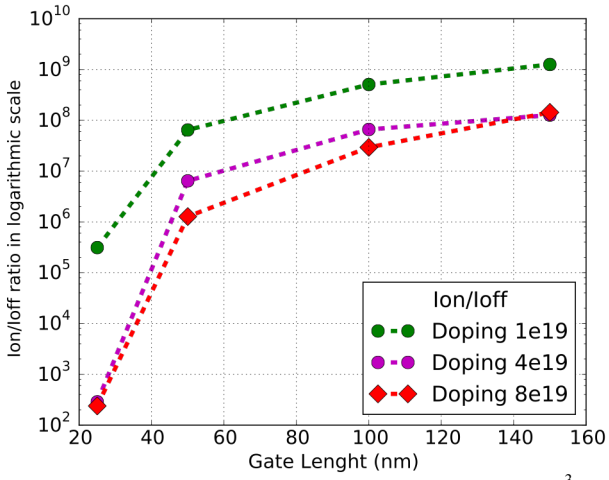

Fig. 7 Impact of three channel doping densities (1/cm^3) on the ratio between I_{on} and I_{off}. V_D=1.5V and Si nanowires diameter of 8 nm.

III. Conclusion

In conclusion, in this paper we report initial steps towards systematic study based on a combination of experimental and computational results for ultra-called 1D Si nanowires with metallic doped channel. We expect these results to allow us to optimise the design of the NWTs and to improve the device performance which could be used for low-power applications.

Acknowledgment

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