Thermoelectric cross-plane Properties on p- and n-Ge/Si_xGe_{1-x} Superlattices

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Abstract – Silicon and germanium materials have demonstrated an increasing attraction for energy harvesting, due to their sustainability and integrability with complementary metal oxide semiconductor and micro-electro-mechanical-systems technology. The thermoelectric efficiencies for these materials, however, are very poor at room temperature and so it is necessary to engineer them in order to compete with telluride based materials, which have demonstrated at room temperature the highest performances in literature [1].

Micro-fabricated devices consisting of mesa structures with integrated heaters, thermometers and Ohmic contacts were used to extract the cross-plane values of the Seebeck coefficient and the thermal conductivity from p- and n-Ge/Si_xGe_{1-x} superlattices. A second device consisting in a modified circular transfer line method structure was used to extract the electrical conductivity of the materials. A range of p-Ge/$Si_{0.5}Ge_{0.5}$ superlattices with different doping levels was investigated in detail to determine the role of the doping density in dictating the thermoelectric properties. A second set of n-Ge/$Si_{0.3}Ge_{0.7}$ superlattices was fabricated to study the impact that quantum well thickness might have on the two thermoelectric figures of merit, and also to demonstrate a further reduction of the thermal conductivity by scattering phonons at different wavelengths. This technique has demonstrated to lower the thermal conductivity by a 25% by adding different barrier thicknesses per period.

1. Introduction

The increasing demand of energy has generated a change in climate on the planet that has made it necessary to identify different strategies to improve energy use [2]. Energy harvesting has become an interesting field to take advantage of energy that is released to the environment in order to make a more effective use of it. The environmental discussion of energy harvesting does not consist solely in replacing high power energy sources and their addition to pollution but it considers the use of power electronic devices for other kinds of environmental savings.

Thermoelectric devices are able to deliver electricity to a load using heat as a power source or to produce heating or cooling in presence of an electrical current. The efficiency of a thermoelectric material is defined by its figure of merit,

$$ZT = \alpha^2 \sigma T/\kappa \qquad (1)$$

where α is the Seebeck coefficient, σ and κ are the electrical and thermal conductivity respectively, and T is the average temperature between the hot and the cold side. The power factor ($PF=\alpha^2\sigma$), which is the second figure of merit of a thermoelectric material, defines the power output that can be delivered to a load, therefore a good thermoelectric material should have a high α and σ, and a low κ. Since the Seebeck effect is responsible for converting thermal energy into electrical energy, thermoelectric generators (TEGs) are suitable for energy harvesting in systems where the energy is released to the environment as waste heat. In addition to sustainable energy generation, TEGs can be easily scaled to satisfy the increasing miniaturization that is demanded of sensors and modules nowadays. Currently, commercial TEGs that work mainly around room temperature (RT) are made of telluride based materials presenting a maximum power output of 2.8 mW at temperature differences of 10 K [3]; enough energy to power a commercial wireless sensor through energy harvesting. These devices present a high density of pellets, such as 1800 number of pair legs integrated in areas of 25 mm^2 [3]. Tellurium, however, is one of the rarest elements on the earth and hence there is increased interest in using different materials with similar or improved efficiencies as an alternative. Furthermore, telluride technology is not compatible with complementary metal oxide semiconductor (CMOS) and micro-electro-mechanical-systems (MEMS) processing.

Silicon (Si) and germanium (Ge) materials are sustainable and suitable for CMOS and MEMS technology. The main problem at the moment is that their thermoelectric efficiencies at RT are still very poor due to their high thermal conductivities, which require engineering to make them competitive with the current market. In low-dimensional structures the addition of a new degree of freedom can contribute to an increase in the efficiency and power output of the system by de-coupling σ from α or κ. For a multi-quantum well structure, this phenomena was introduced by Hicks and Dresselhaus [4], where it was demonstrated that the improvement in α over the bulk system by enhancing the density of carriers, which is a function of the density of states. On the other hand, by engineering the interfaces and the mismatch of the phonons at the different layers, a reduction in the phonon group velocity could be achieved [5], resulting into a reduction of κ.

Three p-Ge/$Si_{0.5}Ge_{0.5}$ superlattices (SL1, SL2 and SL3) with different doping levels were designed and grown to investigate their cross-plane thermoelectric properties as a function of doping density [6].

As a second study, four n-Ge/$Si_{0.3}Ge_{0.7}$ superlattices (SL10, SL11, SL12 and SL13) with different barrier and quantum well (QW) thicknesses but the same doping were fabricated to perform two different experiments. The first experiment aimed to determine the role that the QW thickness might have on the two figures of merit. The second experiment studied the reduction of κ by scattering phonons at the wavelengths that dominate the thermal conductivity of the material.

Ref. [7] already reported some of the samples presented in this work, but in this paper we aim to present more accurate values for κ after performing finite element modeling (FEM) in each of the samples studied. The κ values presented in [7] were an estimation of the experimental data acquired after performing a differential technique. Due to the limitation of our measurement technique, the calculated effective heat flux flowing across the superlattice was over-estimated and therefore smaller values for κ were quoted. FEM analysis has been now performed in every single measurement, including the exact 3D geometry (geometry of the device plus thickness of the complete superlattice) and using the experimental data to extract more accurately the effective heat flowing across the superlattice.

2. Design and Growth

For vertical thermoelectric structures, the heat and carrier conduction occurs perpendicular to the heterostructure. Cross-plane designs should have higher α from the higher asymmetry in the density of the states in the thinner QWs [4,8] and also lower κ due to an increased heterointerface phonon scattering, compare to the in-plane designs [9,10].

For the set of p-type superlattices, Ge QWs were selected for obtaining σ and α values higher than p-type Si samples [11], and $Si_{0.5}Ge_{0.5}$ barriers were chosen to reduce the lattice thermal conductivity of the material as presented in [12]. The three samples (SL1, SL2 and SL3) were doped at doping concentrations of $1.9x10^{17}$, $9.7x10^{17}$ and $2.0x10^{18}$ cm^{-3} respectively. Figure 1 (a) presents the design for these three heterostructures.

For the range of n-type superlattices bulk Ge QWs were combined with $Si_{0.3}Ge_{0.7}$ barriers for all the designs, which were uniformly doped using P as a dopant, and aimed density of $1x10^{19}$ cm^{-3}. Lower Ge content difference between the QWs and barriers was chosen to reduce the interface roughness, which depends on the strain of the material as shown in [13]. Figure 1 (b), (c), (d) and (e) demonstrates the schematic diagrams for the n-type vertical designs, showing the exact heterolayer thicknesses for the samples studied in this work.

All the samples were grown on 100 mm diameter p-Si (001) substrates of 5−10 Ω-cm using low-energy plasma enhanced chemical vapour deposition (LEPECVD) [14,15]. This technique has been developed to reach high growth rates of epitaxial Ge and Ge-rich SiGe alloys, which is suitable for growing layers up to 10 μm thickness within an acceptable time. However, the focused plasma is characterized as having a bell-shaped inhomogeneity, which will result in a variation in the layer thickness across a 100 mm wafer. The variation of the layer thickness can go from 130 % of the nominal thickness in the centre, to 80 % at the edges. A graded buffer layer from Si to Si_xGe_{1-x} was grown at rates 5 and 10 nm/s to obtain a strain-symmetrized superlattice grown on top. The period for all the designs was repeated several times (as indicated in Figure 1) to grow approximately 4 μm thick active areas, which were embedded between a Si_yGe_{1-y} 500 nm thick bottom contact layer and a Ge 60 nm thick top contact layer, both doped at $3x10^{19}$ cm^{-3} to assure the creation of good Ohmic contacts.

The heterolayer thicknesses, as indicated in Figure 1, were determined by high-resolution X-ray diffraction (XRD) and scanning transmission electron microscopy (STEM). [14,16] XRD reciprocal space maps along the (004) and (224) Bragg reflections indicated that all the superlattices were strain symmetrized to the relaxed virtual substrates. The measurements were performed using a PANalytical X'Pert PRO MRD high-resolution X-ray diffractometer: the system is equipped with a hybrid mirror and 2-bounce asymmetric Ge monochromator. The superlattice designs were investigated in a Tecnai F30ST TEM operated at 300 kV (FEI, 0.19 nm point-to-point resolution), and a HD-2700Cs dedicated, Cs-corrected STEM operated at 200 kV (Hitachi, 0.078 nm resolution). Both STEM and XRD indicated interface roughness of order of 4

monolayers for each of the heterolayers for all the samples. The insert of Figure 1 (a) demonstrates a TEM image of SL1 showing the first top layers of the superlattice.

3. Device Fabrication and Characterization

Two different micro-fabricated devices were used to extract the electrical and thermal properties of the material. First a mesa structure was patterned by photolithography and etched using a fluorine-based reactive ion etch process [17]. Next Ohmic contacts were produced at the top and bottom of the mesa using photolithography followed by deposition of Ag (1% Sb) [18] (n-type samples) or Ni (p-type samples) by electron beam evaporation. The samples were then annealed at 400 ^{o}C for 5 minutes to alloy the Ag contacts, and at 340 ^{o}C for 30 seconds to alloy the Ni contacts. Then a thin 50 nm Si_3N_4 electrical insulation layer was deposited by plasma enhanced chemical vapour deposition (PECVD) before four-terminal resistance thermometers consisting of 20 nm of Ti and 80 nm of Pd were patterned at both, the top and bottom of the mesa. 30 nm of Si_3N_4 was again deposited on top of the thermometers to isolate them from the resistance heater made from 33 nm of NiCr and patterned by lithography and lift-off on the top of the mesa. The thermometers were calibrated by immersing the device in perfluo-1, 3-dimethlcyclohexane to produce an isothermal environment for the calibration. Figure 2 demonstrates the calibration of a thermometer with a standard temperature coefficient of resistance of 0.00209 K^{-1}.

The Seebeck coefficients were obtained by extracting the gradient of the Seebeck voltage as a function of the ΔT across the micro-fabricated device. A dc power supply was used to power the top heater in order to create a heat flux across the heterostructure. The two thermometers (top and bottom) were connected in series to a 1 kΩ high precision resistor to lower the current and avoid any Joule heating on the Pd metal line. Two SR830 lock-in amplifiers were used to monitor the change in voltage in the Pd resistor, which was translated into a temperature after performing the calibration. The Seebeck voltage in open circuit was measured by probing the two contacts, whose terminals were connected to an external voltmeter. Figure 3 presents a SEM image of a fabricated device, where all the connections required to extract the Seebeck

coefficient have been indicated. Figure 4 demonstrates the experimental data collected for two identical devices fabricated on SL11.

In addition finite element simulations were used to validate the experimental results and to estimate the error in extracting the Seebeck coefficients in the devices and in particular determining any error from parasitic thermal conducting channels. Experimental and theoretical results, presented else where [19], agreed within 90%.

In order to extract κ a differential technique reviewed in [20] was used. This technique subtracted the effective heat flowing across the active area by discriminating between the multiple parasitic thermal paths on the device. By using this technique a reference sample of SiO_2 produced a κ value of 1.7 ± 0.6 $Wm^{-1}K^{-1}$, which compares well with literature values of 1.6 $Wm^{-1}K^{-1}$ [21].

A modified circular transfer line method (CTLM) [20,22] was used in order to extract the electrical conductivity across the heterostructure. CTLM structures with gap spacing ranging from 1 μm to 200 μm were fabricated and measured first to extract the contact resistances between the metal and the semiconductor. The devices were then etched anisotropically between the contacts for different etch depths, and the resistance values corresponding to 0 μm gap spacing were extracted and plotted as a function of etch depth. The gradient of the intercept resistances versus the etch depth, allowed σ perpendicular to the heterostructure to be estimated.

4. Results and Conclusions

The measured thermoelectric cross-plane properties for SL1, SL2 and SL3 are shown in Table 1, and they are compared to p-Ge bulk material [21] and to in-plane values for $Ge/Si_{0.3}Ge_{0.7}$ superlattices (previous work published in [16]).

The electrical conductivity increased by 75 % from the lowest to the highest doping density and the Seebeck coefficient was reduced by a 25 %. Since the PF is defined by $\alpha^2\sigma$, this increased by a factor of 2.1 reaching

a maximum value of 1.34 $mWK^{-2}m^{-1}$ for a doping density of $2.0x10^{18}$ cm^{-3}. This result is very modest compared to the in-plane values [16], and even smaller than PF for p-Ge material reported in the literature [21]. The main difference was due to the small σ values obtained in the cross-plane direction, which were expected to be 7 or 8 times smaller than the in-plane electrical conductivities, as it is shown in Table 1. At the same time the κ values were reduced by a factor of 4 between the in-plane and the cross-plane data, which suggested that the alloy barriers are strongly scattering phonons in the SL as it was also demonstrated in [23]. This made the cross-plane ZTs, for the highest doping level (SL3), 5 times bigger than for bulk material and quite comparable to the in-plane efficiencies.

The cross-plane thermoelectric properties of four n-Ge/$Si_{0.3}Ge_{0.7}$ superlattices with the same doping densities ($1x10^{19}$ cm^{-3}) have been studied to perform two different experiments, see Table 2. For the first experiment the impact of QW thickness on the ZT and PF was investigated. SL10 featuring a thin QW width of 4.6 nm with and a single barrier was compared to an identical sample SL11 presenting a thick QW width of 12.2 nm and also a single barrier per period. Thin QWs (SL10) have been shown to present higher Seebeck coefficients and so higher values of ZT and PF [8]. The addition of extra layers in SL10 to reach the same SL thickness as SL11 decreased the value of σ by a 60%, but this reduction was compensated by a higher value of α and by a 35 % reduction of κ, resulting into similar ZT values and a higher PF value for SL11 at 300 K. The reduction of κ and σ seems to be dominated by interface scattering, as SL10 had twice the number of interfaces than SL11.

For the second experiment samples with thick QW widths were evaluated. For this experiment the further reduction of the thermal conductivity by adding different barrier thicknesses to the superlattice period and therefore reducing the number of interfaces was studied. Three samples SL11, SL12 and SL13 featuring 1, 2 and 3 different barrier thicknesses per period were compared to scatter phonons more efficiently.

The addition of different barrier thicknesses per period did reduce the thermal conductivity by 25%, and increased the Seebeck coefficient. Table 2 indicates that multiple numbers of barriers per period could decrease the thermal conductivity by a lower density of interfaces. These results seem to indicate that the

reduction of κ is not related to the number of interfaces per unit thickness but by another mechanism, as it could be alloy scattering. In addition STEM and high-resolution XRD measurements indicated an interface roughness of 4 monolayers at the heterointerfaces for the superlattices studied. In [24] it has been demonstrated that alloy interfaces could increase the thermal boundary resistance of superlattices when compared to sharp interfaces, and therefore decrease the value of κ.

On the other hand, the electrical conductivity was also reduced, and therefore the values of ZT and PF remained mainly identical for samples SL11, SL12 and SL13. The presence of roughness at the heterointerfaces could also contribute to decrease the electron transport, phenomena that still need further study.

To conclude, a set of p-type and n-type superlattices with pure Ge QWs and SiGe alloy barriers (rich Ge) have been measured to characterize all the cross-plane thermoelectric parameters that define the efficiency of a thermoelectric material. The thermal conductivity values presented in this work are higher than κ values measured in the literature for Si/Ge superlattices [25,26], which normally present values around 3 W/m K. Nevertheless, the lack of α and more importantly σ values in the literature makes difficult to understand how improving one parameter could actually enhance or deteriorate other one.

In this work the further reduction of κ for samples with multiple numbers of barriers per period with different thicknesses is encouraging for further extension of the number of barriers as this could produce a big impact in the two thermoelectric figures of merit. Higher electrical conductivities could be achieved by smoother heterointerfaces, however, a better understanding for the cross-plane electrical transport is still required to succeed, and to be able to compare these values with the state of the art telluride based materials.

5. Acknowledgements

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Figure 1: (a) The schematic diagram of the p-type design followed for SL1, SL2 and SL3. The insert shows a TEM image of the top of the superlattice for SL1. The schematic diagrams of the n-type vertical designs unit cells that corresponds to SL10 (b), SL11 (c), SL12 (d), and to SL13 (e), showing the exact heterolayer thicknesses which were measured by STEM and XRD.

Figure 2: The calibration of a 20/80 nm Ti/Pd thermometer. The thermometer was placed inside an isothermal environment and its change of resistance was monitored each time the temperature was increased.

Figure 3: A SEM top image of one of the devices where it has been indicated the probing and the equipment used for extracting the Seebeck coefficient.

Figure 4: The Seebeck voltage measured as a function of ΔT between the top and the bottom of the superlattice. The plot demonstrates two individual measurements undertaken in two different devices fabricated on the same chip (SL11).

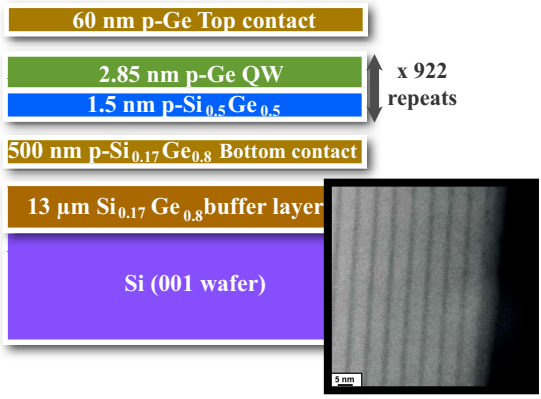
Table 1: A comparison of bulk p-Ge and p-Ge/$Si_{0.3}Ge_{0.7}$ in-plane superlattices, to the present work (SL1, SL2 and SL3).

Table 2: A summary of the thermoelectric properties measured for SL10, SL11, SL12 and SL13. SL10 and SL11 results were investigated to study how thick or thin QW widths can produce an impact in the two figures of merit. While SL11, SL12 and SL13 studied the further reduction of the thermal conductivity by the addition of barriers with different thicknesses to the SL period.

Sample ID	N cm^{-3}	σ S/m	α μVK^{-1}	κ $Wm^{-1}K^{-1}$	ZT	PF mW $K^{-2}m^{-1}$
p-Ge	$7.1x10^{18}$	30,300	300	59.5	0.014	2.73
p-$Ge/Si_{0.3}Ge_{0.7}$	$7.7x10^{18}$	77,169	279	23.1	0.078	6.02
SL1	$1.9x10^{17}$	2,220 ± 62	533 ± 25	6.0 ± 0.4	0.031 ± 0.01	0.63 ± 0.06
SL2	$9.7x10^{17}$	6,680 ± 863	393 ± 7	4.5 ± 0.4	0.068 ± 0.01	1.03 ± 0.06
SL3	$2.0x10^{18}$	8,630 ± 910	394 ± 6	5.1 ± 0.4	0.08 ± 0.011	1.34 ± 0.05

Sample ID	QW/barrier width (nm)	σ S/m	α μVK^{-1}	κ $Wm^{-1}K^{-1}$	ZT	PF $mWK^{-2}m^{-1}$
SL10	4.6/1.5	1,834 ± 287	-455 ± 23	4.3 ± 0.67	0.028 ± 0.003	0.38 ± 0.01
SL11	12.2/2.3	4,471 ± 616	-322 ± 4	5.9 ± 0.5	0.026 ± 0.004	0.45 ± 0.06
SL12	9.3/1.8 9.3/2.6	4,918 ± 745	-295 ± 33	4.9 ± 0.5	0.028 ± 0.006	0.42 ± 0.02
SL13	16.7/2.8 16.0/2.0 15.5/1.5	2,277 ± 394	- 403 ± 3	4.4 ± 0.5	0.027 ± 0.004	0.37 ± 0.06

(a)



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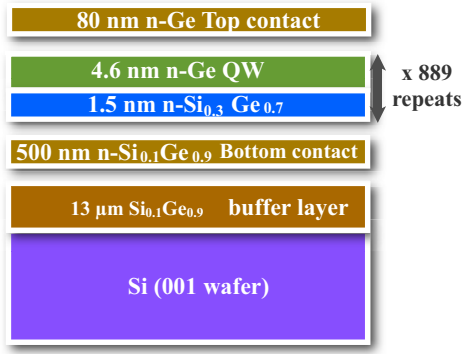

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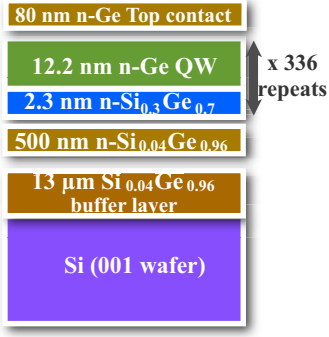

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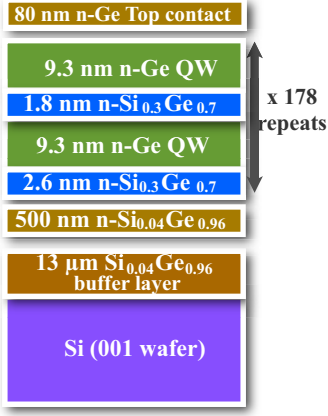

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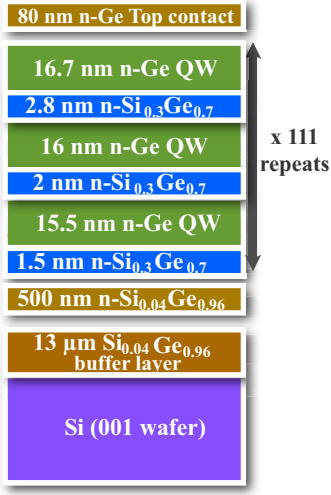

Figure_2
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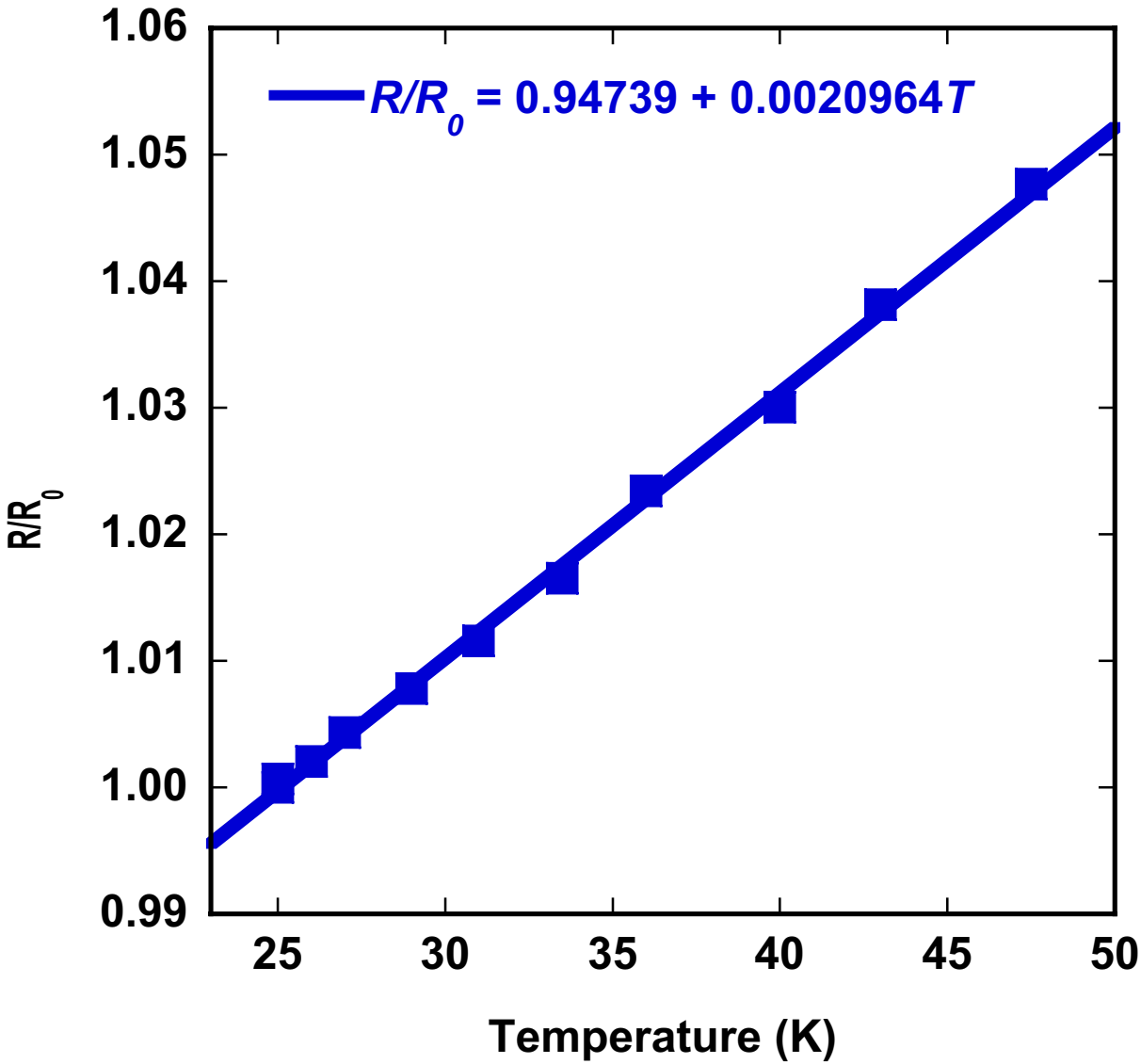

Figure_3

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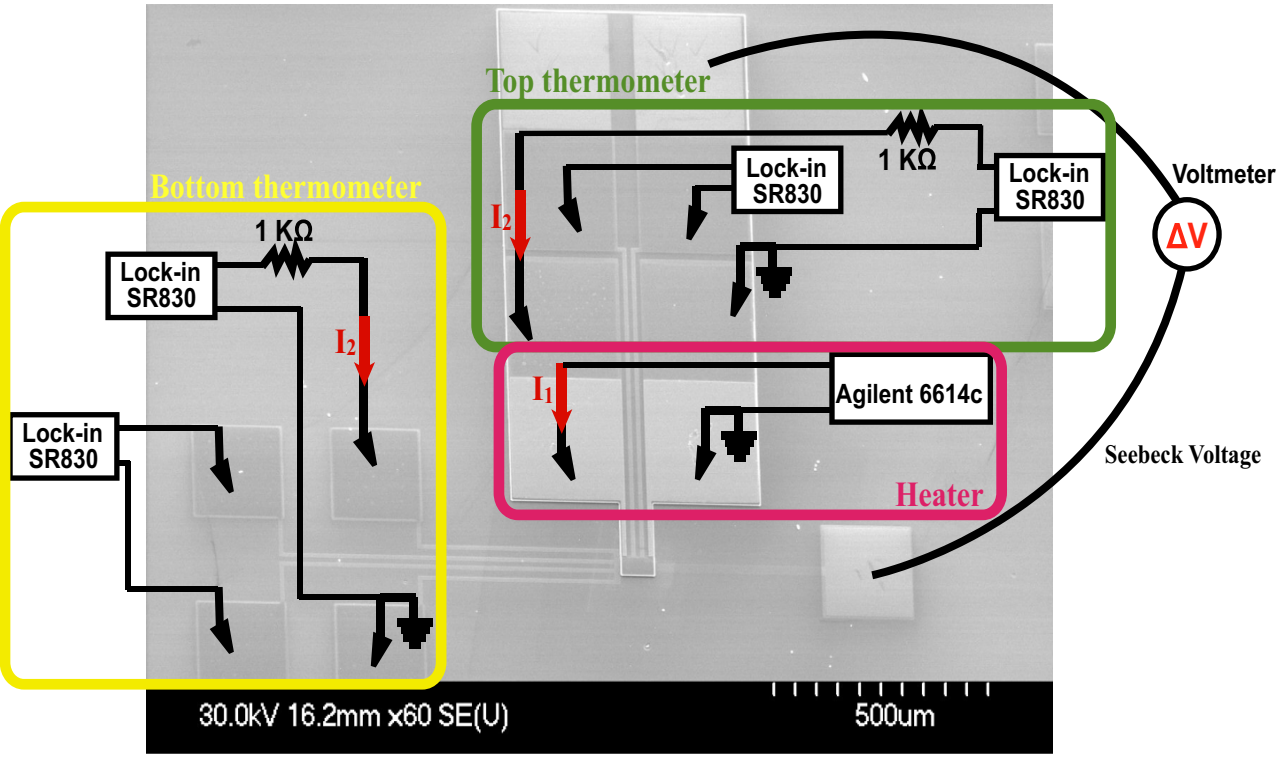

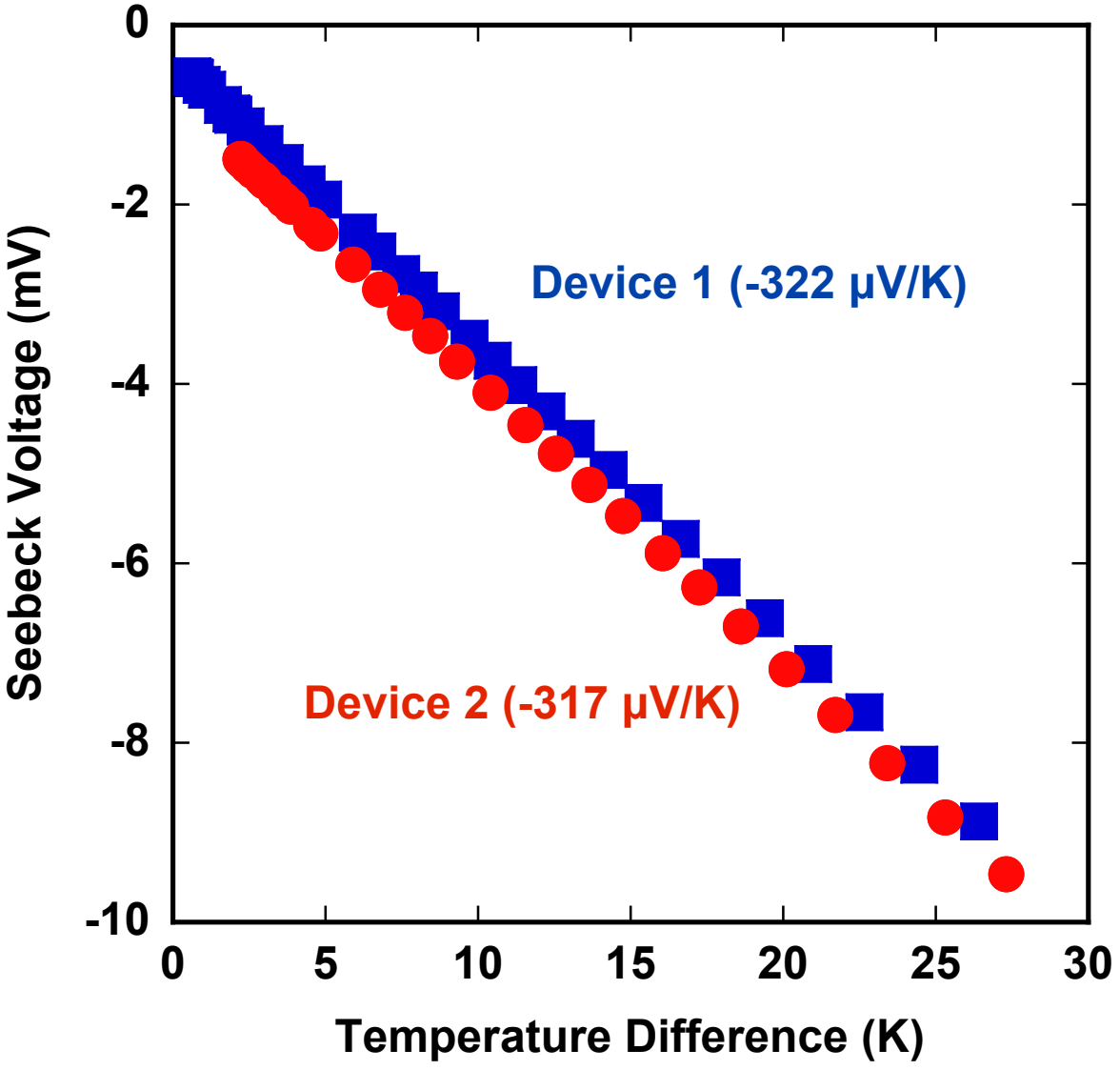
0
-2
-4
-6
-8
-10
Seebeck Voltage (mV)
0
5
10
15
20
25
30
Temperature Difference (K)
Device 1 (-322 μV/K)
Device 2 (-317 μV/K)