This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

Flexible MISFET Devices from Transfer Printed Si Microwires and Spray Coating

Saleem Khan, Leandro Lorenzelli, *Member, IEEE*, Ravinder Dahiya, *Senior Member, IEEE*

***Abstract*—This paper presents two types of MISFETs (Metal Insulator Field Effect Transistors) devices fabricated from Si microwires through a new manufacturing route involving a combination of printing and microfabrication technologies. Si microwires, developed through standard photolithography and etching steps, are transferred from a SOI (silicon on insulator) wafer onto polyimide (PI) using stamp-assisted transfer printing. The MISFETs are then obtained by spray coating the dielectric layer and metal contact layer. Spray coating has been introduced here for the first time for deposition of organic dielectric on transfer printed Si microwires. Two groups of the devices are fabricated, one based on a single Si microwire and the other based on the array of 15 microwires of similar dimensions. The variations in the output response of the two groups of devices has been investigated. The devices based on array of microwires are observed to have less variation in the output response, with lesser standard deviations as compared to MISFETs made from single Si microwires.**

***Index Terms*— Microwires, silicon, spray coating, transfer printing.**

I. Introduction

PRINTED electronics is gaining significant interest these days because of the potential for cost-effective manufacturing and electronics over large areas and non-planar substrates. A cost effective manufacturing is always a desired feature and therefore it is not surprising if the current trend indicates the merging of well-established microelectronics and printing technologies [1-3]. In terms of applications, the devices and systems printed on flexible substrates provide an attractive avenue for the foldable and wearable electronics and e-skin for robotics and healthcare etc. [1, 4-6].

Typically, the printing technologies are used for solution printing of materials such as organic semiconductors, which form the active layers of the electronic devices. Organic semiconductors are inherently flexible, and are considered to have lower material and fabrication costs (which is often mistaken as the cost of final device). However, the major issues with organic semiconductor based devices are their poor stability, non-repeatable response and poor device performance, especially in comparison with silicon based devices. This is because of number of factors including low mobility of organic semiconductors (~1 cm^2/V.s in comparison with ~1000 cm^2/V.s for single crystal silicon (Si)) [7-9], and the poor resolution of current printing technologies (as low as ~20μm), which results in higher channel lengths. In this regard, the printing of inorganic semiconductors such as Si can offer an interesting alternative, as Si has 3 order of magnitude higher mobility, and the Si based devices are stable and repeatable [7, 10-13]. For this reason, the transfer printing of Si nanostructures such as nanowires (NWs) has been explored recently and demonstrated as the viable route for high-performance electronics over flexible substrates [7, 11-17]. With nano/microwires form of Si, it is also easier to obtain the electronics on flexible substrates. Further, the high aspect ratio of Si nano/microwires widens the range of functionalities from basic electronic devices to sensors and energy harvesters.

This paper presents a new approach for obtaining single crystal Si microwires based MISFETs. The devices are fabricated using a mix of conventional microfabrication and printing processes. Using conventional microfabrication steps (i.e. photolithography and etching techniques), the Si wires are defined on SOI wafer and then transfer printed onto final substrate (i.e. PI) using PDMS (poly(dimethyl siloxane) as carrier or transfer substrate. The spray coating is then used to print dielectric and metal layers. In comparison to various solution processed techniques, the spray coating is a low cost solution, which also results in low material waste [1, 18-20]. Considering that the conventional microfabrication tools allow better control than the coating methods, the approach reported here is likely to result in the variability among the device responses. For this reason, we have developed two different sets of MISFETs, first based on single Si microwire and the second based on the array of microwires and both sets have been evaluated in terms of uniformity of device responses. Due to lesser statistical variations, the arrays type MISFETs show better response uniformity than the devices based on single microwires.

This paper is organized as follows: Section II discusses the materials and experimental steps such as the transfer printing and spray coating for device fabrications. The device designs described in the Section III, is followed by results and discussions in section IV. Finally, the major research outcomes of the paper are summarized in section V.

II. Materials And Experimental Procedures

A. Thin and Flexible Silicon

The Si based microelectronics technology has transformed the electronics industry and Si still remains the favorite due to some of the features highlighted in the previous section. The additional features include the regular crystal structure of Si, which has been extensively studied and is controllable to a large extent for desired electronic applications [21-23]. The developments in microfabrication technology for Si in the last

This work was supported in part by the European Commission under grant agreements PITN–GA–2012–317488-CONTEST, and EPSRC Fellowship for Growth – Printable Tactile Skin (EP/M002527/1).

Saleem Khan and Leandro Lorenzelli are with Centre for Materials and Microsystems, Fondazione Bruno Kessler, Trento 38123, Italy.

Ravinder Dahiya is with Electronics and Nanoscale Engineering Research Division, School of Engineering, University of Glasgow, G12 8QQ, UK. Correspondence to: Ravinder.Dahiya@glasgow.ac.uk

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

few decades have provided many opportunities to explore new applications for Si based devices [24]. However, these developments have largely witnessed Si as rigid substrates. With new applications, described in previous section, the need has arisen for electronics on nonconventional polymeric substrates, which conform to curved surfaces. The additional high-performance requirements have also brought Si in focus for flexible electronics [7-9]. For this reason, Si in different forms (e.g. ultra-thin chips, membranes, micro/nanowires and microribbons etc.) have been investigated recently for flexible electronics [7, 11-17]. The Si micro/nanostructures based approach is particularly attractive because of the potential for obtaining electronics and sensors from them on large areas (larger than standard wafer size). In this regard, the Si microwires based transistors described in following sections mark a significant advance towards high-performance electronics on flexible substrate.

B. Si Microwires Fabrication and Transfer Printing

1) Si microwires design and fabrication

A key challenge with Si based flexible electronics is that some of the fabrication steps (e.g. high quality oxide deposition, annealing after implantation etc.) require high temperatures (700-1000 ^{o}C), which are incompatible with most of the plastic or polymeric substrates. This thermal budget related issue has been overcome in this work with new fabrication strategy, whereby fabrication steps requiring high-temperature are carried out while Si microwires are still on the wafer and rest of the steps, which can be carried out at low temperatures (e.g. metallization), are carried out after the microwires have been transferred to polymeric substrates. This modified fabrication approach has been demonstrated in past [14, 25]. The methodology was used to obtain microwires (Fig. 1(a)-(b)) from *p*-type SOI (Si on insulator) wafer with 2.5 µm top Si layer and resistivity ~15 Ω.cm). The SOI wafer was used in this work because it allows better control over the geometric parameters such as thickness of microwires (Fig. 1 - 2). The photomask needed to fabricate Si microwires (developed with L-Edit from Tanner, Electronic Design and Automation) contains the desired patterns for alternate wires and trenches. The trenches (Fig. 2 a-b) are the locations where the Si from SOI wafer was etched away anisotropically using DRIE (dry reactive ion etching). The microwires with different combinations of lengths and widths were fabricated to investigate the effect of wire dimensions on process of transferring microwires and to optimize the same. It was observed in past that the contact area between the polymeric stamp and the Si microwire affects both the transfer of microwires from the donor to carrier substrate and the carrier to the final target substrate. Similarly, the length of the microwires is critical to prevent the breaking or delamination of microwires from the carrier substrate. For this investigation, the microwires and trenches were fabricated with a combination of varying widths (e.g. 4, 6, 8, 10, 20, 50 µm) and lengths (e.g. 30, 50, 100, 150, 200, 1000, 5000 µm). A total of ten samples arrays (of 15 microwires each) were designed in the photomask for each of the above combinations.

Fabrication of Si microwires followed the standard photolithography steps. The process starts with cleaning of a

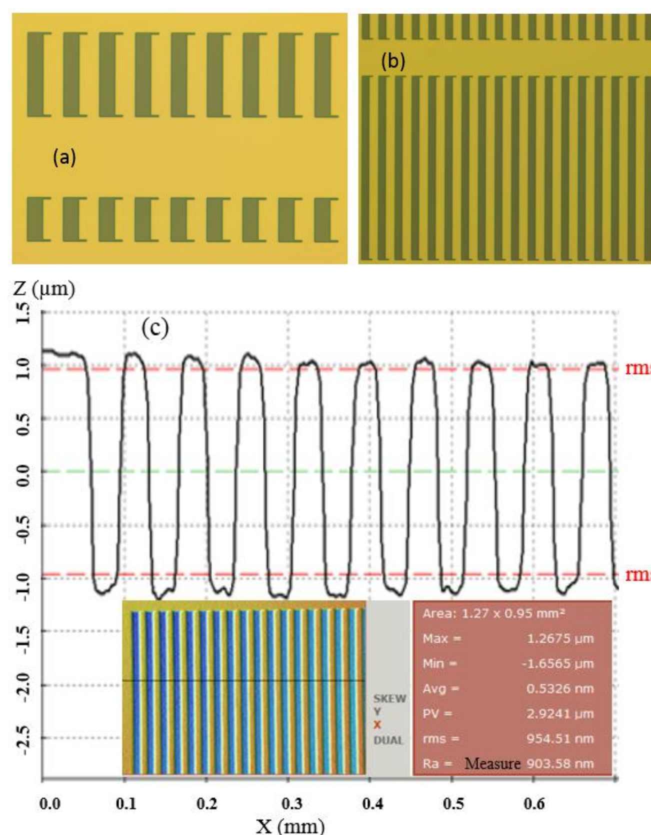


Fig. 1. Optical graphs of Si microwires after photolithography and DRIE etching. (a) Si microwire with 50 µm trench, µm um width and 30 µm stress intensifier, (b) Si microwire with 40 µm and 30 µm trench and 20 µm stress intensifier. (c) Optical interferometer graph of the wires showing uniformity of the wires widths and deep trenches.

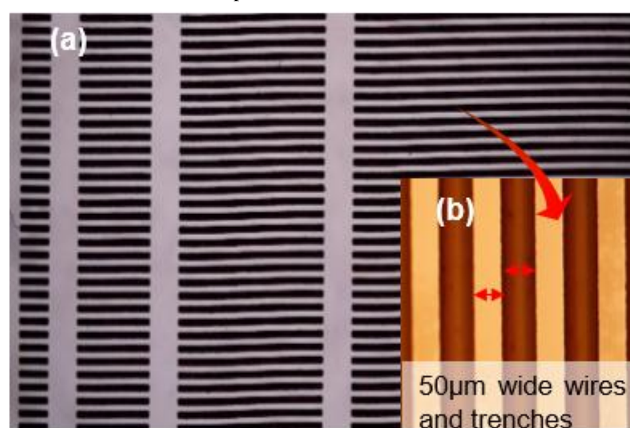


Fig. 2 (a). DRIE etched 50 µm Si wires on SOI wafers after finishing fabrication process. Inset (b) shows Si microwires with trenches of similar dimension as microwires.

p-SOI (boron doped) wafer through standard RCA cleaning process, then coating the wafer with positive photoresist to define the alignment marks and finally, developing the photoresist. The alignment marks were plasma etched and the photoresist was removed through ashing and wet resist removal steps. The pre-litho clean was also performed before defining the trench areas and positive photoresist was coated to define the trench structures. The 2.5µm thick Si microwires were then obtained by anisotropic Deep Reactive Ion Etching (DRIE). Following this step, the photoresist was removed and

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

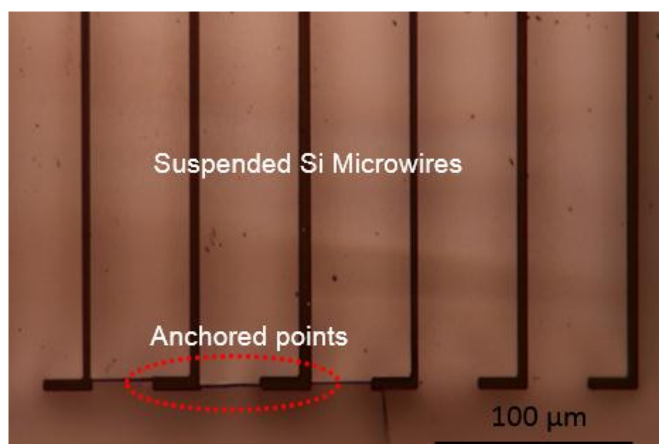


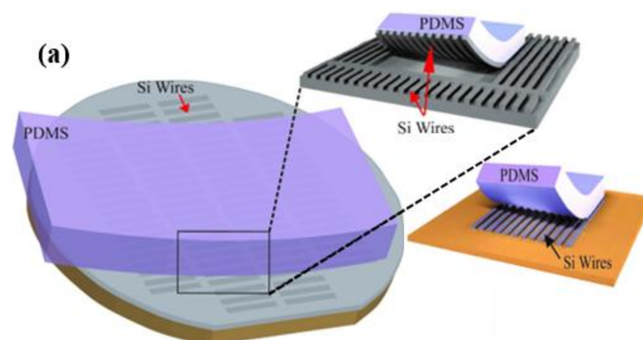
Fig. 3. Optical micrograph of the under-etched Si microwires, before their transfer to PDMS stamp.

through standard wet etching steps. Following this the microwires were treated with piranha (i.e. solution of H_2SO_4 and H_2O_2 in 3:1 ratio) to remove any residual organic layers. Various Si microwires developed with this approach are shown in Fig. 1(a-c). The dimensions such as the depth and width of trenches or the thickness and width of microwires, observed through optical interferometry, are shown in the Fig. 1(c).

2) Transfer Printing

The first step in the transfer printing of Si microwires is to ensure that they are tethered to SOI wafer only at the anchored points (Fig. 2 and Fig. 3). Therefore, after fabrication of microwires, the SOI wafer was kept in buffered HF (BHF) solution to etch away the buried oxide. The duration of oxide etching depends on the width of microwires and the etching rate of solution. It was observed that the transfer yield of more than 95% can be achieved with overetching of buried oxide, which is done by keeping the SOI wafer with microwires in BHF for some extra time (~15 minutes in this work) than desired. After this, the sample with microwires was gently washed with acetone, isopropanol, deionized water, and kept in an oven at 100 ^{o}C for about 10 minutes. Fig. 3 shows optical micrograph of Si microwires before transferring to PDMS stamp.

Transfer printing from donor (i.e. SOI) to receiver substrate can be carried out with either: (a) wet-assisted process, or (b) dry-transfer printing. In the wet-assisted process, the Si microwires are dispersed in a solution, which is ultimately printed on target substrate using various dispensing methods [1]. The microwires are randomly deposited with this method and it is difficult to keep track of the desired finished or doped surfaces for further processing. On the contrary, dry-transfer printing results in deterministic assembly of oriented microwires on the transfer substrate. Within dry-transfer printing there can be two approaches: (a) flip-over, and (b) stamp-assisted transfer printing. The flip-over transfer is a single step process where the adhesive surface of the target substrate is brought in conformal contact with the Si microwires and then pulled over to pick the microwires. However with this method the top surface of microwires



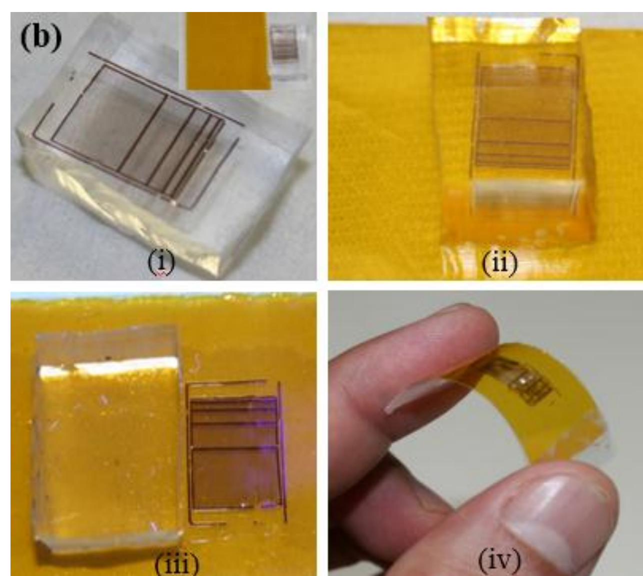


Fig.4. (a). The steps related to transfer printing of Si wires from SOI wafers to flexible substrates; (b) Experimental results at various stages of transfer printing: (i) Wires picked-up by PDMS stamp (ii) PDMS stamped on adhesive SU-8 layer (iii) Wires transferred to substrate after removing PDMS (iv) Wires in bent mode.

(which is also doped for development of device after transfer is achieved) is facing towards the transfer substrate, which makes it difficult to carry realize metal contacts. Given this challenge, the stamp-assisted transfer printing (which involves two flip-over steps) is preferred for dry transfer printing. The process shown in Fig. 4(a)-(b), uses elastomeric stamp to pick the Si microwires from donor wafer and transfers them onto the target substrate. The stamp-assisted transfer printing is used in this work to transfer of Si microwires onto flexible polyimide (PI) substrates. The above steps are compatible with the thermal budget of PI, which is ~300°C [26]. To facilitate the dry transfer printing, a highly planar PDMS (polydimethylsiloxane) carrier stamp was developed with a special mould, which had two polished silicon wafers held 5mm apart. This leads to 5mm thick PDMS stamp. A thicker stamp is desired to prevent any cracks in the wire during the transfer process. The details related to the mould assembly and development of planar stamp are described elsewhere [25, 26].

The PDMS stamp was brought in conformal contact with microwires and was left there for about five minutes. The small Van der Waals forces between microwires and PDMS allow sufficient adhesion between them [12, 17]. The adhesion can also be tuned with plasma oxidation to functionalize the PDMS surface. The controlled adhesion is a critical step, as strong adhesion at this level is not desired as one more transfer

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

step is needed to obtain the devices. The PDMS was peeled-off gently (with about 30 degree angle between the wafer and PDMS at peel-off point) to break the microwires at the tethering points.

In the second transfer step, a stronger adhesion of Si microwires and target substrate is needed for higher transfer yield of microwires from PDMS to PI. To achieve this a thin adhesive layer of SU-8 (Microchem, positive photoresist) is spin coated on the flexible PI substrate. When partially cured the SU-8 exhibits a sticky behavior, which is exploited here as adhesive. Fig. 4b (i)-(iv) show the experimental results at various transfer steps. SU-8 has the advantage of being with ultraviolet (UV) light curable, which promotes the rapid transfer of microwires from PDMS to flexible PI substrate. The optical transparency of PDMS stamp also facilitates the UV light curing of the underlying SU-8 layer. The strong bond between Si microwires and SU-8 layer ensured 100% transfer yield in the second transfer step.

C. Device Designs

The efficacy of the transferred Si microwires can be validated through active devices from them. Therefore, the Si microwires were used to obtain different top-gated field effect transistors or MISFETs. These included: (a) transistors from single microwire of 50µm width, and (b) transistors from an ensemble of microwires (an array of 15 wires, each 50 µm wide). The reason behind using an ensemble of microwires for MISFETs is to investigate the better uniformity of device responses. As discussed in Sec 1, the spray coating for metallization results in dimensional variations, which in turn affect the response uniformity among devices, especially for the device made of single microwires. However, such variations are averaged out in the case of devices made from ensemble of microwires. The usefulness of uniform response will be significant when these devices are used to develop circuits. For example, with two similar transistors with dissimilar responses, the circuit design is challenging. The wires width of 50µm was chosen because of higher transfer yield for this width [26]. The architecture of top-gate top-contact MISFET structures is shown in Fig 5 (a)-(b). The dimensions and number of microwires could be reduced easily during the photolithography stage to control the area of the final devices.

D. Spray Coating

The overall cost of fabricating Si microwires based devices could be reduced by using solution based printing for some of the steps [1, 19]. Spray coating has been used in this work for depositing the dielectric layer and metallic patterns, as shown in schematic of the Fig. 5(a)-(b). The spray coating is single step process for depositing functional materials, with a hard/shadow mask used to define the patterns. It is a low-cost process and the experiments are performed in ambient conditions, which makes it compatible with flexible substrates. Post transfer printing all steps require low temperature (i.e. within the thermal budget of PI substrate i.e. < 300°C) processing. Likewise, the chemicals should be compatible with the polymeric substrate and the receiving (SU-8) layer to

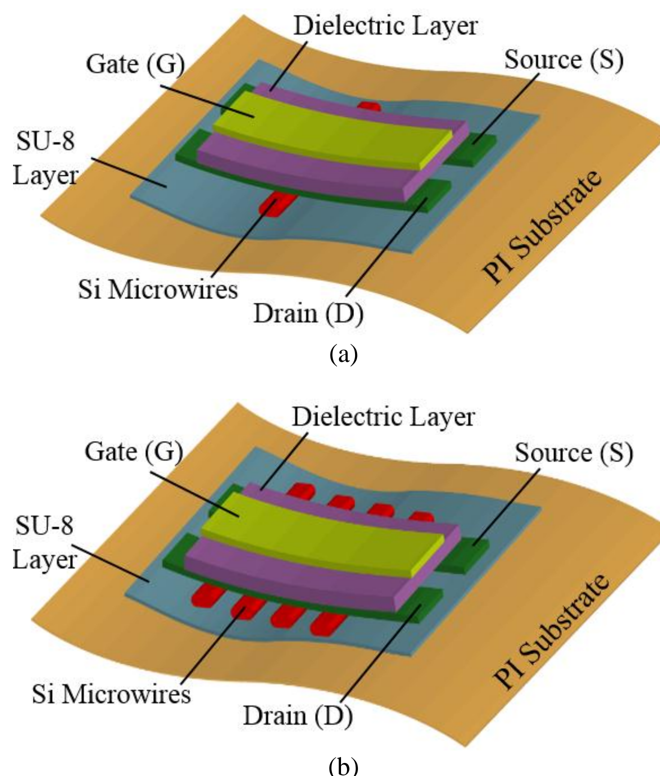


Fig. 5. The scheme of MISFET devices using (a) single Si microwire, and (b) array of Si microwires.

prevent deterioration of the interface between Si microwires and adhesive layer. For this reason, the standard photolithography and etchants cannot be used after transfer printing of Si microwires. Moreover, the trenches between Si microwires make it challenging to have uniform coating of materials. The aerospray coating technique is therefore an attractive choice for depositing the dielectric and metallic layers.

The spray coating, shown in Fig. 6, is a direct deposition technique where the material is deposited from solution with specific process parameters like atomization pressure, snap-off between substrate and nozzle tip, speed and temperature of the supporting plate for the substrate. All the surfactants and solutions evaporate either during the spraying or immediately after deposition on the hot substrate. As a result, a uniform and thin layer can be deposited with whole area covered, especially the non-continuous surfaces of Si microwires. Spray coating is also a material efficient process. The above features make spray coating ideal for bringing down the overall cost. A UV-curable as well as organic dielectrics such as PMMA (poly(methyl methacrylate)) are selected for deposition of the dielectric layer for the MISFETS and Ag (silver) based paste is used to develop the metallic patterns for source, drain and gate contacts. For patterned deposition of both materials, shadow masks were used. The shadow masks were prepared using a computer controlled milling machine. Spray coating system used in the experiments and key components such as syringe pump, Teflon tubing for fluid delivery, nozzle holder, hot plate and shadow masks for patterned deposition are shown in Fig 7(a)-(d). A double concentric nozzle with internal diameter 500 µm and external diameter of 1 mm (Fig. 7(b)) was used for the spray

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

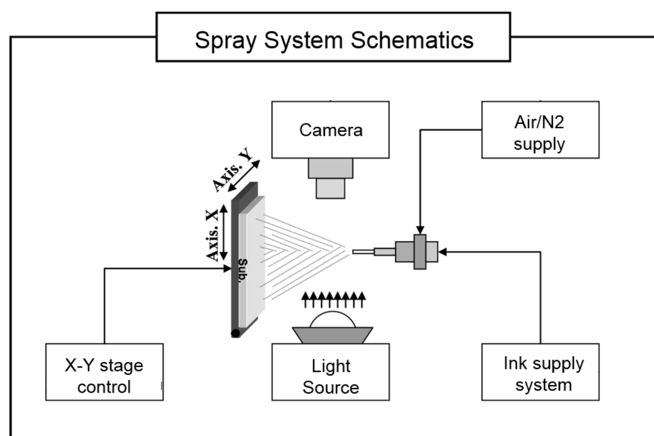


Fig. 6. Schematic of the spray deposition assembly with prominent tools for operation.

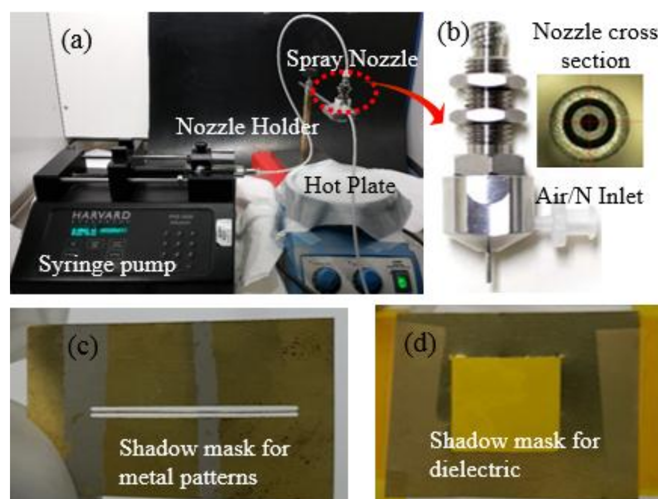


Fig 7. Spray coating system (a) main components of spray coating i.e. syringe pump, tube delivery, hot plate and spray nozzle. (b) Dual concentric spray nozzle with cross sectional view. (c). Shadow mask prepared using milling machine for metal patterns (d) Shadow mask for dielectric deposition.

deposition. The internal nozzle was used for fluid delivery while the outer was used to allow compressed N_2 (Nitrogen) for spraying the solution.

A cleaning step with HF is essential after the transfer printing of Si microwires to remove any native oxide and enhance the ohmic contact between metal and Si microwires. The shadow mask (made of brass), shown in Fig.7(c), was used to realize the source and drain contacts. To keep the metal layers thin (~1µm.), the substrate was heated at around 120°C so as to evaporate the surfactants immediately. This step ensures the deposition of metal layers with good control on the edges, especially in the case of MISFETs made of array of Si microwires, as the trenches between the wires (Fig. 1-2) make the surface nonuniform and uneven. In the case of flowable or low viscosity paste, these trenches act as micro-channels for the paste to flow, which may eventually result in the short-circuiting of source and drain. This was one of the major issues experienced during our previous experiments [15, 26]. Two different solutions are foreseen here to address this issue - the first is to use the Si wires with reduced thickness (i.e. using SOI wafer with Si device layer in nanometer) and the second is the quick solidification of spray-coated metals. The first solution comes with greater risk of Si microwires breaking during the transfer-printing step. Partial sintering or instant solidification of spray–coated Ag paste (e.g. due to a heated substrate) can be used to prevent short-circuiting the source and drain. The latter option is also closer to rapid processing for large area flexible electronics.

An ultraviolet (UV) curable (DuPont 5018) solution of the dielectric material is spray coated at the channel area of the devices through the shadow mask shown in Fig. 7(d). Spray coating of dielectric layer is critical as the solution deposited from the top covers all the exposed areas within the shadow mask for uniform deposition of a thin layer. The wire trenches could hinder the uniform or planar spreading of dielectric during the coating step; especially with conventional coating methods such as spin coating. For this reason, UV-curable dielectric solution was spray-coated. A thin layer of about ~450 (±30) nm was achieved as a result of spray coating the dielectric solution. Variations in the layer thickness were observed because of multiple passes of the spray nozzle. If sufficient time is not given for the solvents to evaporate from the substrates, multiple passes of the spray coating results in accumulation of the solution at random locations. This occasional wet on wet deposition could be overcome by properly adjusting the spray nozzle height from the substrate and speed of the stage.

Finally, a separate shadow mask is used to pattern Ag for the gate contact with good alignment with the channel area. Various steps related to spray coating were carried out within the thermal budget of PI substrate. For example, during spray coating the substrate was kept at 120°C to ensure that the surfactants and solvents evaporate immediately after spray deposition of materials. Similarly, the sintering of Ag paste was carried out at 120°C. The solvents used were also compatible with PI and SU-8, which is used here to adhere Si microwires on PI. As a result, uniform thin dielectric and metal contacts were deposited on Si microwires.

III. Results and Discussions

The top-gate structures of MISFETs are mechanically robust as the materials on top of Si microwires prevent their dislocation or breakage. The fabricated FETs have channel length of ~30µm and channel width of 50µm for the single wire devices. The channel width increases 20 times for the array based devices. As the channel length depends on the resolution of printing tools, the device performance is linked to the printing resolution. As a result, small variations in dimensions during printing may lead to bigger variations and non-uniformity of response among similar devices. In this regard, the MISFETs based on array of Si microwires are expected to be better as dimensional variations are averaged out, which then leads to uniform response of the devices.

After device fabrication, the bending tests were performed to inspect the mechanical reliability of the structure and to investigate the adhesion-loss at the interface of Si microwires and SU-8. For this purpose, the structure was attached to a separate plastic sheet and wrapped around cylinders with different diameters of 8, 12 and 16 mm, which are revolved

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

for 500 cycles. Bending test is critical for monitoring cracks caused by the stresses within the layers during the bending process. It is also used to check the dislocation or delamination of the microwires from the adhesive layer. No crack or delamination was observed after repeated bending tests.

For electrical characterization, 12 devices (6 from each type, as described in Table I) are evaluated in terms of drain current and threshold of the onset voltages. A set of 2 devices from each group was investigated under similar gate voltage and the responses were compared. Fig. 4 shows the output response of MISFETs based on array of 20 Si microwires. Fig. 8(a) shows responses of devices 1a, 2a and 3a at different gate voltages. Fig. 8(b) shows the response of other 3 similar devices (i.e. 4a, 5a and 6a) at similar characterization conditions. For device 1a in Fig. 8(a), the saturation threshold voltage for the onset is ~2.1V (V_{DS}) and a drain current of ~1.75μA, whereas its corresponding device i.e. 4a in Fig. 8(b) has a threshold voltage at ~2.2V (V_{DS}) and a drain current of 2.0μA. The difference in drain currents of these devices is 0.3μA and the onset voltage difference is 0.1V. Similarly, the threshold voltage for the onset of device 2a is 2.5V (V_{DS}) and a drain current of 3.1μA while the onset voltage for its corresponding device 5a is 2.1V (V_{DS}) and a drain current of 2.75μA. The corresponding devices 3a and 6a with similar structural parameters have a difference in the onset voltage of 0.4V (V_{DS}) while the change in current response is about 0.2μA. Similarly, Fig. 9(a) and (b) show the variations in the drain current of the devices made of a single Si microwire. Comparison of the data extracted from both the graphs in Fig. 8 and Fig. 9 show an increased drain current with less variations among devices made of multiple Si microwires. Table I summarizes the net changes in the characterization values of the devices with standard deviation and percentage changes between corresponding values. Statistical analysis of the data in the graphs of Fig. 8 and Fig. 9 show mean values of 1.6, 2.4 and 1.9 for the threshold voltages of related devices i.e. (1a, 4a), (2a, 5a) and (3a, 6a) respectively for the multiwires based devices. Similarly, the mean values for the drain current of multiwires-based devices are 1.8, 2.9 and 5.3 respectively. On other hand, the mean threshold voltage values for the single Si microwire based devices i.e. (1b, 4b), (2b, 5b) and (3b, 6b) are 2.5, 2.7 and 3.1 respectively. The mean drain current values for the same set of devices are 0.03, 0.06 and 0.09 respectively. The standard deviation and the average change (in percentage) of threshold voltages for the multiwires-based devices is lesser as compared to the single wire counterparts, as shown in Table 1. It is observed that devices made of multiwires better mitigate the response variations. Further, they are more reliable, as any variations due to physical disruptions of a single wire within the array could be compensated by rest of the wires.

IV. Conclusion

A new fabrication route, using conventional microfabrication technology and printing tools, is presented for development of transistors. Two types of MISFETs have been investigated to understand the types of device structures possible with presented methodology. It has been observed that devices with multiwires have better performance and lesser variations compared to single Si microwire based devices. Further improvement in the device performance is could be obtained by decreasing the width of microwires from 50μm, as this will result in increased aspect ratio and diminishing the overall size of the device. We conclude that devices using arrays of Si microwires are less prone to printing related dimensional variations and have better reliable performance compared to devices with single microwire.

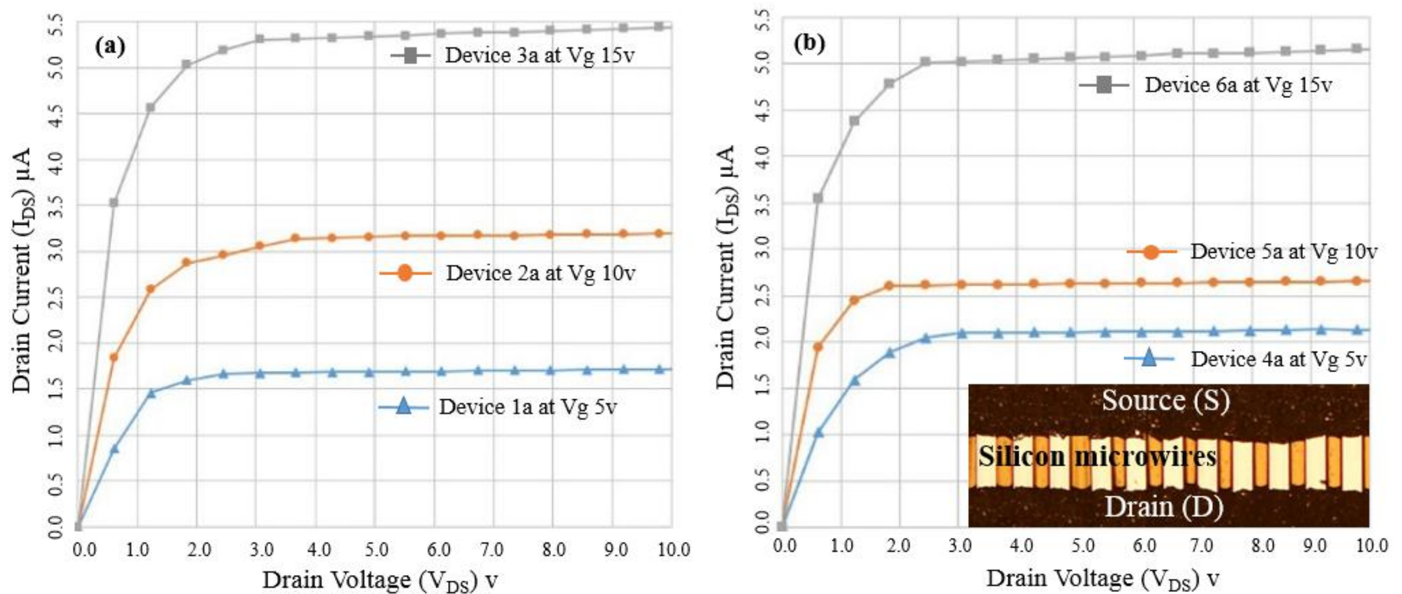


Fig. 8. (a) and (b). Output response of MISFET devices made of multiple Si multiwires at different gate voltages. (a) and (b) represents two sets of devices with similar geometric parameters and characterized under similar conditions of drain and gate voltages.

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

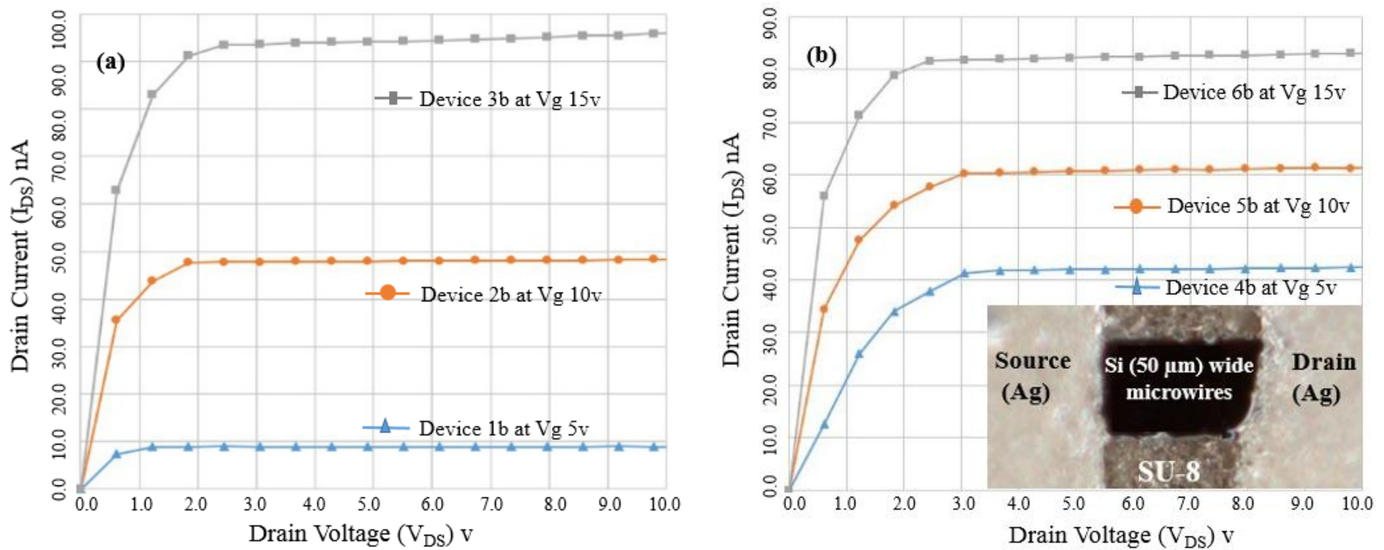


Fig. 9. (a) and (b). Output response of MISFET devices made of single Si microwire with at different gate voltages. (a) and (b) represent two sets of devices with similar geometric parameters and characterized under similar conditions of drain and gate voltages.

TABLE I. Summary of the responses with corresponding device variations.

Relevant Devices	ΔV_{th} (v)	δ (V_{th})	ΔV_{th} %	ΔI (μA)	δ (I)	ΔI %
1a, 4a	0.1	0.07	4.65	0.25	0.18	13.33
2a, 5a	0.2	0.18	9.52	0.35	0.25	11.96
3a, 6a	0.1	0.07	3.27	0.15	0.11	2.76
1b, 4b	1.2	0.85	48.00	0.03	0.03	> 50.00
2b, 5b	0.6	0.43	22.33	0.01	0.07	18.18
3b, 6b	0.2	0.15	6.45	0.02	0.09	14.62

a, corresponds to the type of multiwires based MISFETs (1a, 4a), (2a, 5a) & (3a, 6a) are corresponding devices characterized at similar gate voltages.
b, corresponds to the type of single wires based devices (1b, 4b), (2b, 5b), and (3b, 6b) are corresponding devices at similar gate voltages.

REFERENCES

[1] S. Khan, R. Dahiya, and L. Lorenzelli, "Technologies for Printing Sensors and Electronics over Large Flexible Substrates: A Review," *IEEE Sensors Journal,* vol. 15, pp. 3164-3185, 2015.

[2] P. F. Moonen, I. Yakimets, and J. Huskens, "Fabrication of Transistors on Flexible Substrates: from Mass-Printing to High-Resolution Alternative Lithography Strategies," *Adv. Mater,* vol. 24, pp. 5526-5541, 2012.

[3] B. Michel, A. Bernard, A. Bietsch, E. Delamarche, M. Geissler, D. Juncker, *et al.*, "Printing meets lithography: soft approaches to high-resolution patterning," *IBM J. of Research and Development,* vol. 45, pp. 697-719, 2001.

[4] R. R. Søndergaard, M. Hösel, and F. C. Krebs, "Roll-to-Roll fabrication of large area functional organic materials," *J. of Polymer Science Part B: Polymer Physics,* vol. 51, pp. 16-34, 2013.

[5] R. S. Dahiya and M. Valle, *Robotic Tactile Sensing – Technologies and System*. Dordrecht: Springer, 2012.

[6] E. O. Polat, O. Balci, N. Kakenov, H. B. Uzlu, C. Kocabas, and R. Dahiya, "Synthesis of Large Area Graphene for High Performance in Flexible Optoelectronic Devices," *Scientific reports,* vol. 5, 2015.

[7] X. Liu, Y.-Z. Long, L. Liao, X. Duan, and Z. Fan, "Large-scale integration of semiconductor nanowires for high-performance flexible electronics," *Acs Nano,* vol. 6, pp. 1888-1900, 2012.

[8] H. Zhou, J.-H. Seo, D. M. Paskiewicz, Y. Zhu, G. K. Celler, P. M. Voyles, *et al.*, "Fast flexible electronics with strained silicon nanomembranes," 2013.

[9] J. Lewis, "Material challenge for flexible organic devices," *Materials today,* vol. 9, pp. 38-45, 2006.

[10] Y. Sun and J. A. Rogers, "Inorganic semiconductors for flexible electronics," *Adv. Mater,* vol. 19, pp. 1897-1916, 2007.

[11] K. Zhang, J. H. Seo, W. Zhou, and Z. Ma, "Fast flexible electronics using transferrable silicon nanomembranes," *J. of Physics D: Appl. Phys,* vol. 45, p. 143001, 2012.

[12] R. S. Dahiya, A. Adami, C. Collini, and L. Lorenzelli, "Fabrication of single crystal silicon mirco-/nanostructures and transferring them to flexible substrates," *Microelectron. Eng,* vol. 98, pp. 502-507, 2012.

[13] R. Dahiya, G. Gottardi, and N. Laidani, "PDMS residues-free micro/macrostructures on flexible substrates," *Microelectronic Engineering,* vol. 136, pp. 57-62, 2015.

[14] T. I. Kim, Y. H. Jung, H. J. Chung, K. J. Yu, N. Ahmed, C. J. Corcoran, *et al.*, "Deterministic assembly of releasable single crystal silicon-metal oxide field-effect devices formed from bulk wafers," *Appl. Phys. Lett,* vol. 102, p. 182104, 2013.

[15] S. Khan, R. Dahiya, and L. Lorenzelli, "Flexible thermoelectric generator based on transfer printed Si microwires," presented at the 44th European Solid State Device Research Conference (ESSDERC), 2014 2014.

[16] G. Qin, J.-H. Seo, Y. Zhang, H. Zhou, W. Zhou, Y. Wang, *et al.*, "RF characterization of gigahertz flexible silicon thin-film transistor on plastic substrates under bending conditions," *IEEE Electron Device Letters,* vol. 34, pp. 262-264, 2013.

[17] R. S. Dahiya and S. Gennaro, "Bendable ultra-thin chips on flexible foils," *IEEE Sensors J,* vol. 13, pp. 4030-4037, 2013.

[18] K. H. Choi, S. Khan, H. W. Dang, Y. H. Doh, and S. J. Hong, "Electrohydrodynamic spray deposition of ZnO nanoparticles," *Jpn. J. of Appl. Phys,* vol. 49, pp. 05EC08 (1-6), 2010.

[19] S. Khan, Y. H. Doh, A. Khan, A. Rahman, K. H. Choi, and D. S. Kim, "Direct patterning and electrospray deposition through EHD for fabrication of printed thin film transistors," *Curr. Appl. Phys,* vol. 11, pp. S271-S279, 2011.

[20] S. Khan, Y. H. Doh, K. H. Choi, A. Khan, N. M. Mohammad, and A. A. Gohar, "Development of Electrostatic Inkjet Head by Integrating Metallic and Silica Capillaries for Stable Meniscus," *Mater. Manufact. Processes,* vol. 27, pp. 1239-1244, 2012.

[21] G. Fisher, M. R. Seacrist, and R. W. Standley, "Silicon crystal growth and wafer technologies," *Proceedings of the IEEE,* vol. 100, pp. 1454-1474, 2012.

[22] A. M. Hussain and M. M. Hussain, "CMOS-Technology-Enabled Flexible and Stretchable Electronics for Internet of Everything Applications," *Advanced Materials,* 2015.

[23] Z. Ma, K. Zhang, J. H. Seo, H. Zhou, L. Sun, H. C. Yuan, *et al.*, "Fast flexible electronics based on printable thin mono-crystalline silicon," *ECS Trans,* vol. 34, pp. 137-142, 2011.

[24] R. Zaouk, B. Y. Park, and M. J. Madou, "Introduction to microfabrication techniques," in *Microfluidic Techniques*, ed: Springer, 2006, pp. 5-15.

[25] S. Khan, N. Yogeswaran, W. Taube, L. Lorenzelli, and R. Dahiya, "Flexible FETs using ultrathin Si microwires embedded in solution processed

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JEDS.2016.2559586, IEEE Journal of the Electron Devices Society

dielectric and metal layers," *Journal of Micromechanics and Microengineering,* vol. 25, p. 125019, 2015.

[26] S. Khan, N. Yogeswaran, L. Lorenzelli, and R. Dahiya, "Si Microwires based FETs on Flexible Substrates," in *11th Int. Conf. on PhD Res. in Microelectr. and Electr.*, Glasgow, 2015, pp. 1-4.

This work is licensed under a Creative Commons Attribution 3.0 License. For more information, see http://creativecommons.org/licenses/by/3.0/.