Influence of quantum confinement effects and device electrostatic driven performance in ultra-scaled Si_xGe_{1-x} nanowire transistors

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***Abstract*— In this work we have investigated the impact of quantum mechanical effects on the device performance of n-type in ultra-scaled Si_xGe_{1-x} nanowire transistors (NWT) for possible future applications. For the purpose of this paper Si_xGe_{1-x} NWTs with different Si_xGe_{1-x} molar fraction has been simulated. However, in all devices the cross-sectional area, dimensions and doping profiles are kept constant in order to provide fair comparison. The design of computational experiment in this work includes nanowire transistors with different gate length of 6nm, 8nm, 10nm, 12nm and 14nm. All wires are simulated with various Si_xGe_{1-x} ratio. As a result we have established a correlation between the mobile charge distribution in the channel and gate capacitance, drain induced barrier lowering (DIBL) and the sub-threshold slope (SS). The mobile charge to gate capacitance ratio, which is an indicator of the intrinsic speed of the NWTs, is also have been investigated. More importantly all calculations are based on quantum mechanical description of the mobile charge distribution in the channel. This description is based on Schrödinger equation, which is indeed preferred approach for nanowires with such ultra-scale dimensions.**

***Keywords*— CMOS, $SixGe_{1-x}$, electrostatics, nanowire transistors, performance, quantum effects, TCAD**

I. INTRODUCTION

The gate-all-around (GAA) silicon nanowire FET structure has the potential of keeping Moore's law applicable beyond sub-5nm CMOS technology. They are being investigated as an option near the end and beyond the current International Technology Roadmap for Semiconductors (ITRS) [1-4]. In such ultra-scaled dimensions the quantum mechanical nature of the charge carriers play an important role which dictates the device behaviour and performance. Some of the quantum mechanical effects are related to charge confinement in the direction perpendicular to the transport. As a result, threshold voltage shift is introduced which is directly correlated to reducing the gate-to-charge capacitance and the charge in the channel available for transport. Therefore, accurate description of quantum mechanical effects in such ultra-scaled devices is indeed mandatory [5-11].

Moreover, various combinations of device architecture and channel materials have been investigated in order to improve the transistor's performance [12]. One possibility is to replace the *Si* channel with Germanium-(*Ge*). *Ge* is of renewed interest as a semiconductor material to complement silicon due to its higher carrier mobility and the trend in gate dielectrics evolution [13]. *Ge* is also compatible to the existing CMOS technology which makes it easy to integrate. Moreover, using different ratio of *Si* and *Ge*, Si_xGe_{1-x}, can lead to improvement of the material properties and the performance of nanowire transistors (NWT) [13]. Our main aim in this paper is to establish a link between different molar ratio of *Si* and *Ge* channel and electrostatic performance on ultra-scaled NWTs, taking into account the quantum confinement effects.

II. DEVICE STRUCTURE

In this paper we consider an n-type test structure of Si_xGe_{1-x} NWT. All devices have a cylindrical cross-section with diameter of D = 4 nm which is similar to our recently published work [14], [16]. The channel has a low doping concentration in the gate region and it is warped with a high-k oxide material (Hafnium) while the source and drain region are relatively highly doped. The Si_xGe_{1-x} molar fraction which is the amount of a constituent (expressed in moles), divided by the total amount of all constituents in a mixture are varied from 10% to 90% for booth *Si* and *Ge* in order to find the optimal electrostatic confinement and performance. The transport direction is along <110> crystallographic orientation. All NWTs have effective oxide thickness of t_{ox}= 0.8nm, gate length 6, 8, 10, 12 and 14 nm, spacer thickness of 5nm, source/drain doping peak of 2×10^{20} cm^{-3} and channel doping of 10^{15} cm^{-3}. 3D view and the design parameters for all simulated devices are presented in Fig. 1 and Table 1 respectively.

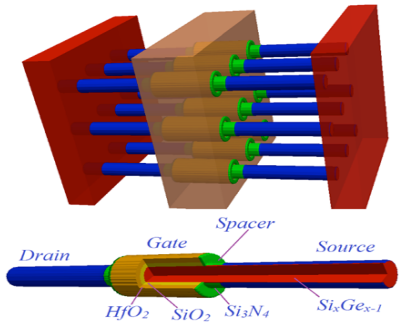

Fig. 1 3D schematic view of the circular NWT (down) and NWTs array (up).

III. SIMULATION METHOD

Our simulations are based on a Poisson-Schrödinger (PS) quantum correction technology achieved in a drift-diffusion (DD) module of the GSS 'atomistic simulator' GARAND [15].

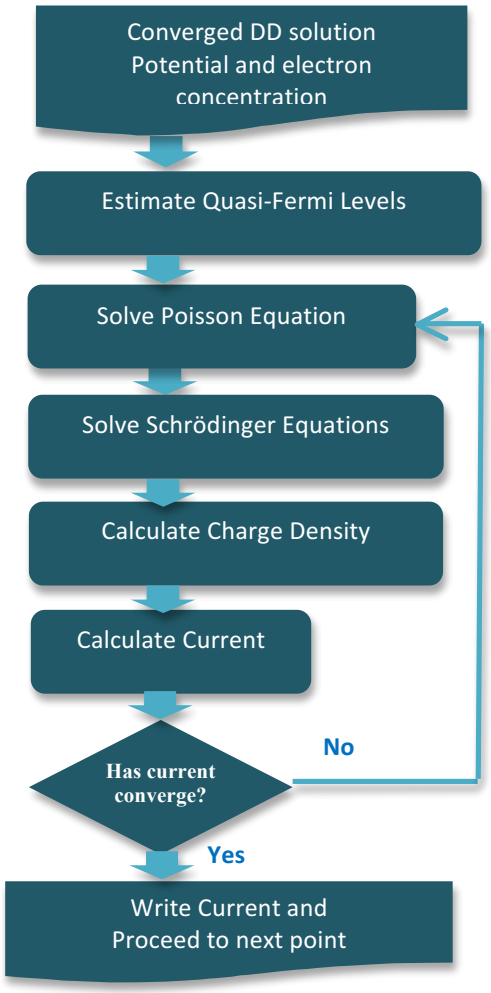

Fig. 2 Flow diagram of the Poisson-Schrödinger model in GARAND simulator.

The PS model is coupled with the GARAND drift-diffusion (DD) solution in stages to allow a computationally efficient manner of combining the impact of quantum confinement and carrier transport (as shown Fig .2). To achieve this, the DD simulation is carried out until convergence, then the quasi-Fermi level from the converged DD solution is used as a fixed reference within the PS model to transfer the current transport behavior. The PS model is then solved until convergence to obtain a QM solution of the charge density. After this the QM charge density is used to obtain a fixed 'quantum correction' term. Using the fixed 'quantum correction' the DD simulation is carried out again until convergence is obtained.

Quantum corrections is included within drift diffusion simulation through the solution of the density gradient equation. This is coupled with both the non-linear Poisson and current continuity solutions and applied to both majority and minority carrier distributions. The quantum corrections modify the carrier distribution in regions of high carrier density variation. The modified carrier density then set an effective quantum potential, applied in the solution of the current-continuity equation. In this way the charge distribution in the NWT's cross section identical to the charge distribution obtained from the Solution of the Schrodinger equation. The simulations are finished when the current converges.

T_{oxide} (nm)	0.8
Gate Diameter (nm)	4
Gate length (nm)	14
Spacer thickness (nm)	5.0
S/D peak doping (cm^{-3})	2×10^{20}
Channel doping (cm^{-3})	10^{15}
Substrate orientation	001
Nanowire orientation	110
Channel material	Si_xGe_{1-x}
Drain voltages (V)	0.05V, 0.7V

Table 1 Parameters of the simulated devices.

	Q_M ($\times10^6$/cm)	C_G (10^{-11}F/cm)	Q_M/C_G (10^{17}/F)
Si	1.13008	3.864140	2.92453
$Si_{90}Ge_{10}$	1.15170	3.897476	2.95499
$Si_{80}Ge_{20}$	1.15990	3.927255	2.95346
$Si_{70}Ge_{30}$	1.16580	3.953547	2.94874
$Si_{60}Ge_{40}$	1.17150	3.976392	2.94614
$Si_{50}Ge_{50}$	1.17870	3.999063	2.94744
$Si_{40}Ge_{60}$	1.18690	4.014751	2.95635
$Si_{30}Ge_{70}$	1.19790	4.026970	2.97469
$Si_{20}Ge_{80}$	1.21280	4.03570	3.00517

Table 2 $Q_M(V_G=0.60V)$, C_G ($V_G=0.60V$) and Q_M/C_G ratio at identical $Q_M(G_V=0V)$ for NWTs at $L_G=14nm$.

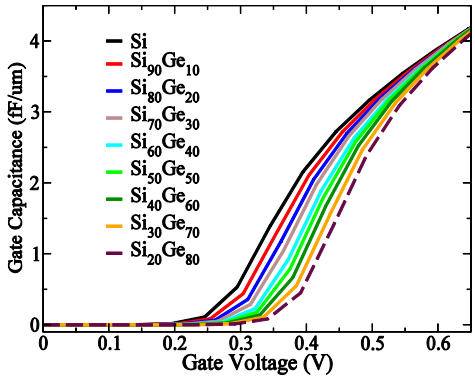

Fig. 3 Gate voltage dependence of the capacitance of all gate-all-around NWTs at L_G=14 nm channel length.

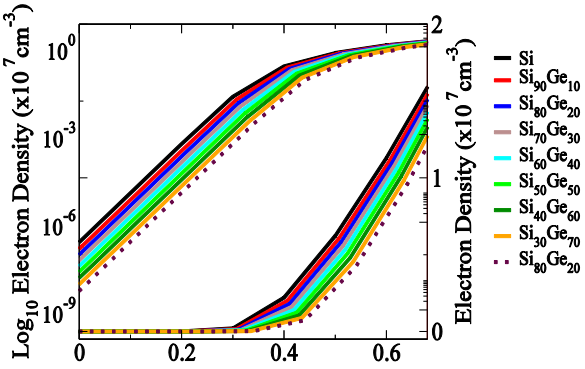

Fig. 4 Gate voltage dependence of the mobile charge of all gate-all-around NWTs at L_G=14 nm channel length.

IV. Results and Discussion

Fig. 3 shows the capacitance-voltage (C-V) characteristics for all simulated NWTs. Fig. 4 presents the gate voltage dependence of the mobile charge in the channel. As expected the mobile charge (Q_M) and the gate capacitance (C_G) increases with increasing gate voltage. Moreover, both the Q_M and C_G reveal their dependence on the *Si/Ge* molar fraction. In order to evaluate objectively the impact of the *Si/Ge* concentrations on the NTW's performance, Table 2 compares Q_M *and* C_G (V_G=0.60V) for identical Q_M (V_G=0.0V). To make this comparison fairer, the Q_M (V_G) curves are aligned by modifying the gate work function.

From Table 2 the following important conclusions can be obtained. Firstly, $Si_{20}Ge_{80}$ has the highest C_G and Q_M/C_G ratio and consistently the lowest value is for pure Si wire. Secondly, increasing *Ge* concentration leads to almost linear increase of Q_M/C_G ratio. Q_M/C_G ratio is an indicator for the 'intrinsic' NWT's speed. Higher value of the ratio means better 'intrinsic' speed.

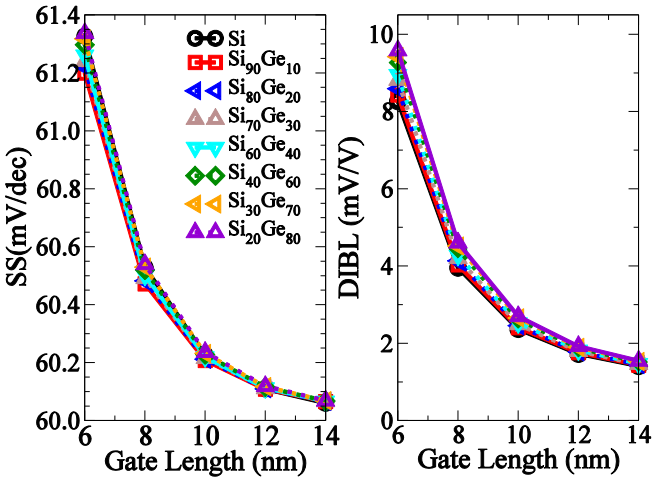

Fig. 5 Impact of the gate length on the SS (left) and DIBL (right) for all NWTs with different $SixGe1_{-x}$ molar fraction.

The impact of the gate length on the drain-induced barrier lowering (DIBL), defined as $\Delta V_T/\Delta V_D$, and sub-threshold slope (SS) is illustrated in Fig. 5. There is a relatively little difference in the electrostatic behavior between the NTWs with different *Si/Ge* fraction. Both DIBL and SS increase with decreasing the gate length of the devices. However, there is no significant difference between the values for both descriptors at each gate length. Also the difference in SS and DIBL values increases with decreasing of the gate length.

Fig. 6 presents the electron concentration and electrostatic potential for all devices along the transport direction. From the figure is clearly visible that the main difference between the devices is in the channel region. Also the charge in the channel and the potential increase with increasing *Si* concentration. Fig. 7 reveals the 2D charge distribution in the middle of the channel for all devices. The data show that the charge difference is not significant between various NWTs

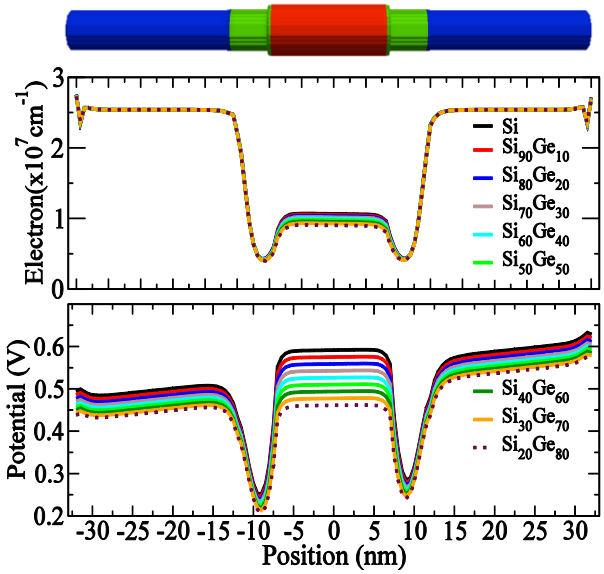

Fig. 6 Electron concentration (top) and electrostatic potential (down) along the transport direction of Si_xGe_{1-x} NWTs at V_D=0.05 and V_G=0.6V. The concentration is obtained by integrating in the plane perpendicular to the transport direction.

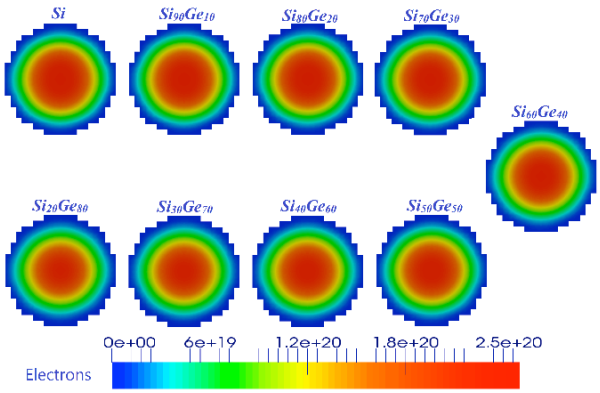

Fig. 7 2D charge distributions, in the middle of the channel, obtained for the Si_xGe_{1-x} NWTs with deferent Si/Ge concentration.

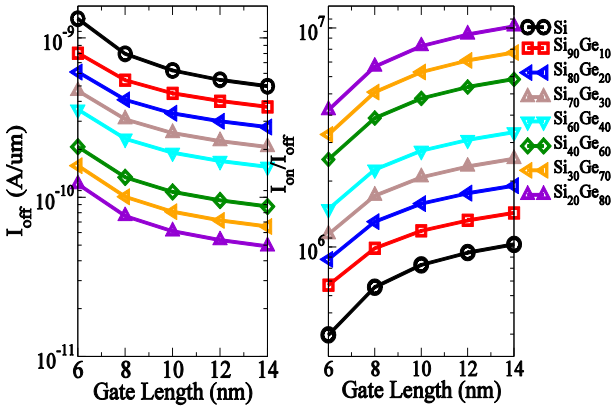

Fig. 8 The impact of different molar ratio of Si and Ge on I_{on}/I_{off} (right) and on the leakage current I_{off} (left).

and the quantum simulations capture the well-known volume inversion effects.

Fig 8 reveals the impact of channel length on I_{off} at low drain voltage V_D=0.05V and gate voltage V_G=0.6V for the Silicon NWTs in addition to seven different Si_xGe_{1-x} molar fraction. As it is expected reducing the channel length leads to decrease in the leakage current for all simulated devices. Additionally, increasing the *Ge* concentration in the channel reduces the leaked current as wll. For example, silicon channel with 14 nm gate length has the worst I_{off} around $5x10^{-10}$ A/μm while $Si_{20}Ge_{80}$ shows the lowest (the best) leakage current about $5x10^{-11}$ A/μm for the same gate bias and and gate length. The right hand side of Fig. 8 shows the impact of channel length on I_{on}/I_{off} which has a positive effect on the device performance.

Similarly, to the discussion in the above, the $Si_{20}Ge_{80}$ devices show the best Ion/Ioff performance in comparison to all other wires. For example at 14 nm gate length the Ion/Ioff ration for $Si_{20}Ge_{80}$ is around 10^7 while for the silicon transistor is just bellow 10^6. This ration decreases with decreasing of the channel length but more importantly the trend is consistent for all devices.

V. CONCULUTION

In this paper we have studied the impact of quantum mechanical effects on the electrostatic driven performance of Si_xGe_{1-x} NWTs at the sub 5-nm CMOS technology. By varying the *Si/Ge* molar fraction in NWTs, we have established a link between the quantum confinement effects and the electrostatics properties in those devices. We also discuss properties such as DIBL and sub threshold slop SS. Based on our computational experiments we can conclude that the NTW with $Si_{20}Ge_{80}$ molecular share has the highest Q_M/C_G ratio, the lowest DIBL and sub threshold slop (SS), which makes it the best choice from all investigated devices.

VI. REFERANCES

[1] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Transactions on Electron Devices*, vol. 59, pp. 1813 - 1828, 16 May 2012.

[2] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi*, et al.*, "High-performance fully depleted silicon nanowire (diameter < 5 nm) gate-all-around CMOS devices," *Electron Device Letters, IEEE,* vol. 27, pp. 383-386, 2006.

[3] W. Lu, P. Xie, and C. M. Lieber, "Nanowire Transistor Performance Limits and Applications," *IEEE Transactions on Electron Devices,* vol. 55, pp. 2859-2876, Nov. 2008.

[4] E. G. Marin, F. J. G. Ruiz, and I. M. Tienda-Luna, "Analytical Gate Capacitance Modeling of III–V Nanowire Transistors," *IEEE Transactions on Electron Devices,* vol. 60, pp. 1590 - 1599, 02 April 2013 2013.

[5] H. Takeda and N. Mori, "Three-dimensional quantum transport simulation of ultra-small FinFETs," in *Computational Electronics, 2004. IWCE-10 2004. Abstracts. 10th International Workshop on*, 2004, pp. 91-92.

[6] Y. Yamada, H. Tsuchiya, and M. Ogawa, "Quantum Transport Simulation of Silicon-Nanowire Transistors Based on Direct Solution Approach of the Wigner Transport Equation," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 1396-1401, 2009.

[7] S. Sung Dae, L. Sung-Young, K. Sung-Min, Y. Eun-Jung, M.-S. Kim, L. Ming*, et al.*, "High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : fabrication on bulk si wafer, characteristics, and reliability," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 717-720.

[8] G. Chindalore, S. A. Hareland, S. A. Jallepalli, A. F. Tasch, C. M. Maziar, V. K. F. Chia*, et al.*, "Experimental determination of threshold voltage shifts due to quantum mechanical effects in MOS electron and hole inversion layers," *Electron Device Letters, IEEE,* vol. 18, pp. 206-208, 1997.

[9] V. P. Georgiev, E. A. Towie, and A. Asenov, "Impact of Precisely Positioned Dopants on the Performance of an Ultimate Silicon Nanowire Transistor: A Full Three-Dimensional NEGF Simulation Study," *IEEE Transactions on Electron Devices,* vol. 60, pp. 965-971, Mar 2013.

[10] S. U. Z. Khan and M. S. Hossain, "Impact of high-κ gate dielectric and other physical parameters on the electrostatics and threshold voltage of long channel gate-all-around nanowire transistor," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields,* vol. 28, pp. 389–403, 8 SEP 2014 2015.

[11] M. Bescond, "Quantum transport in semiconductor nanowires," in *Semiconductor Nanowires: Material, Synthesis, Characterization and Applications*, ed: Woodhead Publishing, 2015.

[12] J.-W. Lee and H.-M. Chou, "Silicon-Germanium Structure in Surrounding-Gate Strained Silicon Nanowire Field Effect Transistors," *Journal of Computational Electronics*, vol. 3, pp. 251-255, October 2004.

[13] D. Wang, Q. Wang, and A. Javey, "Germanium nanowire field-effect transistors with SiO_2 and high-k HfO_2 gate dielectrics," *Applied Physics Letters,* vol. 83, pp. 2432-2434, 22 September 2003.

[14] T. Al-Ameri, V. Georgiev, F. Adamu-Lema, X. Wang, and A. Asenov, "Correlation Between Gate Length, Geometry and Electrostatic Driven Performance in Ultra-Scaled Silicon Nanowire Transistors," in IEEE Nanotechnology Materials and Devices Conference (NMDC), 2015, pp. 23-27.

[15] "http://www.GoldStandardSimulations.com."

[16] Y. Wang and *et al.*, "Simulation Study of the Impact of Quantum Confinement on the Electrostatically Driven Performance of N-type Nanowire Transistors," *IEEE Transactions on Electron Devices*, vol. 62, pp. 3229 - 3236, 2015