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Perspective

Multiple facets of tightly coupled transducer–transistor structures

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Abstract
The ever increasing demand for data processing requires different paradigms for electronics. Excellent performance capabilities such as low power and high speed in electronics can be attained through several factors including using functional materials, which sometimes acquire superior electronic properties. The transduction-based transistor switching mechanism is one such possibility, which exploits the change in electrical properties of the transducer as a function of a mechanically induced deformation. Originally developed for deformation sensors, the technique is now moving to the centre stage of the electronic industry as the basis for new transistor concepts to circumvent the gate voltage bottleneck in transistor miniaturization. In issue 37 of *Nanotechnology*, Chang *et al* show the piezoelectronic transistor (PET), which uses a fast, low-power mechanical transduction mechanism to propagate an input gate voltage signal into an output resistance modulation. The findings by *Chang et al* will spur further research into piezoelectric scaling, and the PET fabrication techniques needed to advance this type of device in the future.

Keywords: piezoresistive, piezoelectric, transduction method

(Some figures may appear in colour only in the online journal)

Power and speed are the burning issues in modern very large scale integration (VLSI) that have led researchers to explore many innovative techniques, including hybrid transistor structures and reduced operating voltages. Traditional complementary metal–oxide–semiconductor (CMOS) transistors fundamentally require around half a volt to operate as a switch, and the rest goes to the interconnects to overcome noise and communication. A significant amount of power is eaten up by interconnects, as they are charged to a high voltage [1]. The issue is likely to take on a new dimension with new technologies such as flexible or bendable electronics [2]. For example, stress-induced changes in mobility of charge carriers will pose new challenges.

Hybrid transistor structures with new material layers in conventional transistors have been explored for a long time to overcome the above challenges and to develop new applications such as solid-state sensors. Figure 1 shows some of the schemes where additional transducer material layers (e.g. piezoresistive (PR), piezoelectric (PE), capacitive, optical, and pressure conductive rubber etc) have been used to modulate channel current as a result of an applied electrical or physical stimulus. These structures can overcome the energy-efficiency limits of CMOS devices and offer advantages in terms of low power and high speed, due partly to the mechanical tension in the transducer material. The pressure-

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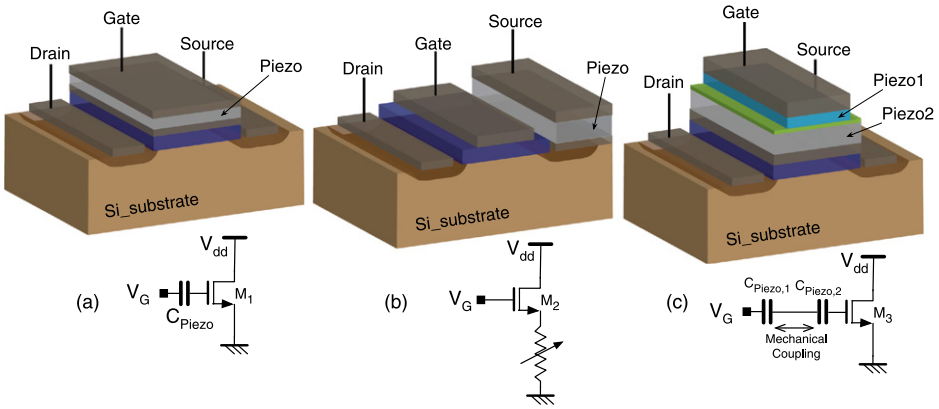

Figure 1. Concept of transistors with tightly coupled transistors. (a) A single piezoelectric layer on the gate region of a FET transistor used in POSFET and FeRAM. (b) A single piezoelectric or pressure conductive layer on the source region. (c) Two piezoelectric layers used in PET include mechanically-coupled but electrically-distinct actuator and switch elements.

modulated channel is the key factor in terms of low power as it prevents using constant gate voltage and thus reduces the leakage current. This also creates an inherent advantage in terms of low ON electrical resistance, which potentially reduces the time constant and hence raises the speed. Further, piezoelectric transducers with substrates such as the one provided by the material used in the transistor can have a response time of the order of nanoseconds [3]. Some examples of such devices include piezoelectric oxide field-effect transistor (POSFET) [4–6], carbon-nanotube field-effect transistors (CNFET) [7], tunnel field-effect transistors (TFET) [8], graphene-based field-effect transistors [9], FinFET [10], and ferroelectric random access memory (FeRAM) [11]. The new material layer is used in these devices to tailor or tune some of the device characteristics. For example, the piezoresistive or piezoelectric transducer layers on the gate of transistors help reduce the voltage needed for switching as a low-power CMOS-compatible voltage transformer [12, 13]. Apart from utilizing piezoresistive and piezoelectric materials for developing low-power or even self-powered devices, the integrated piezoelectric polymers can also be used to construct flexible and conformable devices for e-skin applications [14]. It is worth noting that these materials are not always compatible with Si-based technology and often require new strategies to ensure compatibility. For example, piezoelectric materials on the gate area of a transistor require the application of a high voltage to orient the dipole in the material. The high voltage is detrimental as there is a risk of damaging the circuitry underneath. Further, there are challenges related to charge leakage. With the next technology nodes, appearing in the most recent International Technology Roadmap for Semiconductors (ITRS), the new layers of material within the transistor structures will be challenging.

Adding to this list of transistors with a tightly coupled transducer layer is the work on piezoelectronic transistor (PET) by Chang *et al* [15], with a similar structure as reported by other researchers [16–18]. In the case of PET the mechanical stress is used to trigger an insulator–metal transition (IMT) generating the output. An input gate voltage expands the piezoelectric layer, which then results in the application of pressure on the piezoresistive later and ultimately modulating the channel current. For the 5 nm technology node, compared to a FinFET running at 0.8 V, a PET could potentially switch at 20× lower power for a VDD of 0.14 V, and 50× lower power for a VDD of 0.1 V [19].

In issue 37 of *Nanotechnology*, Chang *et al* present the first realization of the stand-alone integrated PET and addressed the processing challenges associated with its fabrication and also made a surrounding cage against which the system can be suspended and compressed [15]. To overcome the problem of the

fabrication of a nanoscale pillar of piezoresistive material, the authors used a hard metal nail to indent a large area piezoresistive film. The authors explored an innovative device structure, which has allowed fabricating a fully integrated PET including PZT ($PbZr_{0.52}Ti_{0.48}O_3$) PE and SmSe (Samarium monochalcogenides) PR elements held together by a drum clamp suspended over an air-gap. They propose, simulate, fabricate and measure a novel device structure to enable PET device fabrication under realistic processing constraints. The paper by Chang *et al* is similar to others reported recently [12]. The authors introduced the processing challenges of integrating chemically incompatible piezoresistive and piezoelectric materials together within a surrounding cage against which the piezoresistive material is compressed. This proof-of-concept demonstration of a fully integrated, stand-alone PET device is a key step towards development of a fast, low-power VLSI technology.

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