

Multi-Subband Ensemble Monte Carlo Simulation of Si Nanowire MOSFETs

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Abstract—The need for an accurate simulation of non-planar devices such as FinFETs and nanowire based FETs, including a full quantum treatment of transversal two-dimensional confinement, motivated the development of a three-dimensional Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator. Here we describe the last improvements of such simulator including better convergence properties and statistical improvements for the computation of the drain current. The simulator is employed to study MOS devices based on Si nanowires with lateral sizes of a few nanometers. The results show the importance of a proper two-dimensional treatment of quantum confinement, which can be achieved with our simulator.

I. INTRODUCTION

Multi-Subband Ensemble Monte Carlo (MS-EMC) simulators have been extensively employed to study the behavior of planar devices, either traditional or SOI based MOSFETs [1], [2], [3]. This approach considers a semi-classical transport description while taking into account quantum confinement by solving the one-dimensional Schrödinger equation on different slices of the device along the transport direction. Compared to full quantum methods such as Non Equilibrium Green's Functions it allows a lower computational cost and an accurate and straightforward treatment of the scattering mechanisms. In principle, MS-EMC simulators do not take into account directly quantum effects in the transport direction such as tunneling; however, they can be added separately [4], [5].

Nowadays, three-dimensional devices with two-dimensional carrier confinement are of special interest for the optimization of upcoming CMOS technological generations: FinFETs, tri-gate or gate-all-around FETs. However, the existing Multi-Subband tools can only afford the study of planar devices. Non-planar structures are usually simulated employing quantum corrected approaches (such as Density Gradient) which need a proper calibration, or by assuming that the height of a FinFET is much larger than its width so that a planar approximation with a double-gate structure can be employed. In any case, for channels with a very small cross section, a fully quantum two-dimensional treatment is mandatory and therefore both approaches are not suitable. For this reason, we developed a MS-EMC simulator which couples the 2D solution of the Schrödinger equation in different device cross sections with the 3D solution of Poisson equation and 1D simulation of ballistic transport employing the Monte Carlo technique [6].

In this paper we first describe the 3D MS-EMC simulator we developed, then we employ it to study MOS devices based on $\langle 110 \rangle$ Si nanowires with lateral size in the range from 2 nm to 6 nm.

II. SIMULATOR DEVELOPMENT

The general structure of our simulator is the same as the existing Multi-Subband simulators [1], [2], [3]: solvers for the Poisson and Schrödinger equations are coupled to an Ensemble Monte Carlo simulator in order to achieve a self-consistent solution. The difference and the increased complexity given by three-dimensional device structures deal with the dimensionality of the problem: a 3D Poisson equation is needed, the device cross sections in which Schrödinger equation is solved are 2D and, finally, the transport is reduced to 1D [6]. After a self-consistent state is reached, a steady state simulation is performed to compute the drain current: it runs until the estimated error of the current is below an user-specified limit.

To improve the convergence properties of the self-consistent Schrödinger-Poisson-Monte Carlo loop, we implemented an adaptive damping scheme that uses a heuristic method to adjust the relaxation parameter. The potential computed by solving the Poisson equation is not fed directly to the Schrödinger equation; instead, the difference between the potential and its “old” value from the previous iteration is multiplied by a dynamically computed factor and then added to the “old” potential. Thus, if we denote $\bar{\varphi}_{i,j,k,n}$ the “corrected” potential at step n for mesh point i, j, k and $\varphi_{i,j,k,n}$ the solution of Poisson equation at step n , we have:

$$\bar{\varphi}_{i,j,k,n} = \bar{\varphi}_{i,j,k,n-1} + u_n(\varphi_{i,j,k,n} - \bar{\varphi}_{i,j,k,n-1}) \quad (1)$$

The fractional update parameter, u_n , is computed as:

$$u_n = \left. \frac{u_{n-1}}{1 - \Delta_{n-1}/\Delta_{n-2}} \right]_{u_{\min}}^{u_{\max}} \quad (2)$$

where $\Delta_n = \max_{i,j,k}(\varphi_{i,j,k,n} - \bar{\varphi}_{i,j,k,n-1})$ and the value of u_n is restricted to a range $[u_{\min}, u_{\max}]$ specified by the user. In this way, the convergence to a self-consistent state is both faster and more robust.

Then, to improve the MC statistics for the sub-threshold regime of the transistor without an unnecessary increase of the number of simulated particles, we employed a variance

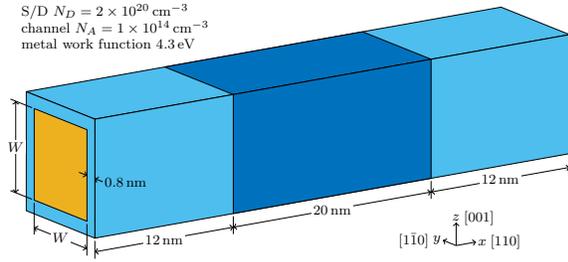


Fig. 1. Structure of the simulated devices.

reduction technique [7] with non-uniform weights for the simulated super-particles depending on the total energy. For each subband, an energy limit, based on the height of the barrier, is chosen; then the weights of the low- and high-energy particles are computed to obtain a given number of particles in the whole device. Since the transport is ballistic, the total energy of a particle is constant so there is no need for particle splitting, merging, or re-sampling.

Finally, we employed a parallel eigenvalue solver for Schrödinger equation in the 2D device cross sections, which is the computationally most expensive portion of the approach, especially for the larger devices. Parallelization of the Monte Carlo part is planned as the next step.

III. DEVICE STRUCTURE AND RESULTS

The structure of the simulated devices is shown in Figure 1: Si nanowires with square cross section W between 2 nm and 6 nm and gate length $L_g = 20$ nm. The channel is oriented along the $[110]$ crystallographic direction (x axis) and the lateral sides are along $[1\bar{1}0]$ and $[100]$ directions (y and z axis, respectively). The thickness of the SiO_2 oxide is $T_{ox} = 0.8$ nm, the doping density is $N_D = 2 \times 10^{20} \text{ cm}^{-3}$ in the source and drain regions (with Gaussian profile) and $N_A = 1 \times 10^{14} \text{ cm}^{-3}$ in the channel; the metal gate work function is 4.3 eV. We simulated ballistic I_D - V_G curves with $V_S = 0$, $V_D = 50$ mV and V_G in the range 0.1 V to 0.7 V.

Figure 2 shows the electron distribution in different cross sections in the middle of the channel or near the source contact. For the wider device ($W = 6$ nm) and low bias the charge is essentially confined to the center of the nanowire; only at high values of V_G the carrier concentration peak splits and the highest charge density is obtained near the top and bottom interfaces (Figure 2(e)). This anisotropy can be explained by examining the contributions of the 6 conduction valleys of Si, whose degeneracy is broken by confinement into a 4-fold (Δ_4) and a 2-fold (Δ_2) sets (Figure 3) with different masses m_y and m_z . Due to these masses, electrons in Δ_2 valleys are expected to be closer to the top and bottom sides of the nanowire, while those in Δ_4 valleys tend to stay closer to the lateral sides. Due to the larger confinement masses, Δ_2 valleys have, in general, lower energy sub-bands and, as a consequence, a larger population. Therefore, the charge peaks are located near the top and bottom Si/SiO₂ interfaces (Figure 2(e)). However, in the source and drain regions, for

$W = 6$ nm the sub-band energy difference is quite small, so that the larger degeneracy compensates for this and the population of Δ_4 and Δ_2 valleys is approximately the same. Indeed, in Figure 2(f), we can see that in this case the electron charge is distributed near the whole perimeter of the nanowire with peaks corresponding to the corners.

On the contrary, for the $W = 3$ nm device, the charge is always located at the center of the channel, as we can see in Figures 2(a), (b), and (c): quantum effects keep the mobile charge away from the silicon-insulator barrier for both Δ_4 and Δ_2 valleys. The electric field from the gate (for realistic values of the gate bias for the considered oxide thickness) cannot overcome such repulsion produced by quantum confinement.

The use of the aforementioned weighting scheme based on the total energy of the super-particles allows us to obtain reasonable low levels of statistical noise in the sub-threshold region of all the considered devices for currents as low as $1 \times 10^{-4} \mu\text{A}$, with a number of simulated particles in the device $N_p = 5 \times 10^4$ regardless of the applied bias (Figure 4). The simulation time (after self-consistency is reached) needed to achieve the results shown in Figure 4 depends on the device size and applied bias: it ranges from 30 ps for the highest gate bias to 1 ns for the widest device at $V_G = 0.1$ V.

An almost ideal electrostatic behavior is obtained, as expected for gate-all-around devices with a lateral size in the order of a few nanometers and an oxide thickness of 0.8 nm. Indeed, the fitted values of the sub-threshold swing range from ~ 62 mV/dec for the narrowest device ($W = 2$ nm) to ~ 68 mV/dec for the widest one ($W = 6$ nm). By comparing the I_D - V_G curves of Figure 4, we can observe an increase of the threshold voltage V_t as the nanowire width decreases. This observation can be quantified by computing the value of V_t for each curve by locating the maximum of the second derivative of I_D as a function of V_G . The results are shown in Figure 5, where a strong increase of V_t can be observed for small values of W due to quantum confinement effects: as the device cross section shrinks, the quantized sub-band levels raise. If we represent I_D as a function of the overdrive voltage, $V_G - V_t$, as in Figure 6(a), we can see that the curves corresponding to the nanowires up to $W = 4$ nm collapse. This means that, for these structures, the current is almost independent of the nanowire size, and it only depends on the applied overdrive voltage. This is confirmed by the inset of Figure 5 where the current corresponding to $V_G = V_t$ is plotted as a function of the nanowire lateral size. We can observe that such current is almost constant up to $W = 4$ nm: this agrees with the fact that for thinner nanowires the charge is not distributed along the nanowire sides, but it is accumulated only near the center. On the contrary, for the wider nanowires the current I_D grows with the nanowire size; as one would expect when the charge distribution is located along the nanowire sides. Indeed, when I_D is normalized by the nanowire perimeter ($4W$) as in Figure 6(b) we can see that the curves corresponding to the wider nanowires (4 nm, 5 nm and 6 nm) are now collapsing, contrarily to the previous case. This behavior is also confirmed by the inset of Figure 5: for the larger values of W the current

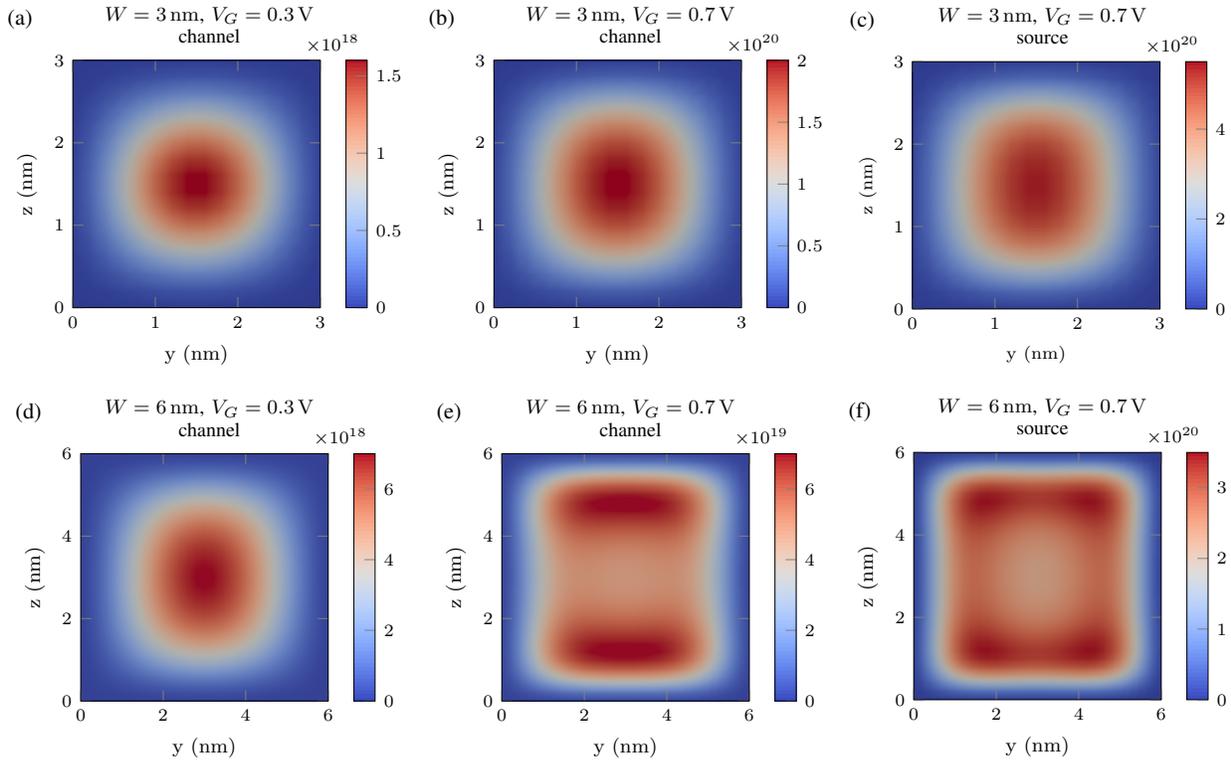


Fig. 2. Charge distribution (in cm^{-3}) in device cross sections for two different nanowire widths — 3 nm for (a), (b), and (c), 6 nm for (d), (e), and (f) — and two different applied biases — 0.3 V for (a) and (d), 0.6 V for (b), (c), (e), and (f). In (a), (b), (d), and (e) the cross section is taken in the middle of the channel, while (c) and (f) are in the source.

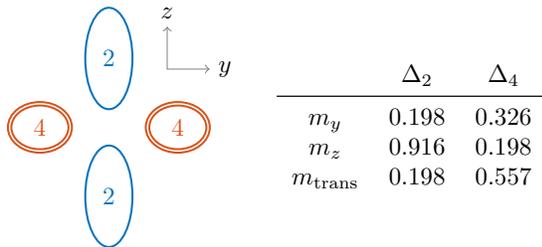


Fig. 3. Energy ellipsoids for the different sets of equivalent valleys in the confinement plane, with the corresponding effective masses [8] in units of the free electron mass.

is (approximately) proportional to W .

IV. CONCLUSION

This paper describes the improvements in our ballistic MS-EMC simulator for 3D devices and shows the results obtained for $\langle 110 \rangle$ square Si nanowire devices, highlighting the importance of a full quantum description in the device cross section plane. Quantum confinement effects play a major role in devices with dimensions such as the ones considered in this paper: a transition is observed between two regimes where, depending on the nanowire lateral size, the charge can

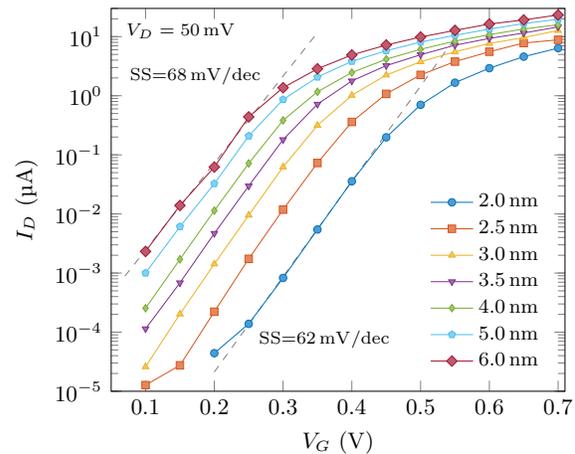


Fig. 4. I_D - V_G curves for different nanowire widths. The dashed lines show the sub-threshold slope for the widest and the thinnest devices.

be considered distributed along the channel sides or only in its center.

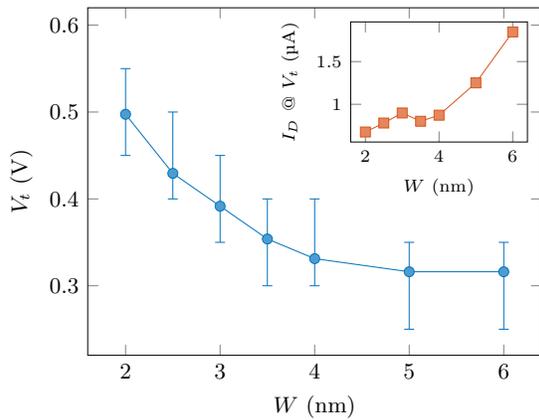


Fig. 5. Threshold voltage V_t as a function of nanowire width. The inset shows the corresponding values of the current I_D evaluated at $V_G = V_t$.

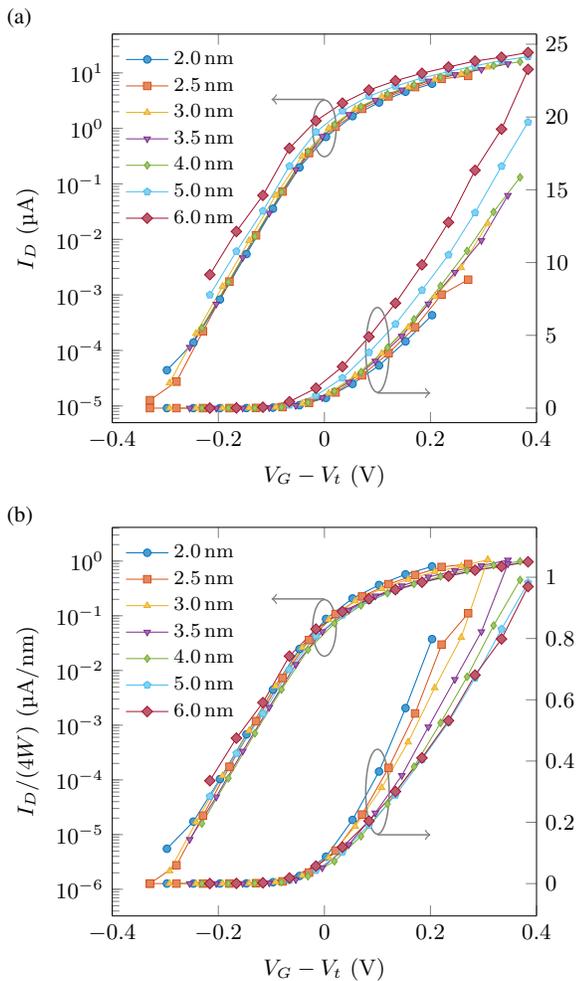


Fig. 6. (a) Drain current and (b) drain current normalized by nanowire perimeter, plotted as a function of gate overdrive $V_G - V_t$.

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