Simulation Study of the Impact of Quantum Confinement on the Electrostatically Driven Performance of n-type Nanowire Transistors

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***Abstract*— In this paper, we have studied the impact of quantum confinement on the performance of n-type silicon nanowire transistors (NWTs) for application in advanced CMOS technologies. The 3-D drift-diffusion simulations based on the density gradient approach that has been calibrated with respect to the solution of the Schrödinger equation in 2-D cross sections along the direction of the transport are presented. The simulated NWTs have cross sections and dimensional characteristics representative of the transistors expected at a 7-nm CMOS technology. Different gate lengths, cross-sectional shapes, spacer thicknesses, and doping steepness were considered. We have studied the impact of the quantum corrections on the gate capacitance, mobile charge in the channel, drain-induced barrier lowering, and subthreshold slope. The mobile charge to gate capacitance ratio, which is an indicator of the intrinsic speed of the NWTs, is also investigated. We have also estimated the optimal gate length for different NWT design conditions.**

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***Index Terms*— CMOS, electrostatics, nanowire transistors (NWs), performance, quantum effects, TCAD.**

I. Introduction

PROBLEMS with the oxide thickness and doping-controlled electrostatic integrity of conventional bulk CMOS transistors have prompted interest in thin-body and 3-D transistor architectures, which have improved electrostatic control resulting in steeper subthreshold slope (SS), reduced drain-induced barrier lowering (DIBL), and, therefore, reduced channel leakage compared with bulk transistors [1]–[10]. Tolerance to low channel doping additionally boosts mobility and performance and reduces local (statistical) variability [11]–[16]. This research and corresponding technology development has culminated in the introduction of 28-nm fully depleted silicon-on-insulator (FDSOI) CMOS by STMicroelectronics [17] and 22- and 14-nm FinFET CMOS by Intel [18] and Samsung [19]. It has been speculated that the scalability of FDSOI can extend planar CMOS technology down to 10 nm [20], and FinFETs can extend CMOS technology down to 7 nm [21]. Even better electrostatic integrity, offered by gate-all-around nanowire transistor (NWT) architectures [8]–[10] may be needed to extend CMOS scaling beyond the 7-nm mark [22].

Quantum mechanical effects play a critical role in confined channels, including bulk, FDSOI, FinFET, and NWTs [23]–[25]. The confinement effects introduce a threshold voltage shift, simultaneously reducing the gate-to-channel capacitance and the charge in the channel available for transport [26], [27]. The reduced gate-to-channel capacitance also adversely affects the electrostatic integrity. The impact of the above effects increases with the reduction of the characteristic confined dimensions and, therefore, will play a critical role in the simulation-based research and design of a sub-7-nm NWT-based CMOS technology. Although significant research has been published in recent years on the simulation of quantum confinement effect in the NWTs [28]–[31], in this paper, we comprehensively study and compare the quantum confinement effects in the NWTs suitable for sub-7-nm CMOS applications with different cross sections. The results of Poisson–Schrödinger (PS) and density gradient (DG)-based

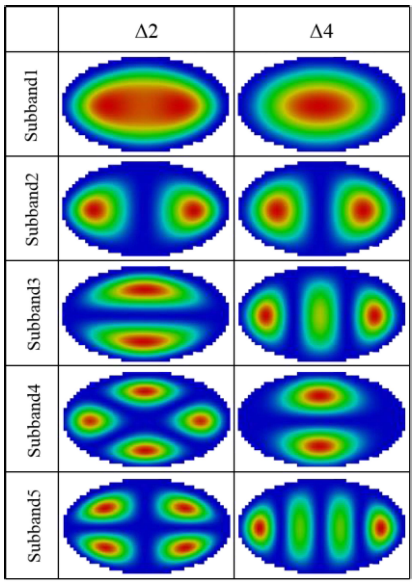


Fig. 1. Wave functions in the twofold and fourfold degenerate valley in the cross section of an elliptical Si NWT.

quantum corrections are carefully compared to assess the applicability of the DG approach in the simulation and design of NWTs. We also systematically study and compare the impact of the nanowire cross-sectional shape on the gate capacitance, charge available for transport, SS, and DIBL of the simulated NWTs. Finally, the optimization of the configurations of the nanowires is given.

This paper is organized as follows: After the introduction, in Section II, we describe the simulation methodology and the NWT design used in this paper. Section III investigates the impact of the quantum confinement on the gate capacitances and the charge available for transport in the channel in comparison with classical DD simulations. The impact of the quantum confinement on the nanowire electrostatic integrity, including the SS and DIBL, is investigated in Section IV. In Section V, we study the impact of different source/drain (S/D) doping designs on the optimal gate length for different NWT cross sections before drawing the conclusions in Section VI.

II. Simulation Methodology

A. Poisson–Schrödinger Quantum Corrections

All simulations are executed with the Gold Standard Simulations 3-D TCAD simulator GARAND [32], in which quantum corrections in the DD modules can be based on the 2-D solution of the Schrödinger equation in 2-D cross-sectional slices along the gate length of the simulated 3-D transistors, within which nonparabolicity has not been captured. The 2-D Schrödinger equation in effective mass approximation [33] is discretized and solved using a LAPACK solver [34]. The wave function penetration in the gate oxide is considered. The wave functions in the twofold ($\Delta 2$) and fourfold ($\Delta 4$) degenerate valleys in the cross section of an elliptical Si NWT at gate bias of 0.65 V are shown in Fig. 1. The description of the corresponding NWT is provided in Section II-B. The PS model is coupled with the DD solution. Initially, the DD simulation is carried out until convergence, and then the quasi-Fermi level from the converged DD solution is used as a fixed reference for PS solution. The effective quantum-corrected potential is used as the driving potential in the solution of the current-continuity equation, keeping the charge distribution in the NWT cross section identical to the charge distribution obtained from the solution of the Schrödinger equation.

B. Simulated Nanowire Transistor

The NWTs simulated in this paper have a generic structure and design parameters, as shown in Fig. 2. All results, in this paper, are from the n-type NWTs. The simulated NWTs have different cross-sectional shapes, as shown in Fig. 3, but an identical cross-sectional area of 44 nm^2. Simple doping profiles with a Gaussian roll-off and different steepness are implemented. An undoped channel with a residual doping of 10^{14} cm^{-3} is assumed. Fig. 3 shows the classical, PS, and DG charge distributions at $V_G = 0.65$ V for the nanowires with different cross-sectional shapes. It can be seen that quantum simulations with both the PS and the DG capture the well-known volume inversion effect [35]. Note that the asymmetry in the charge distribution along the two main axes of the cross sections in Fig. 3 is due to the fact that the transport direction is lying along the crystallographic orientation $\langle 110 \rangle$.

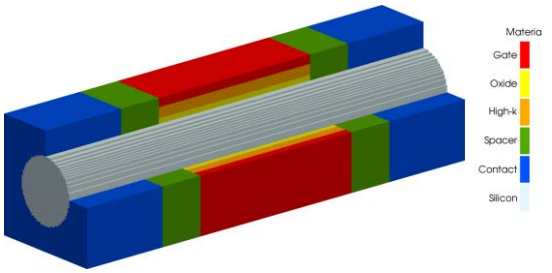
C. Density Gradient Calibration

Although the PS quantum corrections provide very accurate quantum charge distribution in the channel of the simulated NWTs, the large number of cross-sectional solutions of the Schrödinger equation significantly slows the simulations and reducing efficiency and productivity. Therefore, a compromise solution will be to calibrate the DG quantum corrections [36] to the PS charge distribution and then use the DG simulations. Although other techniques, such as MLDA [37], have been proposed in the literature and are available in other commercial software [38], a comparison of the several simulation models is outside the scope of this paper. The DG formalism introduces an additional quantum correction term, ψ_{qm}, which is proportional to the second derivative of the square root of the carrier density

$$\psi_{qm} = 2b_n \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} = \phi_n - \psi + \frac{k_B T}{q} \ln\left(\frac{n}{n_i}\right) \tag{1}$$

where $b_n = \hbar^2/12qm_n$. The DG equation is calibrated against quantum-mechanical simulations based on a PS solution by considering a tensorial effective mass, whose components are used as fitting parameters. By substitution of the effective mass components m_x, m_y, and m_z in the principle tensor directions into (1) as

$$\frac{2b_n}{S}\left(\frac{1}{m_x}\frac{\partial^2 S}{\partial x^2} + \frac{1}{m_y}\frac{\partial^2 S}{\partial y^2} + \frac{1}{m_z}\frac{\partial^2 S}{\partial z^2}\right) = \phi_n - \psi + \frac{k_B T}{q} \ln\left(\frac{S^2}{n_i}\right) \tag{2}$$



$T_{interfacial\ layer}$, $T_{high\text{-}k}$ (nm)	0.6, 1.2
Gate length (nm)	10-24
Spacer thickness (nm)	3.0, 5.0
S/D peak doping (cm^{-3})	2×10^{20}
Doping roll-off (nm/dec)	1.0, 1.5, 2.0
Channel doping (cm^{-3})	10^{14}
Substrate orientation	(001)
Nanowire orientation	<110>

Fig. 2. (left) Schematic view and (right) design parameters of the simulated NWTs.

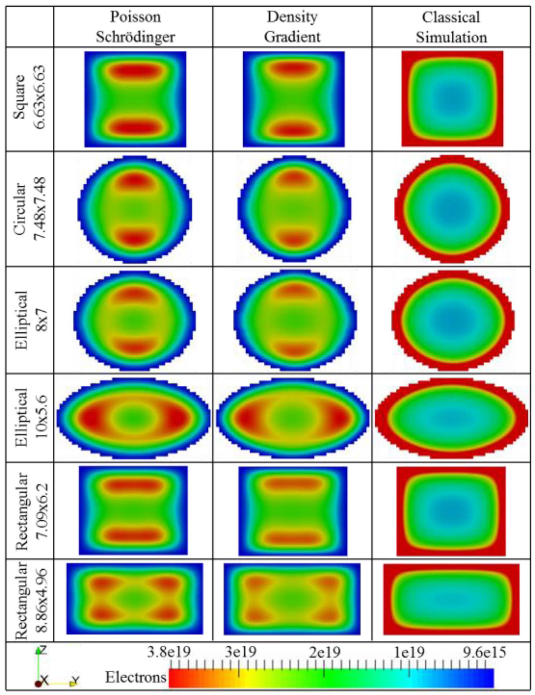


Fig. 3. Different NWT cross sections simulated in this paper. Comparison of the charge distribution in the nanowire cross section obtained from the PS, DG, and classical DD simulations at $V_g = 0.65$ V.

where $b_n = \hbar^2/12q$, and we solve for $S = \sqrt{n}$. The electron density penetration as a function of distance x, from the Si/SiO_2 interface can be approximated as

$$n(x) = n(0)\exp(-2x/x_p) \tag{3}$$

where $n(0)$ is the electron density at the interface, and x_p, given by $x_p = \hbar/(2m^*_{ox}\Phi_B)^{1/2}$ is the characteristic penetration depth obtained from the Wentzel–Kramers–Brillouin approximation. Here, m^*_{ox} is the electron effective mass within the oxide, and Φ_B is the potential barrier of the oxide. Using (3), the outward normal component of $b_n\nabla S$ at the Si/SiO_2 interface can be written as $\mathbf{n}\cdot b_n\nabla S = -(b_{ox}/x_p)S$, where b_{ox} is given by $b_{ox} = (\hbar^2/12qm_{ox})$. The oxide masses are used to define the boundary conditions between the semiconductor and the insulator. The relative value of the semiconductor and oxide masses defines a gradient for the solution variable, S, that is imposed at the semiconductor/insulator boundaries. This information along with other details about the DG model employed in this paper are presented in great detail in [36]. The DG effective masses for the conduction band in silicon and the oxide masses are calibrated to fit the charge distributions obtained from the PS solutions along the major axis and the minor axis of the NWT cross section and the integrated mobile charge in the channel at a gate voltage of 0.65 V. This procedure is automated by Enigma [39], which employs a trust region optimizer with the objective function formulated as a pointwise least squares across the channel region. It should be noted that the orientation dependence is captured by the PS solution. The DG effective masses are only fitting parameters. In addition, the quantum confinement is only applied perpendicular to the transport direction, and the DG effective mass along the transport is set at 0.5 m_e, which is large enough to avoid artificial S/D tunneling due to lowering of the barrier by the DG solution. On the other hand, the values of the effective masses in the interfacial layer and the high-k region are set to 0.22 m_e. For both the Poisson and the DG equations, there are Dirichlet boundary conditions on the Fermi level in the contacts. The potential and carrier concentrations for the respective equations have Neumann boundary conditions to allow them to respond to confinement effects coming from the quantum corrections. The Schrödinger equation has Dirichlet boundary conditions on the wave function at the outer edge of the confinement plane, which is set at the gate contact (the outer edge of the insulator region). In order to illustrate the calibration procedure for the DG parameters and make the results reproducible by others, the resulting fitting parameters of one example, the NW with circular cross section are specified. For Si conduction band, $m_x = 0.5$ m_e, $m_y = 0.11$ m_e, and $m_z = 0.9$ m_e; for the oxide, $m_x = 0.27$ m_e, $m_y = 0.001$ m_e, and $m_z = 0.1$ m_e.

A comparison of the charge distribution in the different NWT cross sections obtained from the PS, DG, and classical DD simulations is shown in Fig. 3. A better understanding of the accuracy of the calibration process can be gained from Fig. 4, which compares the 1-D charge distributions obtained from the PS and DG solutions along the principle diameters of the NWT cross section.

III. Nanowire Gate Capacitance and Charge

In this section, we study the impact of the quantum mechanical effects and NWT cross section on the gate voltage dependence of the gate capacitance for the cross sections, as shown in Fig. 3. To validate our simulation, a comparison with the experimental data [40] is first shown in Fig. 5. The permittivity of SiO_2 and HfO_2 employed in this work is 3.9

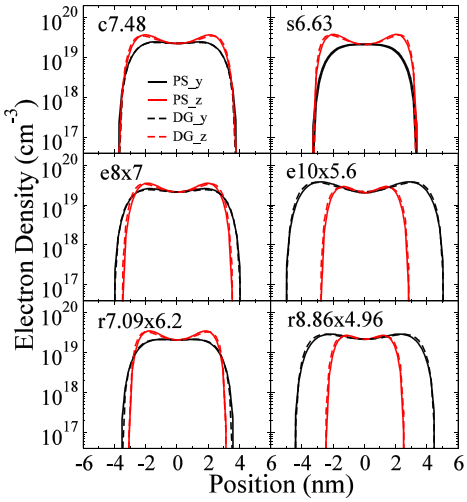


Fig. 4. 1-D charge distributions obtained from the PS and DG solutions along two of the diameters of the NWT cross section.

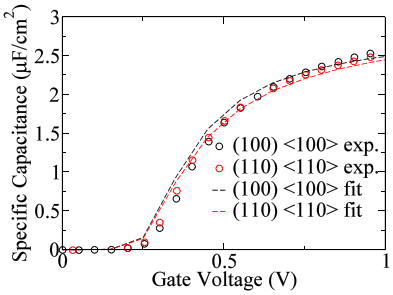


Fig. 5. Comparison between the experimental data and the PS-calibrated DG results of n-type SOI FinFET.

and 20, respectively. The work function is set at 4.48 eV. For the (100)⟨100⟩ orientation, $m_x = 0.5$ m$_e$, $m_y = 0.38$ m$_e$, and $m_z = 0.4$ m$_e$ for Si conduction band and $m_x = 0.27$ m$_e$, $m_y = 0.1$ m$_e$, and $m_z = 0.1$ m$_e$ for the oxide are used. For the (110)⟨110⟩ orientation, $m_x = 0.5$ m$_e$, $m_y = 0.125$ m$_e$, and $m_z = 0.4$ m$_e$ for Si conduction band and $m_x = 0.27$ m$_e$, $m_y = 0.1$ m$_e$, and $m_z = 0.1$ m$_e$ for the oxide are used. In order to highlight the impact of cross section on capacitance, an infinite gate length is assumed here. The capacitance–voltage (C–V) characteristics of the simulated NWT with different cross sections are shown in Fig. 6. It is clear that the quantum mechanical effects have impact on the gate capacitance. On average, the gate capacitance is reduced by 30% compared with the classical simulations. It is very important to notice that the impact of the quantum mechanical effects is different for different cross-sectional shapes even with identical cross-sectional area. As can be seen from Table I, the NWT with extended elliptical cross section (e10 × 5.6) has the largest gate capacitance. This is most likely due to the fact that the asymmetric spatial confinement induced by the elliptical shape compensates the (opposite) electrostatic confinement induced by the different quantum masses along the cross-sectional diameters, offering, therefore, a more uniform charge distribution that is more effectively controlled by the wrapped-around gate. The mobile charge in the channel

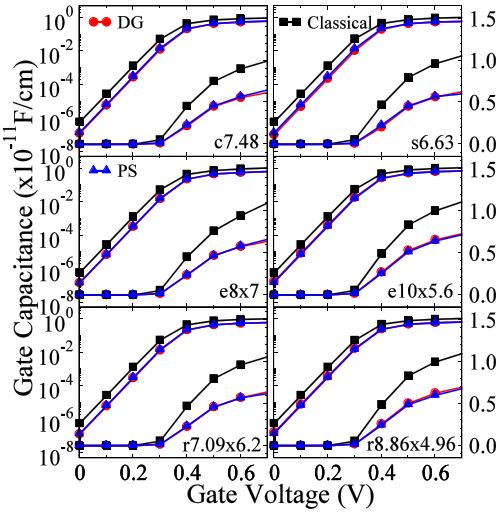


Fig. 6. C–V characteristics of the simulated NWT with different cross sections.

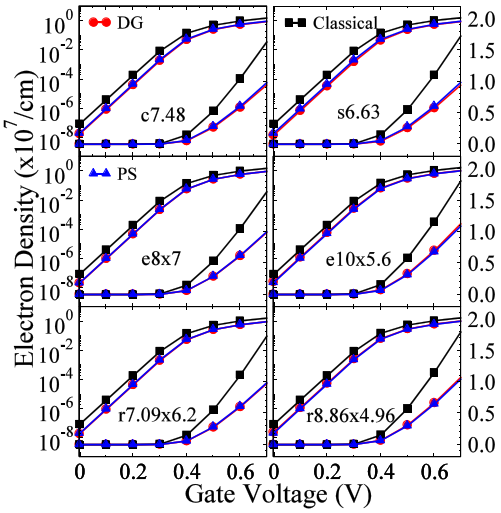


Fig. 7. Gate voltage dependence of the mobile charge in the channel for the NWT with different cross sections.

per-unit length Q_M at particular gate voltage V_G is directly proportional to the NWT gate capacitance per-unit length C_{G1} according to the approximated expression

$$Q_M = C_{G1}(V_G - V_T) \tag{4}$$

where V_T is the threshold voltage, and $V_G - V_T$ is the gate overdrive. Therefore, the reduction of the NWT gate capacitance reduces the mobile charge in the channel and, therefore, the transistor performance. It is also useful to notice that the accurately calibrated DG model very closely follows the PS results and, therefore, remains an efficient approach to account for quantum mechanical effects in the TCAD device simulations even in complex 3-D transistors. Fig. 7 shows the gate voltage dependence of the mobile charge in the channel for the NWTs, as shown in Fig. 3. Note that this is the mobile charge per-unit area estimated at low drain bias in the middle of the channel. As expected from (4), the reduction in the gate capacitance results in a reduction of the mobile

TABLE I

$Q_M(V_G = 0.65\ \text{V})$, C_G, AND Q_M/C_G RATIO AT IDENTICAL $Q_M(V_G = 0\ \text{V})$

	$Q_M(10^6/\text{cm})$	$C_G(10^{-12}\text{F/cm})$	$Q_M/C_G(10^{18}/\text{F})$
s6.63x6.63	7.208	5.915	1.219
c7.48x7.48	7.670	5.922	1.295
e8x7	8.229	6.171	1.334
e10x5.6	9.638	7.081	1.361
r7.09x6.2	7.971	6.130	1.300
r8.86x4.96	9.104	6.746	1.350
e5.6x10	6.771	6.312	1.073

charge in the channel, and, therefore, in a reduction in the expected NWT performance. As with the gate capacitance, the mobile charge for NWTs with identical cross-sectional area depends on the cross-sectional shape. In order to fairly evaluate the impact of the NWT shape on the potential performance, Table I compares $Q_M(V_G = 0.65\ \text{V})$ for identical $Q_M(V_G = 0.0\ \text{V})$. To make this comparison, the $Q_M(V_G)$ curves were aligned by changing the gate work function. Similar to what was seen for the gate capacitance, the structure e10×5.6 has the largest mobile charge in the channel. In Table I, we have added one more case compared with the NWT, as shown in Fig. 3, the structure e10×5.6 is in this case rotated by 90° (but retaining the original crystal orientation) and named e5.6 × 10. The 90° rotation of the best performing NWT results in a dramatic drop in $Q_M(V_G = 0.65\ \text{V})$ from 9.638×10^6/cm to 6.771×10^6/cm, which is ∼30% reduction in the performance. In this case, the asymmetric spatial confinement induced by the elliptical shape exacerbates the (likewise) electrostatic confinement induced by the different quantum masses along the cross-sectional diameters, giving a charge distribution that is concentrated along one of the two diameters and, therefore, less effectively controlled by the wrapped-around gate. We have also compared in Table I the Q_M/C_G ratio as an indicator for the intrinsic NWT speed. There is a correlation between Q_M and Q_M/C_G, which indicates the approximate nature of (1) and the need to evaluate both Q_M and C_G. Clearly, e10 × 5.6 is again the winner.

IV. IMPACT OF QM EFFECTS ON SS AND DIBL

The impact of the gate length on the DIBL, defined as $\Delta V_T/\Delta V_D$, and on the SS are shown in Fig. 8. There is relatively little difference in the electrostatic integrity between the NWTs with different cross sections with the circular nanowire c7.48 and the prolonged elliptical nanowire e10 × 5.6 performing slightly better than the others. It has to be pointed out that down to 10-nm gate length SS performance is comparable with the corresponding figures achieved by 22- and 14-nm FinFET CMOS technologies, whereas the DIBL performance is better. The quantum effects have less impact on the evaluation of DIBL and SS compared with the evaluation of Q_M and C_G, where the error is in the range of 30%. The gate length dependence of the error between the classical and the quantum mechanical estimate of DIBL and SS is shown in Fig. 8 (bottom). It is clear

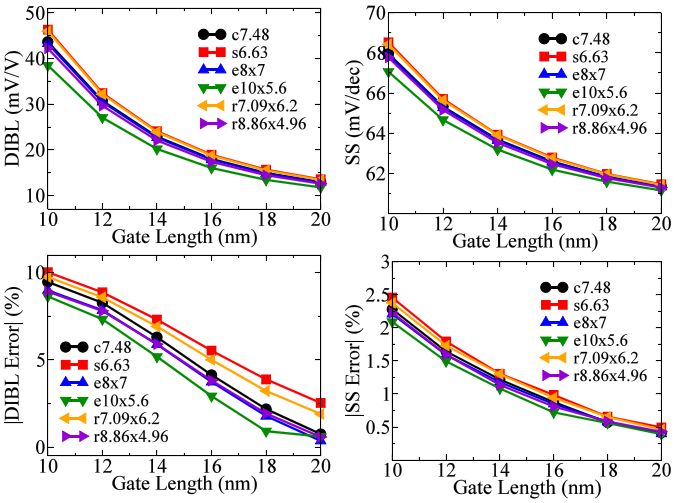


Fig. 8. Top: impact of the gate length on the DIBL and SS for NWT with different cross sections. Bottom: percentage error when using DD without quantum corrections for estimating DIBL and SS.

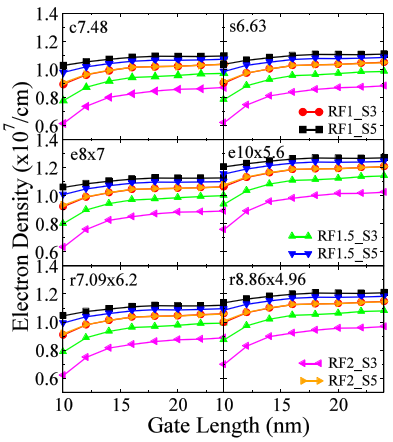


Fig. 9. Dependence of $Q_M(V_G = 0.65\ \text{V})$ on the gate length.

that in both the cases, the error is gate length dependent and increases with the reduction of the gate length. In the case of DIBL, the error increases from a few percent to approximately 10% when the gate length decreases from ∼20 to 10 nm. The corresponding error in the SS increases from ∼0.5% to ∼2.4%.

V. OPTIMAL GATE LENGTH

In this section, we investigate the optimal gate length, which delivers the maximum mobile charge in the channel $Q_M(V_G = 0.65\ \text{V})$ at fixed $Q_M(V_G = 0.0\ \text{V})$. This roughly corresponds to the best drive current at constant leakage. In this particular case, for each NWT with different cross sections, we have considered two different spacer thicknesses 3 and 5 nm and three different values of S/D doping steepness 1, 1.5, and 2 nm/decade. The position of the peak doping is at the edge between the S/D and the extension region. The dependence of $Q_M(V_G = 0.65\ \text{V})$ on the gate length is shown in Fig. 9, in which RF stands for doping roll-off, and S stands for spacer. It is clear that at larger gate lengths,

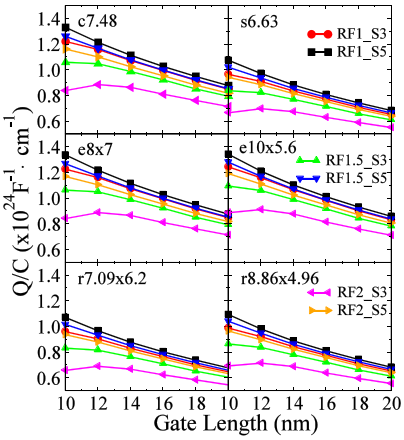


Fig. 10. Dependence of $Q_M/C_G(V_G = 0.65$ V) on the gate length.

larger spacers, and steeper doping roll-off, $Q_M(V_G = 0.65$ V) is flat, and at shorter gate lengths, $Q_M(V_G = 0.65$ V) is progressively reduced. It is, therefore, fair to conclude that the optimal gate length is the shortest possible gate length before $Q_M(V_G = 0.65$ V) starts to fall. This is based on the assumption that the shortest possible gate length, which sustains high $Q_M(V_G = 0.65$ V) will deliver the highest current due to better ballisticity. From this point of view, nanowires with the spacer thicknesses 5 nm and doping roll-off of 1 nm/decade can be scaled to approximately 16-nm gate length, while nanowires with the spacer thicknesses 3 nm and doping roll-off of 2 nm/decade cannot be scaled below 20-nm gate length. There are two potential pitfalls in this analysis. First, the gain from increased ballisticity with the reduction of the gate length can be bigger compared with the corresponding loss of electrostatic control. Second, the access resistance, which increases with the increase of the spacer thickness and with the increase of the doping steepness is not considered in this analysis. A more accurate analysis of the optimal nanowire gate length based on the EMC simulation will be presented in a follow up paper. This paper also neglects the impact of quantum tunneling between the source and the drain, but this should be negligible for lengths above 6 nm, as demonstrated by Non-Equilibrium Green's Functions simulations [41]. Finally, we investigate the $Q_M/C_G(V_G = 0.65$ V) ratio, which is a measurement for the intrinsic speed of the transistor depends on the gate length. The results of this investigation are shown in Fig. 10 for NWTs with different cross-sectional shapes. In the case of long spacer (5 nm) and steep doping roll-off (1 nm/decade), Q_M/C_G ratio increases monotonically with the reduction of the gate length. However, in the case of short spacer (3 nm) and large doping roll-off (2 nm/decade), the Q_M/C_G peaks at 12-nm gate length and then decreases due to the dominance of the gate fringing effects on the gate capacitance.

VI. Conclusion

We have successfully developed a 3-D quantum correction approach for DD simulations based on the solution of the Schrödinger equation in cross sections along the transport direction. We have demonstrated that after careful calibration against the PS results the DG approach can be used for practical 3-D simulations of NWTs. We have studied the impact of the quantum mechanical effect on the electrostatically driven performance of NWTs suitable for a 7-nm CMOS technology. We have demonstrated that the NWT shape has a strong impact on the gate capacitance and the mobile charge in the NWTs at high gate bias and that this impact strongly depends on the shape of the NWT cross section. The quantum mechanical confinement results in approximately 30% reduction in the mobile charge and in the gate capacitance. In particular, for the NWT with (001) substrate orientation and ⟨110⟩ nanowire orientation, the highest mobile charge for a given gate voltage overdrive is delivered by an elongated elliptical nanowire with the long diameter parallel to the silicon surface. We have also demonstrated that the quantum mechanical effects play a less important role in the subthreshold region modestly affecting the SS and the DIBL, although this impact increases with the reduction of the gate length. Finally, we have demonstrated that although the NWTs deliver excellent SS and DIBL down to 10-nm gate length, the optimal gate length depends on the spacer and the S/D doping profile design and is in the range of 14–22 nm for the chosen cross-sectional area, setting a lower boundary constraint for the minimum effectively printed gate length.

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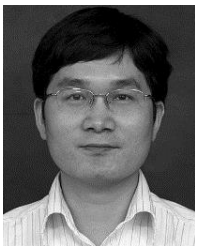

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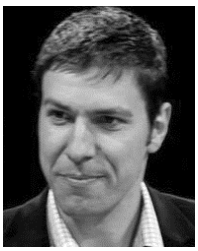

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