

Comparison of Si <100> and <110> crystal orientation nanowire transistor reliability using Poisson–Schrödinger and classical simulations

L. Gerrer ^{a,*}, V. Georgiev ^a, S.M. Amoroso ^b, E. Towie ^b, A. Asenov ^{a,b}

^a Device Modelling Group, Univ. of Glasgow, Rankine building, G12 8LT, UK

^b Gold Standard Simulation, Ltd., Oakfield Avenue, Glasgow, G12 8LT, UK



ARTICLE INFO

Article history:

Received 25 May 2015

Accepted 11 June 2015

Available online 2 September 2015

ABSTRACT

In this paper we perform trap sensitivity simulation analysis of square nanowire transistors (NWT), comparing Poisson–Schrödinger (PS) and classical solutions. Both approaches result in a very different electrostatic behaviour due to strong quantum confinement effects in ultra-scaled NWTs such as the Si NWTs presented in this work. Statistical distributions of traps are investigated, modelling the steady state impact of Random Telegraph Noise and Bias Temperature Instabilities for two crystal orientations. Statistical simulations are performed to evaluate the reliability impact on threshold voltage and ON current, emphasising the importance of both confinement and trap distribution details for the proper assessment of reliability in nanowire transistors.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

Aggressive downscaling of transistors in advanced CMOS technologies has reached dimensions at which the discreteness of charge and matter has to be carefully considered. Statistical variations due to single atom properties and positions in the critical regions of the transistors have to be taken into account to understand the significant increase in the dispersion of parameters of ultra-scaled transistors [1–3]. This led to the introduction of new transistor architectures such as FDSOI, FinFET, and nano-wire transistors, offering a better electrostatic control of the channel by the gate and allowing the reduction of channel doping, which is the dominant source of statistical variability [1,2,4].

The introduction of 3D transistor architectures offers additional design challenges due to the fact that side and top interface properties can differ as a result of the different crystal orientations [5]. Specifically for the <110> channel orientation, different interface roughness leads to different mobilities at the top and at the side interfaces of the transistor. Also the different symmetry of the band structure results in orientation dependent quantum confinement effects and therefore it is expected that the charge distribution and the transport properties are different for each crystal orientation. In addition atomic density, dangling bond density, and roughness are different and therefore traps are more likely to be created at the crystal planes perpendicular to the <110> direction [5,6].

Moreover, the oxide reliability manifestation has also changed with downscaling, emphasising the discrete degradation steps now routinely measured for ultra-scaled transistors, corresponding to individual trapped charges [6–8]. Due to the scaled transistor dimensions and capacitor values, single trapping events can induce a critical change in device performances, therefore limiting the circuit design windows.

It is, therefore, of paramount importance to develop suitable frameworks for simulation and understanding of these phenomena at atomic scale. In this paper we evaluate the steady state reliability of NWTs at TCAD level by means of statistical simulations within a Schrödinger corrected drift-diffusion (DD) framework. The Random Telegraph Noise (RTN) behaviour is investigated as well as the multi-trap degradation responsible for the Bias Temperature Instabilities (BTI). Poisson–Schrödinger results are compared to classical drift diffusion simulation, emphasising the importance of the crystal orientation.

2. Methodology

The investigated ‘template’ device is a square NWT with 5 nm channel width, a 10 nm gate length, a 0.8 nm equivalent oxide thickness and a $10^{15}/\text{cm}^3$ net channel doping. The device geometry is illustrated in Fig. 1. We use the Gold Standard Simulations (GSS) 3D TCAD simulator GARAND. The simulation flow is illustrated in Fig. 2; classical drift diffusion simulations, which may include also a first guess of density-gradient electron masses correction are used to provide an initial solution to the Poisson–Schrödinger (PS) solver [9]. In this paper we use a valley reduction technique, eliminating the upper valleys (L - and Γ -valleys) of the silicon conduction band to speed up the solution. For

* Corresponding author.

E-mail address: Louis.gerrer@glasgow.ac.uk (L. Gerrer).

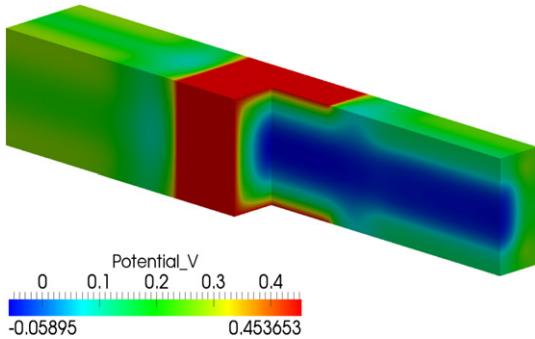


Fig. 1. Poisson–Schrödinger obtained potential of a 5×5 nm square nanowire at $V_d = 0.05$ V and $V_g = 0.8$ V with a $<100>$ channel orientation.

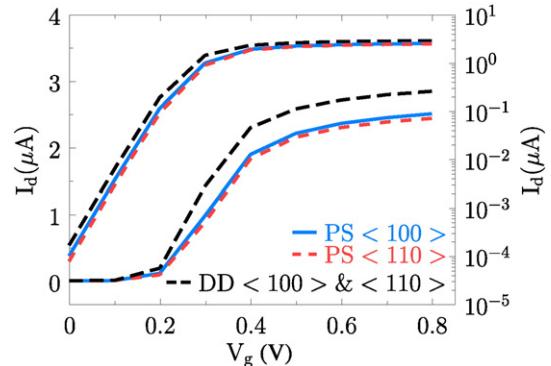


Fig. 3. Linear and logarithmical plots of drain current I_d characteristic for drift-diffusion (DD) simulations and Poisson–Schrödinger corrected DD (PS) for the two channel orientation $<100>$ and $<110>$.

the same reason, only the five first sub-bands, which in silicon NWTs with the simulated dimensions contain the majority of charge, are solved. In post-PS solution, a quantum correction potential is obtained utilising the Schrödinger solution and then used within the quantum corrected drift-diffusion iterations. The simulated current-voltage characteristics are presented in Fig. 3 for the classical simulations and for Schrödinger corrected drift-diffusion simulations. Of course for such nanometric devices the classical approach is inaccurate and we present it only to emphasise the impact of the quantum confinement on the charge distribution and the electrostatic effects, in order to highlight the feature related to our reliability simulations in different crystal orientations. The charge distribution at $V_g = 0.6$ V is presented in Fig. 4 comparing the results obtained from the classical, density gradient corrected DD, and Poisson–Schrödinger simulations in the $<100>$ and $<110>$ channel orientations. Note that the electron masses used in the density gradient correction are initial guesses. As it can be seen, comparing the three methodologies emphasises the necessity of a full quantum approach and of a crystal orientation aware design.

3. Results

In order to investigate the impact of the crystal orientation on steady-state RTN and BTI effects, we have generated a sample of hundred randomly distributed interface traps; however the probability of having a trap on the side interfaces in the $<110>$ channel orientation is twice more probable compared to the $<100>$ channel orientation, following measurement results and this effect enhances the quantum confinement differences between these two crystal orientations. Results are presented in Fig. 5 and Table 1, showing larger impact and broader dispersion on V_t for the quantum simulations, because of the higher spatial confinement of the charge distribution particularly in the $<110>$ orientation, as shown in Fig. 4. Indeed in the classical approach, no quantum effects are accounted for, so that the charge concentrates in a 2D sheet near the interfaces; whereas PS obtained charge distribution spread in a volume in the centre of the wire, progressively formed when inverting the channel. As a result, a fixed charge in the PS framework causes more impact than in the classical approach.

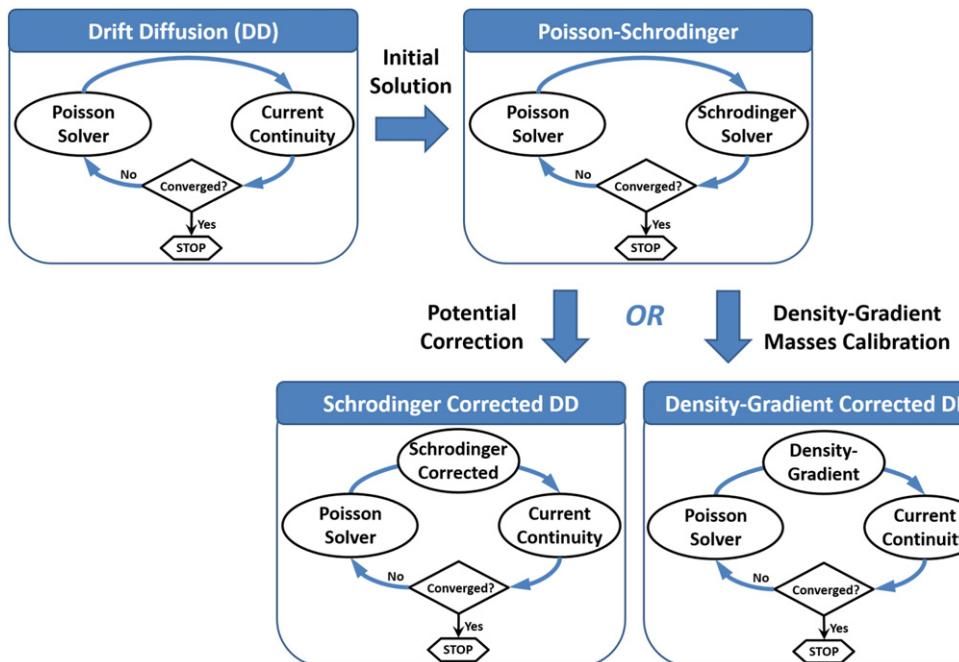


Fig. 2. Schrödinger corrected drift-diffusion framework also allows the calibration of density-gradient masses for computationally efficient DD framework.

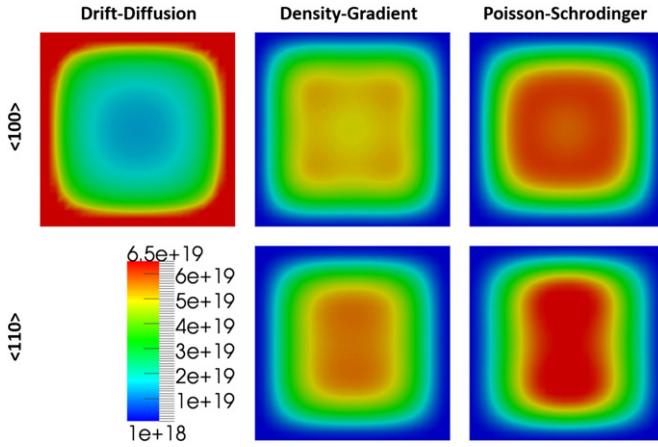


Fig. 4. Electron density at $V_g = 0.6$ V for drift-diffusion (DD), density-gradient corrected (DG) and Poisson-Schrödinger (PS) simulations for the two channel orientation $<100>$ and $<110>$.

However the impact on the ON current is lower for PS than for the classical DD one because the inversion layer is pushed away from the interface. For the same reason the difference between the orientations is much lower in the classical case and the sample size has to be increased to reach a conclusion on this point.

Figs. 6 and 7 explain the reasons for the observed dispersion in ΔV_t in the two crystal orientations. Since the potential barrier modulation between source and drain is responsible for the device threshold voltage, the maximum trap impact occurs for a charge located at the top of this barrier which is located in the middle of the NWT channel, as can be seen in Fig. 6. Fig. 7 shows the single trap impact distribution along the Y and Z axes of the device. As previously mentioned the dispersion of DD obtained trap impact is lower than the PS results. Indeed due to

Table 1

Average and standard deviation of single trap induced threshold voltage shifts for both DD and PS approaches in the two investigated crystal orientations.

	$<100>$		$<110>$	
	DD	PS	DD	PS
$\langle \Delta V_t \rangle$ (mV)	14.7	17.3	15.4	18.5
$\sigma(\Delta V_t)$ (mV)	5.0	6.5	5.0	6.6
$\langle \Delta I_{on} \rangle$ (μA)	-0.010	-0.006	-0.010	-0.006
$\sigma \langle \Delta I_{on} \rangle$ (μA)	0.004	0.003	0.004	0.003

this charge confinement at the interfaces, corner traps and central traps insert more or less the same impact. On the contrary in the PS approach, corner traps are farer away from the inverted part of the channel compare to central traps which results in the observed broader dispersion. Additionally the effects of the different crystal orientation dependent geometries of the inversion volume, shown in Fig. 4, can be observed again in the distribution of the trap impact in Fig. 7.

In Fig. 8 we repeat this experiment for BTI like steady state impact of trapped charges at average trapped charge density of $1 \times 10^{12} \text{ cm}^{-2}$ in the $<100>$ channel orientation. For the $<110>$ one, double the density of traps are placed at the sidewall interface corresponding to a trap density of $1.5 \times 10^{12} \text{ cm}^{-2}$. In this case we can clearly see the specific effect of the quantum confinement, leading to higher impact on I_{on} within the DD framework whereas the higher trap density on the $<110>$ channel sidewalls leads to higher impact on the threshold voltage when the inversion layer is not fully formed. Table 2 provides the threshold voltage and on-current average and standard deviation for DD and PS approaches for both orientations. Table 3 and Fig. 9 extend our observation to higher trap densities, namely $2 \times 10^{12} \text{ cm}^{-2}$ for the $<100>$ and $3 \times 10^{12} \text{ cm}^{-2}$ for the $<110>$. While the difference between trap densities increases, the average impact difference increases as well. The difference in the impact dispersion is, however, slightly reduced. Fig. 10 presents a comparison between DD and PS simulated impacts for the

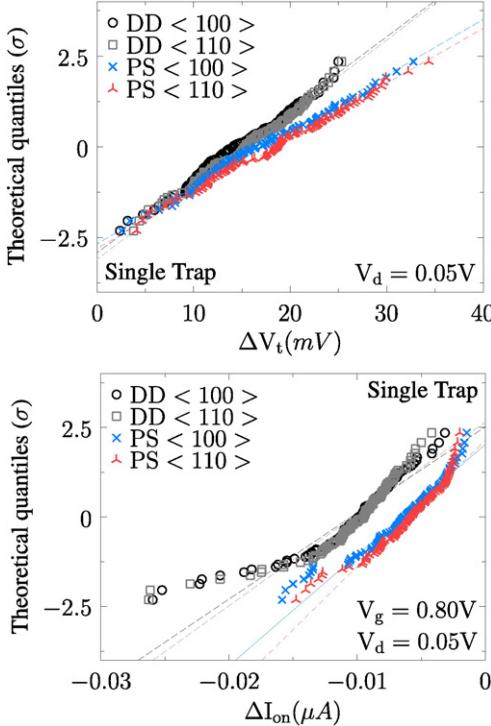


Fig. 5. Top: single trap induced threshold voltage shifts ΔV_t and bottom: on current ΔI_{on} shifts for Schrödinger corrected DD and drift-diffusion frameworks in both channel orientations.

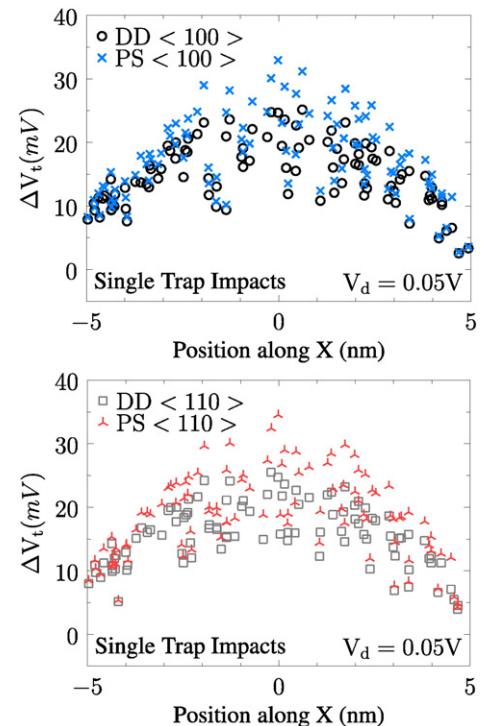


Fig. 6. Single trap impact comparison between PS and DD approaches in the $<100>$ (top) and $<110>$ (bottom) orientations.

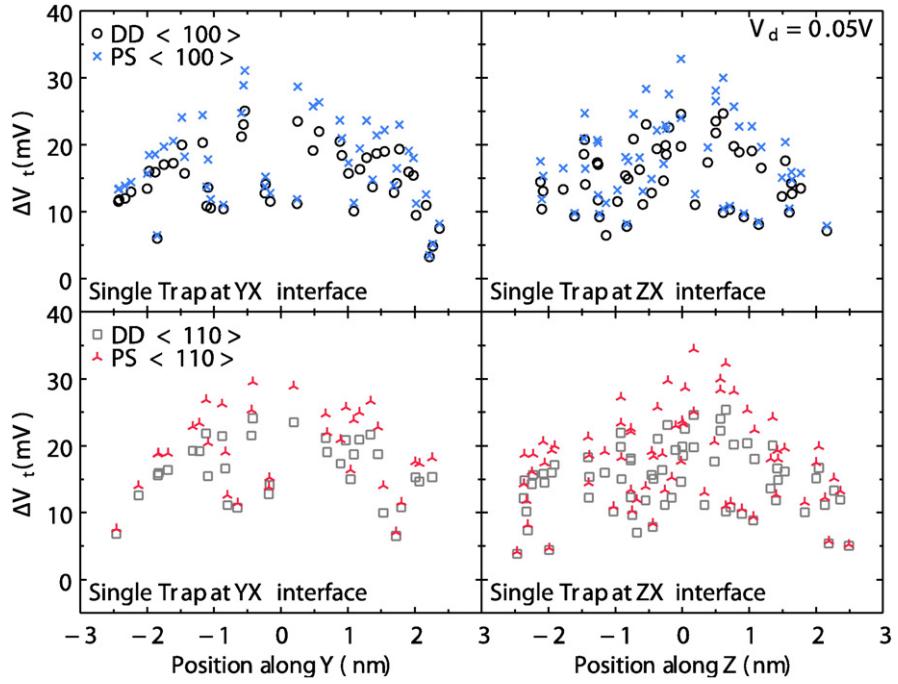


Fig. 7. Single trap impact comparison between PS and DD approaches in the <100> (top) and <110> (bottom) orientations.

two orientations for a) a single trap, b) $1 \times 10^{12} \text{ cm}^{-2}$, and c) $2 \times 10^{12} \text{ cm}^{-2}$ for the <100> orientation (respectively b) $1.5 \times 10^{12} \text{ cm}^{-2}$ and c) $3 \times 10^{12} \text{ cm}^{-2}$ in the <110> orientation). The difference between DD and PS for the threshold voltage impact is decreasing when increasing the number of traps, whereas it is remaining constant in the case of the ON current. This can be understood by

considering the inversion layer formation: while it is fully formed at high gate bias, leading to the constant DD/PS difference in the trap impact on current, it is actually forming around threshold and, because of the charged traps which decay the threshold voltage, it is actually less formed for higher trap densities at a constant V_g . Thus the difference in the DD/PS trap impact on the threshold voltage becomes lower and lower when increasing the trap density. Fig. 10 shows also the increasing difference between the orientations, when increasing the trap density, for this also increases the difference between traps densities in the two orientation.

Figs. 11 and 12 summarize the conclusions of this work, showing the devices presenting the maximum impact respectively on threshold and on the ON current. Presented slices have been cut at the trap positions, illustrating the combination of their impact to obtain the maximum effect on the device.

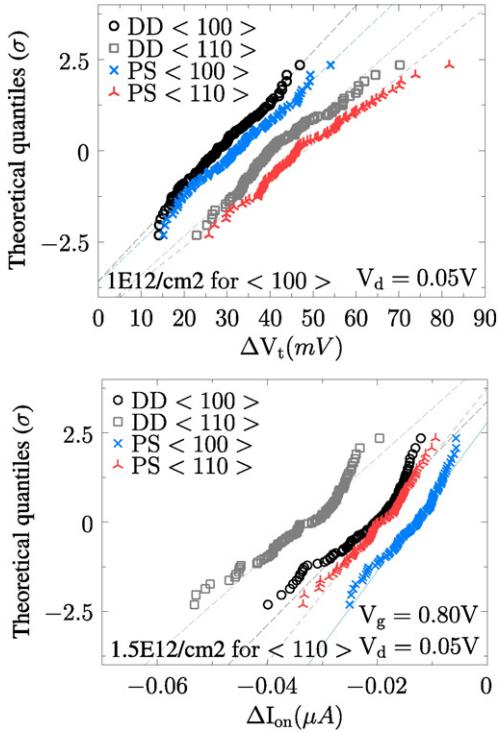


Fig. 8. Top: multi-trap induced threshold voltage shifts ΔV_t and bottom: on current ΔI_{on} shifts for Schrödinger corrected DD and DD frameworks. Sidewalls have twice more traps in the <110> orientation.

Table 2
Average and standard deviation of multi-trap induced threshold voltage shifts for both DD and PS approaches in the two investigated crystal orientations.

	<100>		<110>	
	DD	PS	DD	PS
$\langle \Delta V_t \rangle$ (mV)	28.4	32.5	42.2	48.2
$\sigma(\Delta V_t)$ (mV)	8.0	9.0	9.5	10.7
$\langle \Delta I_{on} \rangle$ (μA)	-0.022	-0.013	-0.033	-0.019
$\sigma(\Delta I_{on})$ (μA)	0.006	0.005	0.007	0.005

Table 3
Average and standard deviation of multi-trap induced threshold voltage shifts for both DD and PS approaches in the two investigated crystal orientations.

	<100>		<110>	
	DD	PS	DD	PS
$\langle \Delta V_t \rangle$ (mV)	56.4	62.5	82.4	92.2
$\sigma(\Delta V_t)$ (mV)	13.3	13.5	14.2	14.6
$\langle \Delta I_{on} \rangle$ (μA)	-0.045	-0.028	-0.073	-0.043
$\sigma(\Delta I_{on})$ (μA)	0.009	0.007	0.013	0.008

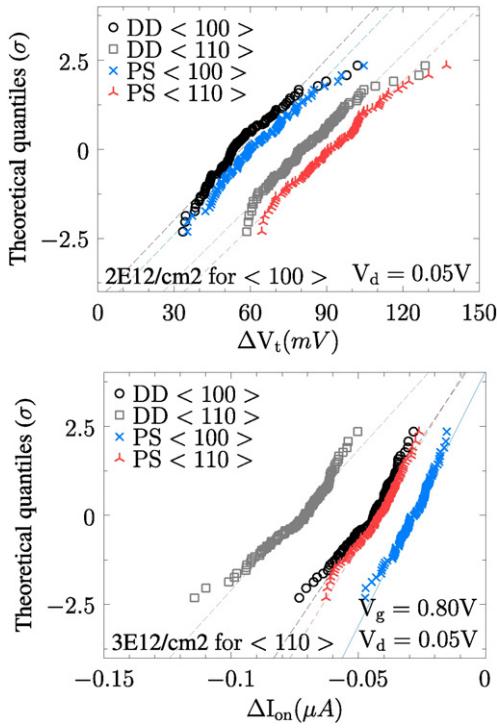


Fig. 9. Top: multi-trap induced threshold voltage shifts ΔV_t and bottom: on current ΔI_{on} shifts for Schrödinger corrected DD and DD frameworks. Sidewalls have twice more traps in the <110> orientation.

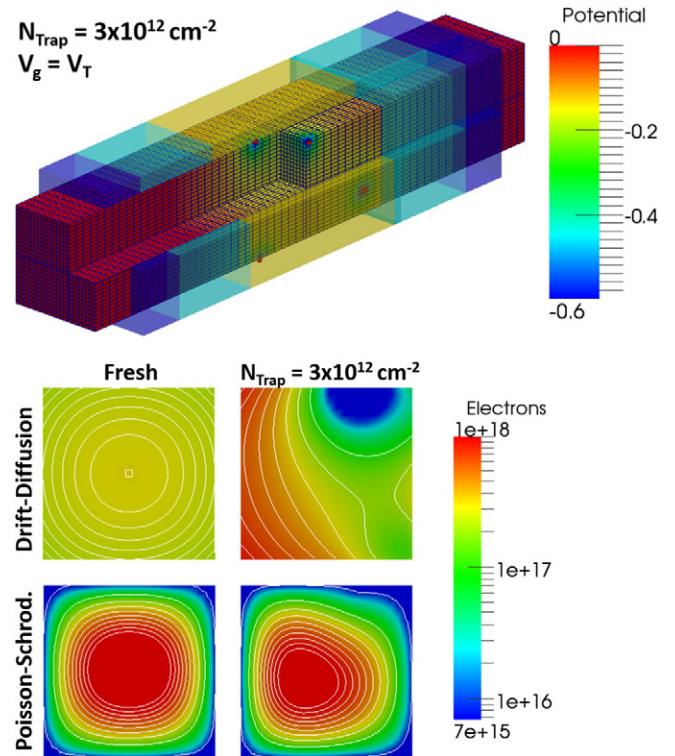


Fig. 11. Top: <110> oriented device featuring the maximum V_T shift from a $3 \times 10^{12} \text{ cm}^{-2}$ trap density; wire coloured by potential at threshold, surrounding transparent volumes illustrate gate and spacers positions. Bottom: comparison between PS and DD obtained electrons densities for fresh and degraded device across the wire at a central trap position.

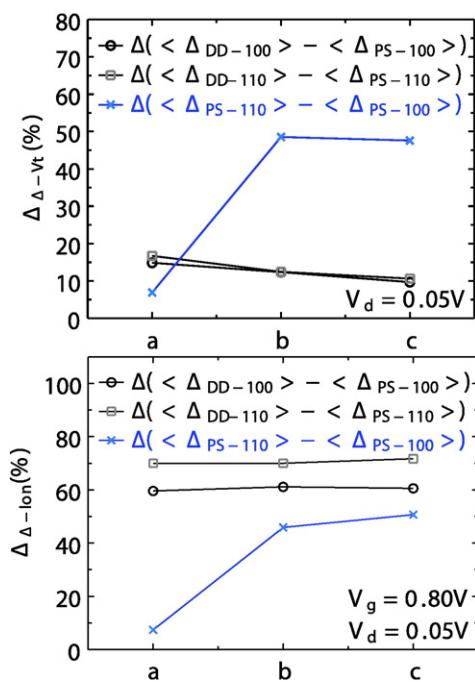


Fig. 10. Top: multi-trap induced threshold voltage shifts ΔV_t and bottom: on current ΔI_{on} shifts for Schrödinger corrected DD and DD frameworks. Sidewalls have twice more traps in the <110> orientation.

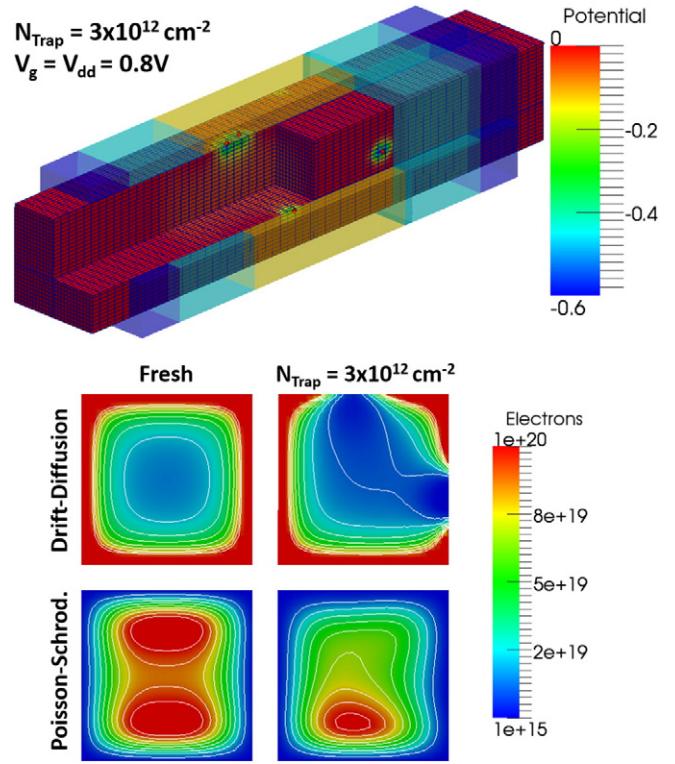


Fig. 12. Top: <110> oriented device featuring the maximum I_{on} shift from a $3 \times 10^{12} \text{ cm}^{-2}$ trap density; coloured by potential. Bottom: comparison between PS and DD obtained electrons densities for fresh and degraded device across the wire at a central trap position.

4. Conclusion

Quantum effects are dominant in aggressively-scaled NWTs. In this paper we have presented results of Schrödinger corrected drift-diffusion simulations compared to the classical approach. As different channel orientations exhibit different confinement depending on the direction, the RTN and BTI impacts differ as well. Moreover the higher dangling bond density and roughness at the $<110>$ channel sidewall interfaces lead to higher impact on the threshold voltage while at higher gate biases these two effects are combined. Further efforts are needed towards full-scale quantum transport simulation using non-equilibrium green functions. Regarding statistical simulations the density gradient masses need to be accurately calibrated in order to test the validity of this approach and proceed to large sample simulations, including the impact of statistical variability on RTN and BTI.

Acknowledgment

This work has been funded by the EPSRC framework, the related project number L010585 is entitled: “Time-Dependent Variability: A test-proven modelling approach for system verification and power consumption minimization”.

References

- [1] J.H. Kuhn, Considerations for ultimate CMOS scaling, *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* 59 (7) (2012) 1813–1828.
- [2] A. Asenov, A.R. Brown, J.H. Davies, S. Kaya, G. Slavcheva, Simulation of intrinsic parameter fluctuations in decanometer and nanometer-scale MOSFETs, *IEEE Trans. Electron Devices* 50–9 (2003) 1837–1852.
- [3] A.R. Brown, A. Asenov, J.R. Watling, Intrinsic fluctuations in sub 10-nm double-gate MOSFETs introduced by discreteness of charge and matter, *IEEE Trans. Nanotechnol.* 1 (4) (2002) 195–200.
- [4] L. Gerrer, S.M. Amoroso, S. Markov, F. Adamu-Lema, A. Asenov, 3-D statistical simulation comparison of oxide reliability of planar MOSFETs and FinFET, *IEEE Trans. Electron Devices* 60–12 (2013) 4008–4014.
- [5] C.D. Young, K. Akarvardar, M.O. Baykan, K. Matthews, I. Ok, T. Ngai, et al., (1 1 0) and (1 0 0) sidewall-oriented FinFETs: a performance and reliability investigation, *Solid State Electron.* 78 (2012) 2–10.
- [6] M. Cho, R. Ritzenthaler, R. Krom, Y. Higuchi, B. Kaczer, T. Chiarella, et al., Negative bias temperature instability in p-FinFETs with 45° substrate rotation, *IEEE Electron Device Lett.* 34 (10) (2013) 1211–1213.
- [7] T. Grasser, et al., Stochastic charge trapping in oxides: from random telegraph noise to bias temperature instabilities, *Microelectron. Reliab.* 52 (1) (2012) 39–70.
- [8] M. Toledano-Luque, B. Kaczer, J. Franco, Ph.J. Roussel, T. Grasser, T.Y. Hoffmann, et al., From mean values to distributions of BTI lifetime of deeply scaled FETs through atomistic understanding of the degradation, *Symposium on VLSI Technology Digest of Technical Papers* 2011, pp. 152–153.
- [9] <http://www.goldstandardsimulations.com>.