Impact of Self-Heating on the Statistical Variability in Bulk and SOI FinFETs

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***Abstract*—In this paper for the first time we study the impact of self-heating on the statistical variability of bulk and SOI FinFETs designed to meet the requirements of the 14/16nm technology node. The simulations are performed using the GSS 'atomistic' simulator GARAND using an enhanced electro-thermal model that takes into account the impact of the fin geometry on the thermal conductivity. In the simulations we have compared the statistical variability obtained from full-scale electro-thermal simulations with the variability at uniform room temperature and at the maximum or average temperatures obtained in the electro-thermal simulations. The combined effects of line edge roughness and metal gate granularity are taken into account. The distributions and the correlations between key figures of merit including the threshold voltage, on-current, subthreshold slope and leakage current are presented and analysed.**

***Index Terms*—CMOS, electro-thermal simulations, FinFETs, statistical variability, correlations**

I. Introduction

FinFETs enable technology scaling at the 22nm CMOS technology generation and beyond because of their excellent electrostatic integrity and control of short channel effects [1]. This is complemented by lower statistical variability due to a tolerance of lower channel doping compared to bulk transistors. Self-heating has been highlighted as one of the areas of concern for FinFETs because of the 3D geometry, the impact of the corresponding 3D heat flow through the fin to the substrate and the impact of the fin geometry on the local thermal conductivity [2-8]. These perceived self-heating problems could be exacerbated in SOI FinFETs where the thermal conduction towards the substrate is impeded by the low thermal conductivity of the SOI layer beneath the fin [7]. Therefore analyzing and modeling the self-heating in FinFETs and the influence on device performance has become one of the topics attracting a lot of recent interest [2-8].

At the same time, statistical variability introduced by the discreteness of charge and matter has become critically important in contemporary and future CMOS technologies [9-10]. In particular the impact of random discrete dopants (RDDs), fin line edge roughness (FER), gate line edge roughness (GER), and metal gate granularity (MGG) on the variability in bulk and SOI FinFETs have been studied in detail previously [11]. However to the best of our knowledge the impact of self-heating has not be taken into account before in such simulation studies.

In this paper we use the enhanced self-heating simulation capabilities, recently introduced in the GSS 'atomistic' device simulator GARAND [8,12], complemented by the unique capabilities for physical simulation of different sources of statistical variability [13-14], to study, for the first time, the impact of self heating on FinFET variability. The test-bed transistors in this study are bulk and SOI FinFETs designed to meet the specifications for the 14/16nm CMOS technology generation [11].

The paper is organized as follows: In section II we briefly describe the bulk and the SOI FinFETs used as demonstrators in this study. Section III presents the simulation technology including the enhanced electro-thermal simulation method in more detail along with the physical statistical simulation capabilities. The results and analysis of statistical variability in the presence of self-heating effects are presented in Section IV. Finally the conclusions are drawn in Section V.

II. The Testbed Transistors

Two n-channel FinFETs, which are on SOI and bulk substrates respectively but have identical dimensions, are used as a test bed in our investigation. Their schematic structures are illustrated in Fig. 1. The nominal device parameters are listed in Table 1. For the bulk FinFET, a 5×10^{18} cm^{-3} channel stop doping is introduced below the channel. A conservative channel length of L_G=25nm was assumed. A high-k gate dielectric is used to minimise gate leakage. Table 2 compares the key figures of merit of the two transistors, which are very similar in terms of performance.

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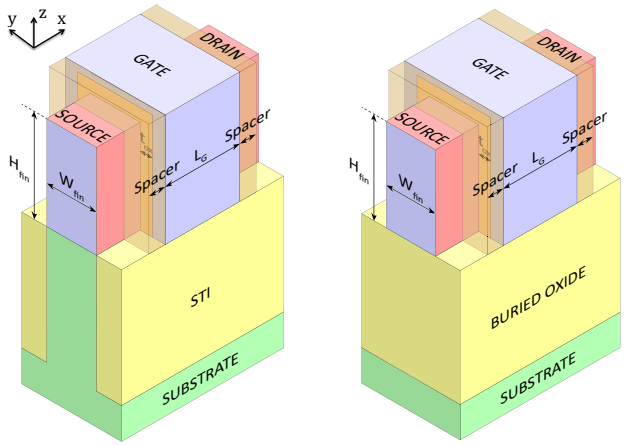


a) b)

Fig. 1. The schematic view of the (a) bulk and (b) SOI FinFETs.

TABLE I. NOMINAL DEVICE PARAMETERS

Parameter	Value
L_G	25 nm
Fin Width, W_F	12 nm
Fin Height, H_F	30 nm
Spacer	6 nm
Extension	No extension doping
highly doped drain (HDD) profile	2nm/dec (σ=2.1nm)
highly doped drain (HDD) doping	1×10^{20} cm^{-3}
Equivalent Oxide Thickness (EOT)	0.8 nm
Channel stop doping	5×10^{18} cm^{-3}
Channel doping	1×10^{15} cm^{-3}
BOX / STI depth	30 nm
Supply Voltage	0.9 V

TABLE II. THE KEY FIGURES OF MERIT OF THE TWO TRANSISTORS

	Bulk FinFET	SOI FinFET
VTlin (Volts)	0.286	0.294
VTsat (Volts)	0.254	0.258
SS (mV/decade)	69.8	71.1
DIBL (mV)	31.6	36.8
IDlin (mA/μm)	0.342	0.360
IDsat (mA/μm)	1.177	1.244

III. SIMULATION METHODOLOGY

A. *Electro-thermal simulations*

Within the framework of the GSS statistical-variability-aware device simulator GARAND [12], we have developed a thermal simulation module to investigate the impact of self-heating on FinFET DC operation and on the corresponding statistical variability. This module is based on the solution of the coupled Heat Flow, Poisson, and Current Continuity Equations [8].

Usually the electrical characteristics of the device are calculated in a restricted device simulation domain in order to maximize computational efficiency. However, heat is dissipated in a much larger domain, including the active region of the transistor, its neighbors, the substrate, the interconnect layers, the case, and eventually the heat sink. Therefore, realistic thermal boundary conditions rely on thermal resistances, employed to account for heat dissipation into interconnects, the wafer, the case, etc. For given values of thermal resistances, GARAND calculates the temperature differences using an iterative scheme according to the temperature gradient until convergence is achieved.

Since the fin thickness (width) is of the order of 10 nm, the thermal conductivity can be significantly reduced compared to bulk Si due to phonon-boundary scattering. We employ a new approximate formula for the calculation of the thermal conductivity in the fin region, which extends the previous 1D formula [15] to 2D [8]. Considering a fin of height h and width w as shown in Fig. 2, the thermal conductivity of the fin is given by

$$\kappa(y,z,T)=\kappa_0(T)\int_0^{\pi/2}\sin^3\theta\left\{1-\exp\left(-\frac{h}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{h-2z}{2\lambda(T)\cos\theta}\right)\right\}d\theta \Big/ \int_0^{\pi/2}\sin^3\theta\left\{1-\exp\left(-\frac{w}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{-2y}{2\lambda(T)\cos\theta}\right)\right\}d\theta \quad (1)$$

where y and z are the coordinates, T is the lattice temperature, $\lambda(T)$ is phonon mean free path with temperature dependence, $\kappa_0(T)$ is the parameterized bulk thermal conductivity with temperature dependence and θ is the integral variable.

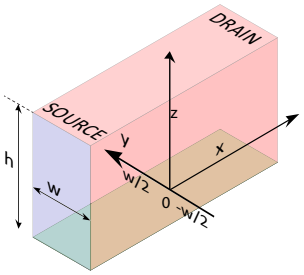
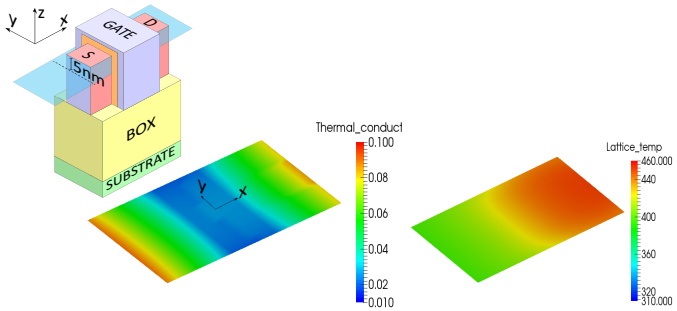


Fig. 2. A fin of height h and width w. The z-axis is along the direction of fin height with the bottom and top surfaces of the fin being at z=0 and z=h, and the y-axis is along the direction of fin width with the surfaces of the fin being at y=-w/2 and y=w/2.

Using this new calculation method, the thermal conductivity of the fin is predicted to be 1~2 orders of magnitude lower than conventional value of the thermal conductivity for bulk Si. In our electro-thermal simulation module, the thermal conductivity at each mesh point in the fin is refreshed according to its spatial position and temperature at each iteration cycle, which ensures the self-consistency of the simulation. By using this formula, the thermal conductivity and lattice temperature in a slice of the fin, which is 5nm below the top gate in the SOI FinFET example, resulting from the self-consistent simulations are illustrated in Fig. 3. The thermal conductivity in the middle of the fin is 0.027W/(cm K). Currently the parameters are adopted from [15], which can be recalibrated if novel experimental data for a nanoscale fin structure becomes available in literature. The anisotropy of thermal conductivity is not included in this work, but will be considered at a future stage.

In the electro-thermal simulations of the bulk and SOI FinFETs, at the bottom of the simulation domain and at the top of the source and drain contacts external thermal resistances are employed and the temperature at these boundaries is calculated according to the values of thermal resistances and heat flow. 2×10^6 K/W substrate thermal resistance and two 1×10^6 K/W contact thermal resistances have been used in this case based on rough estimation. The external thermal resistances are user-specified parameters for the electro-thermal simulation module. The values used here are just for demonstration. A good estimation for external thermal resistances should consider the bulk resistance, interface resistances, effects of heat radiation and spreading. The Masetti model [16] is used for doping-dependent low-field mobility, enhanced Lombardi model [17] is used for perpendicular field-dependent mobility and Caughey-Thomas model [18] is used for lateral field-dependent mobility. Temperature dependency is included in the mobility models and saturation velocity. The reduced thermal conductivity of the fin is taken into account according to Eq. (1).



(a) (b)

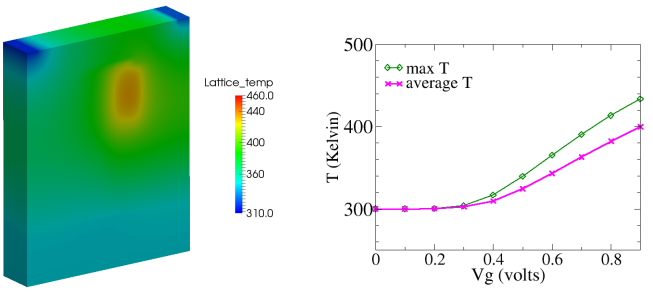
Fig. 3. (a) Thermal conductivity and (b) lattice temperature in a slice of the fin which is 5nm below the top gate in the SOI FinFET example, at Vg=Vd=0.9V, finally obtained from the self-consistent simulation. Inset: schematic showing the cut plane.

The corresponding simulated lattice temperature distribution at high drain voltage (0.9V) and gate bias of 0.9V for the bulk FinFET is illustrated in Fig. 4 (a). At different gate bias, the maximum lattice temperature and average temperature of the fin resulting from the electro-thermal simulations are illustrated in Fig. 4 (b), which show how device temperature is evolving as a function of Vg. The corresponding Id-Vg characteristics are shown in Fig. 5, where the plotted Id is the total drain current divided by the effective fin width, i.e. $W = 2H_F + W_F$. The corresponding simulation results for the SOI FinFET are illustrated in Fig. 6 and Fig. 7. Due to the much lower thermal conductivity of the fin, a significant hot spot is produced near the drain, with peak lattice temperature reaching 457K in the SOI FinFET and reaching 433K in the bulk FinFET. This also indicates strong temperature gradients in the region, which affect the local current density through the additional part related to thermal gradient ∇T_L:

$$J_n = qn\mu_n E_n + k\mu_n T_L \nabla n + k\mu_n n \nabla T_L \qquad (2)$$

where n is the electron density, μ_n is the electron mobility, k is Boltzmann constant.

For comparison, simulations without self-heating, where the lattice temperature is geometrically uniform in the device region, are performed. Results are presented at uniform room temperature and at the temperature corresponding to the maximum temperature observed within the device during the electro-thermal simulations. In addition, we run simulations without self-heating at a constant temperature defined by the maximum temperature (as green lines in Fig. 4(b) and Fig. 6(b)), and defined by the average temperature in the fin (as purple lines in Fig. 4(b) and Fig. 6(b)), at each individual Vd and Vg bias condition obtained from the electro-thermal simulations, which is denoted as “step Tmax” and “step Tavg” respectively. As shown in Fig. 5 and Fig. 7, the self-heating produces higher drain current in the Vg range of 0.4~0.7V, the reason being that the impact on the Vth/SS is stronger than the mobility reduction.



(a) (b)

Fig. 4. Simulation results for the bulk FinFET. (a) Lattice temperature profile in the middle at Vg=Vd=0.9V; (b) maximum temperature and average temperature in the fin at high drain voltage

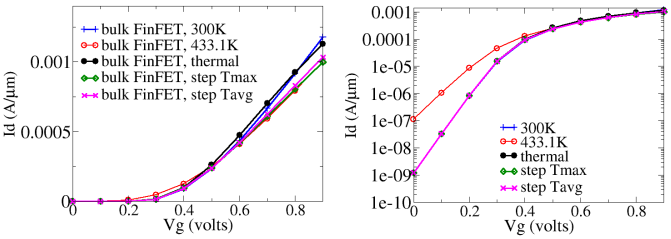
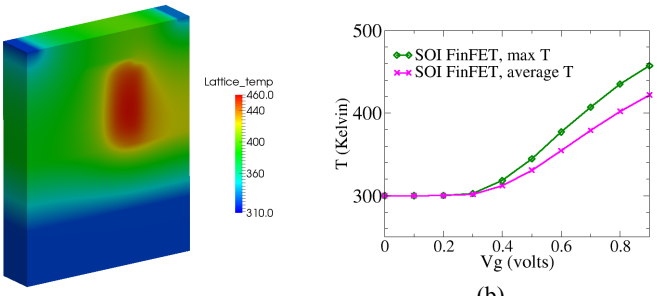


Fig. 5. Simulated Id-Vg characteristics at high drain voltage for the bulk FinFET. Left: on linear scale; right: on logarithmic scale. The self-heating produces lower on-current, however, its impact is different from uniform temperature simulations.



(a) (b)

Fig. 6. Simulation results for the SOI FinFET. (a) Lattice temperature profile in the middle at Vg=Vd=0.9V; (b) maximum temperature and average temperature in the fin at high drain voltage.

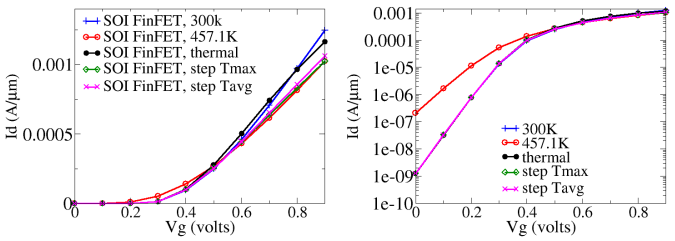


Fig. 7. Simulated Id-Vg characteristics at high drain voltage for the SOI FinFET. Left: on linear scale; right: on logarithmic scale. The self-heating produces lower on-current, however, its impact is different from uniform temperature simulations.

B. Statistical variability simulations

The electro-thermal simulation module is integrated seamlessly with the statistical variability simulation capability of GARAND. Line edge roughness (LER) is modelled with the assumption that it follows a Gaussian autocorrelation function [19]. Both gate edge roughness (GER) and fin edge roughness (FER) are included in the simulations, with three times root-mean-square deviation of the gate edge position of 3Δ=2 nm and a correlation length of Λ=30 nm. In the modelling of MGG we assume a TiN metal gate with an average grain diameter of 5 nm and two major grain orientations which lead to a work-function (WF) difference of 0.2 V, and the probability for the lower and higher WF are 0.4 and 0.6 respectively [20-23]. For both bulk and SOI FinFET examples, ensembles of 400 microscopically different devices were simulated using the automated GSS cluster simulation technology, including combined sources of variability GER, FER and MGG.

The standard deviations of the threshold voltage are very similar for the two FinFETs: 19mv and 21mV for the bulk and the SOI FinFETs respectively. Correspondingly, the matching factors (defined as $A_{VT} = \sigma_{\Delta V_T}\sqrt{WL} = \sqrt{2}\sigma_{V_T}\sqrt{WL}$) for the two FinFETs are 1.14 mV.μm and 1.25 mV.μm respectively, where W in this case is the effective fin width, $W = 2H_F + W_F$.

IV. Electro-thermal Statistical Variability Study

Electro-thermal simulations have been performed on the FinFETs with statistical variations as detailed in Section III (B), and corresponding figures of merit including on-current (I_{on}) , threshold voltage (V_{th}), the subthreshold slope (SS) and the off-current (I_{off}) have been extracted. Fig. 8 shows the statistical distribution of the figures of merit at drain bias of 0.9V for the bulk FinFET obtained from the electro-thermal simulations, and the analogous distributions for the SOI FinFET are shown in Fig. 9. For comparison, results from variability simulations without self-heating for different cases as specified in Section III (A) are also plotted in these two figures. In these comparison simulations, the lattice temperature is geometrically uniform in the device region, and the value from the characteristics of the nominal device is used as the nominal temperature. Here Vth is VTsat and SS is extracted from the saturation curve.

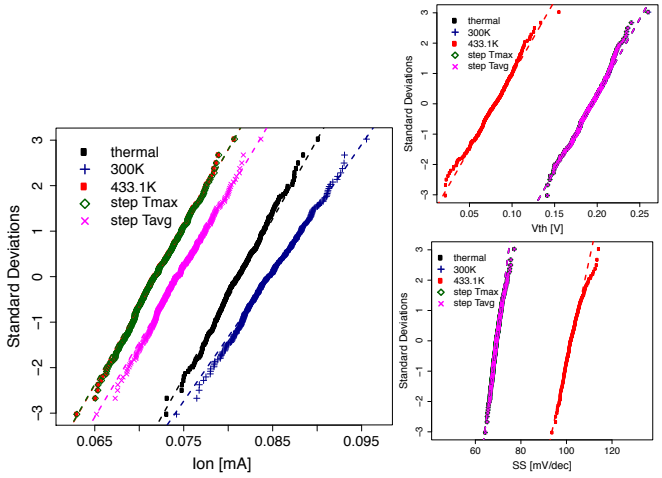


Fig. 8. Comparison of the statistical distribution of on-current for the bulk FinFET obtained from the electro-thermal simulations with uniform temperature simulation results without self-heating. Insets: threshold voltage and subthreshold slope. All at high drain bias. Impact of self-heating on the statistical distribution of the on-current is clearly shown, especially the reduction of the I_{on} variability.

It is not surprising that the self-heating only affects the distribution of the on-current (I_{on}) in the case of DC operation. The rest of the figures of merit are related to the subthreshold region where the self-heating effects are minimal, therefore there is no observable difference between the uniform room temperature simulation and the electro-thermal simulations. What is somewhat surprising is that the self-heating significantly reduces the I_{on} variability according to the electro-thermal simulations. The effect is more pronounced in the SOI FinFET where the self-heating is stronger. The explanation of this effect is related to a negative feedback associated with the statistical distribution of I_{on}. Devices from the higher-current part of the statistical distribution suffer more from the self-heating and their current is more reduced compared to the devices from the lower end of the statistical distribution. In order to illustrate this point Fig. 10 compares the temperature distribution of the two bulk FinFETs from Fig. 8 with the highest and lowest currents in the distribution. The maximum temperature in the first case is 440.8K and the maximum temperature in the second case is 410.8K, because microscopically the structures of the two cases are different due to different GER, LER and MGG patterns, leading to field and current density differences, and the corresponding differences in the heat generation.

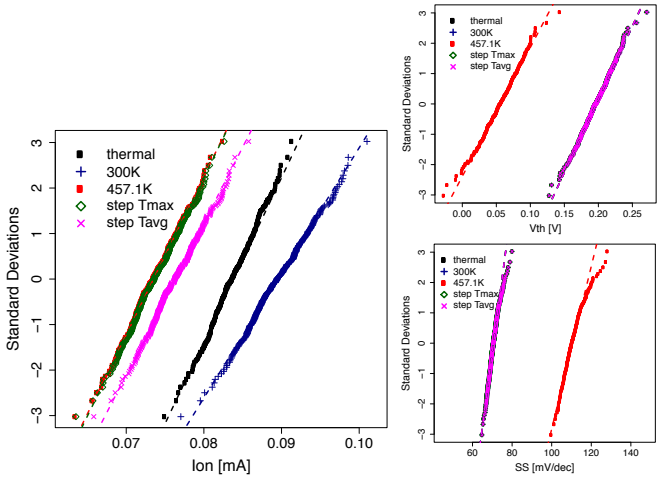
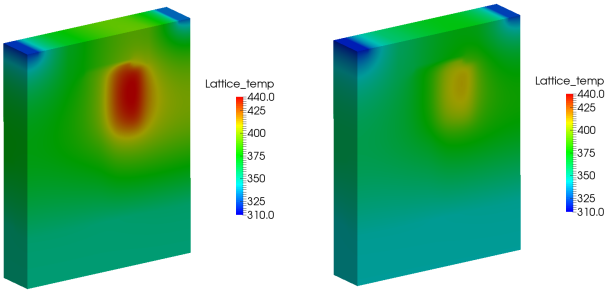


Fig. 9. Comparison of the statistical distribution of on-current for the SOI FinFET obtained from the electro-thermal simulations with uniform temperature simulation results without self-heating. Insets: threshold voltage and subthreshold slope. All at high drain bias. Impact of self-heating on the statistical distribution of the on-current is clearly shown, especially the reduction of the I_{on} variability.



(a) (b)

Fig. 10. Temperature distribution of the two bulk FinFETs from Fig. 8(a) with the (a) highest and (b) lowest currents in the distribution.

The averages and the standard deviations of I_{on} in the five types of simulations presented in Fig. 8 and Fig. 9 are summarized in Table 3. It verifies that both the average (μ) and the standard deviation (σ) for I_{on} have been reduced because of the self-heating effects. Due to the thermal isolation of the buried oxide, these effects are stronger in the SOI FinFET, where standard deviation of I_{on} reduced 1.1 μA from 3.7μA at uniform room temperature according to results from electro-thermal simulations. For bulk FinFET, the standard deviation of I_{on} reduced 0.7 μA from 3.4μA at uniform room temperature according to results from electro-thermal simulations. Looking at the normalized standard deviation of I_{on}, electro-thermal simulations give the results of 3% for both bulk and SOI FinFETs. Contrarily, a uniform increase in the temperature has a different impact: the reduction of average I_{on} is larger, while the standard deviation is comparable, therefore statistical variability is enlarged from the viewpoint of the normalized standard deviation (approximately 4% both for the bulk and the SOI FinFET examples). This means uniform increase of temperature in the whole device region cannot accurately reflect the trends of I_{on} variation, and the temperature gradient in the channel needs to be included when considering the full picture of self-heating effects.

TABLE III. THE MEAN AND STANDARD DEVIATION OF ON-CURRENT, EXTRACTED FROM SIMULATIONS FOR A STATISTICAL ENSEMBLE OF 400.

I_{on} (mA)		***Bulk FinFET***	***SOI FinFET***
Uniform 300K	**μ**	0.0847	0.0896
	σ	0.0034	0.0037
	σ_{normal}	4.0%	4.1%
Electro-thermal simulations	**μ**	0.0813	0.0838
	σ	0.0027	0.0026
	σ_{normal}	3.3%	3.1%
Uniform peak temperature	**μ**	0.0719	0.0736
	σ	0.0028	0.0029
	σ_{normal}	3.9%	3.9%
Step Tmax (maximum temperature at each individual step)	**μ**	0.0719	0.0736
	σ	0.0028	0.0029
	σ_{normal}	3.9%	3.9%
Step Tavg (average temperature in the fin at each individual step)	**μ**	0.0744	0.0764
	σ	0.0029	0.0030
	σ_{normal}	3.9%	3.9%

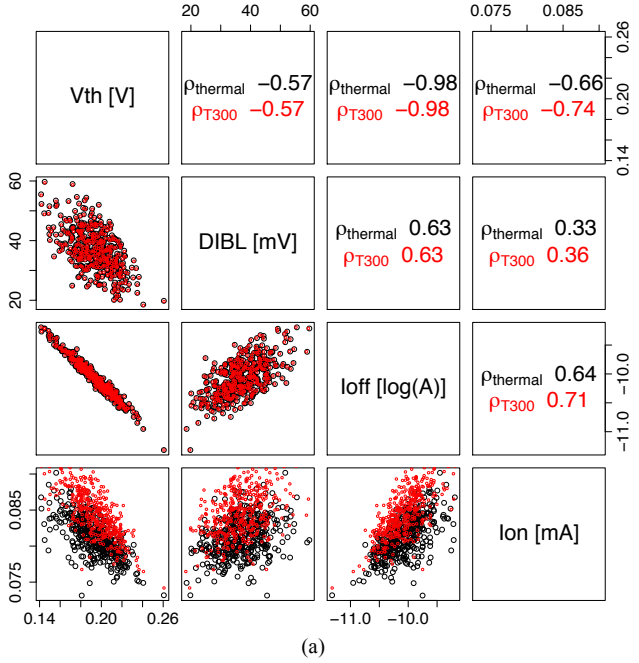
μ: mean; σ: standard deviation; σ_{normal}: normalized standard deviation.

As could be expected, the self-heating strongly affects the correlation between I_{on} and all other figures of merit. This is illustrated in Fig. 11 for both FinFETs, where the correlation coefficients can be read diagonally. For example, for the bulk FinFET the correlation coefficient between I_{on} and V_{th} changes from -0.66 at uniform room temperature to -0.74 according to the electro-thermal simulation, while for the SOI FinFET, change of this correlation coefficient due to self-heating is larger (from -0.70 to -0.80). These will provide useful information for compact modeling.

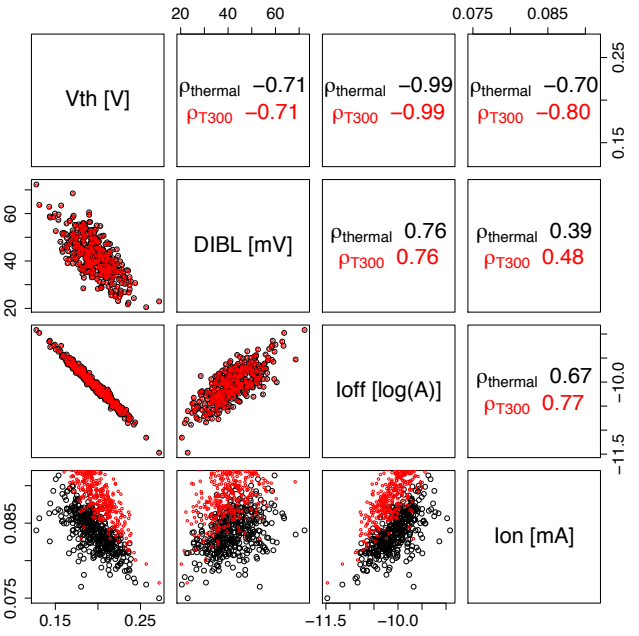
V. CONCLUSIONS

In this paper we present results obtained from the electro-thermal simulation of statistical variability in bulk and SOI FinFETs. The electro-thermal simulations take into account the impact of the fin geometry on the thermal conductivity. The reduced thermal conductivity has a dramatic effect on the self-heating, raising the peak temperature to 433K in the case of bulk FinFETs and to 457K in the case of SOI FinFETs. The self-heating has a strong impact in reducing the on-current variability but does not significantly affect the threshold voltage, subthreshold slope and off current variability. This in turn affects the correlation between the on-current distribution and the distributions of the rest of the figures of merit. This work focuses on the DC operation, while the impact on variability in circuit switching will strongly depend on the workload. A negative feedback between the current variability and the self-heating is indicated from our simulation.

In contrast, uniform increase of temperature in the whole device region cannot accurately reflect the trends of I_{on} variation, and the temperature gradient in the channel needs to be included when considering the full picture of self-heating effects.



(a)



(b)

Fig 11. Correlation between the figures of merit in the electro-thermal statistical simulation (in black) of (a) bulk and (b) SOI FinFETs, comparing to results with uniform lattice temperature at 300K (in red). The correlation coefficients can be read diagonally. The self-heating strongly affects the correlation between I_{on} and all other figures of merit.

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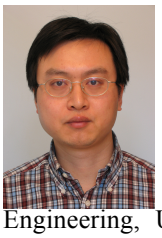

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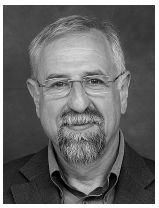

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